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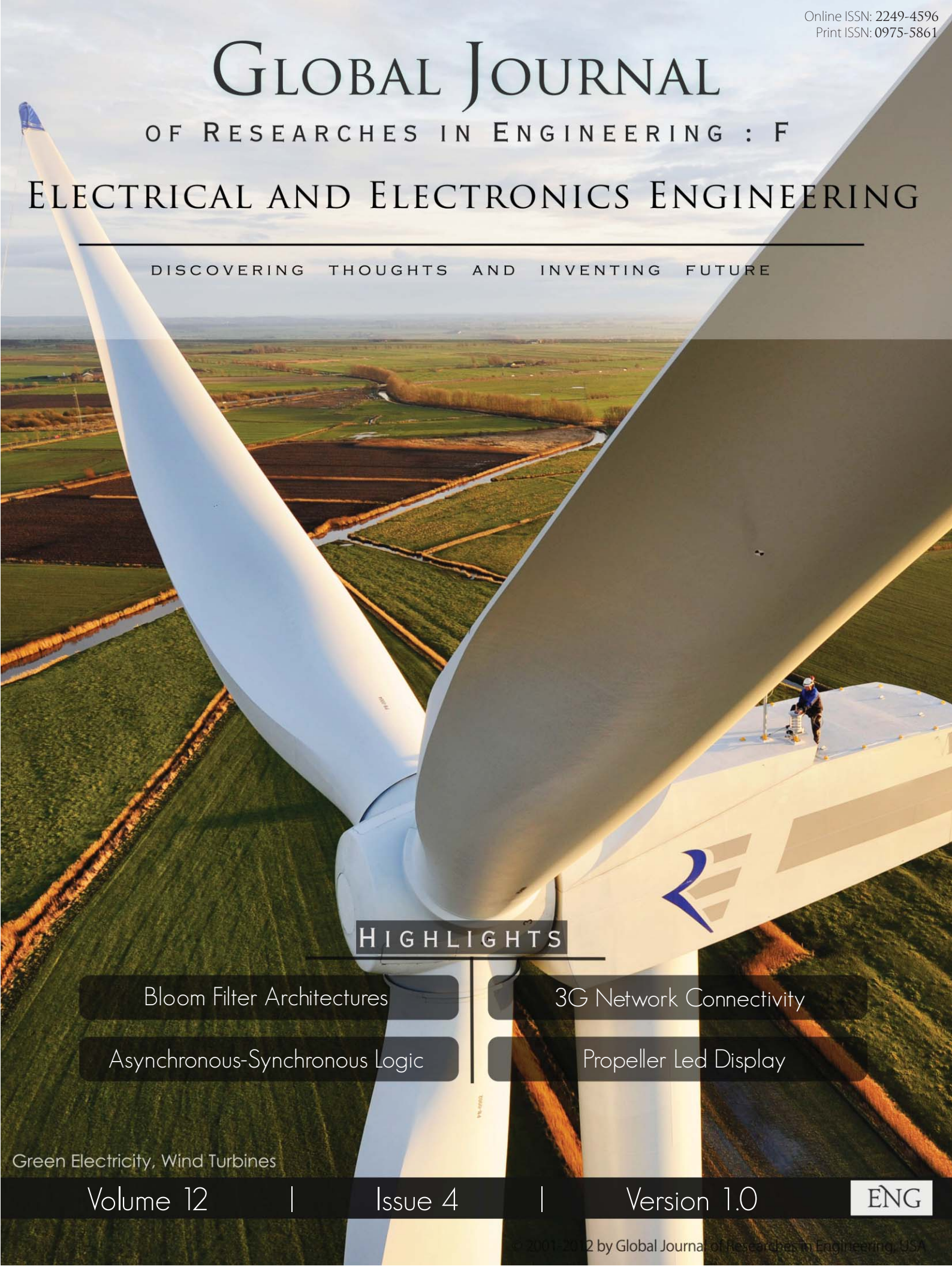

HIGHLIGHTS

- Bloom Filter Architectures
- 3G Network Connectivity
- Asynchronous-Synchronous Logic
- Propeller Led Display

Green Electricity, Wind Turbines

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Highly Secured Military Data Storage on SD/MMC Card

By Madhurya Mudiar & Megha Mukherjee
Smt. Indira Gandhi College of Engineering, India

Abstract - In today's environment when everything is computerized, the protection and secrecy of our information from theft and misuse has become really important. Today, more than ever before, security of data is a key issue for virtually every organization. In simple terms, data security is practice of keeping data protected from corruption and unauthorized access. The focus behind data security is to ensure privacy while protecting personal or corporate data.

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Highly Secured Military Data Storage on SD/MMC Card

Madhurya Mudiar[α] & Megha Mukherjee[σ]

Abstract - In today's environment when everything is computerized, the protection and secrecy of our information from theft and misuse has become really important. Today, more than ever before, security of data is a key issue for virtually every organization. In simple terms, data security is practice of keeping data protected from corruption and unauthorized access. The focus behind data security is to ensure privacy while protecting personal or corporate data.

I. Introduction

Software based security solution encrypt the data to prevent data from being stolen. However, a malicious program or a hacker may corrupt the data in order to make it unrecoverable or unusable. Similarly, encrypted operating system can be corrupted by a malicious program or a hacker, making the system unusable. Hardwarebased security solution can prevent read and write access to data and hence offer very strong protection against tampering and unauthorized access.

II. Background Overview

a) Existing System

The following are the current system for the data storage…

- Now a day Transferring or taking secured Data from one place to other is prime requirement of all the companies. Industries, Institute, Laboratories etc.
- Basic method to do so are either to encode or Zip the Data by one or other software and transfer it by Internet or store the Data in any hardware to carry information.

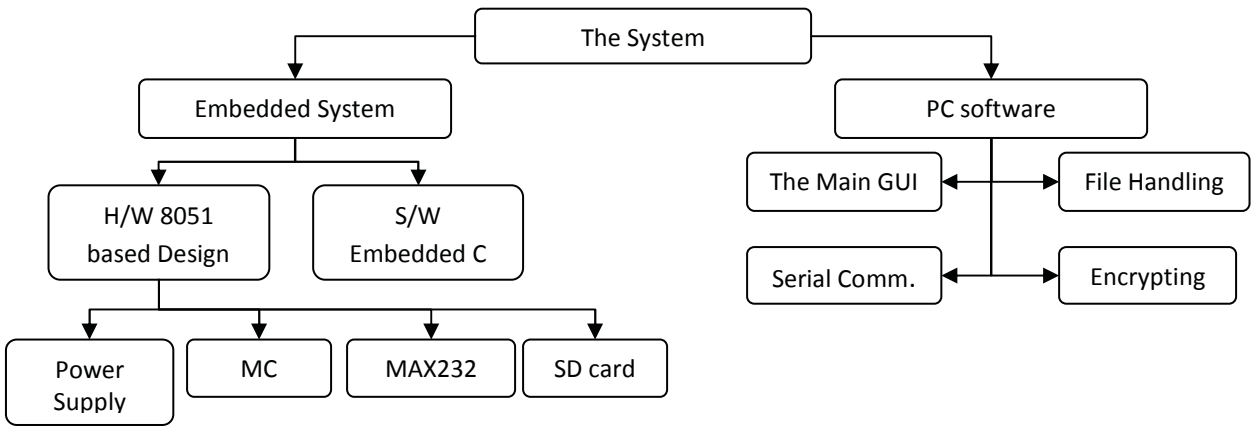
b) Drawback of Existing System

- We all know that transferring the Data through Internet is not full Proof or can be hacked.
- Data transfer by the mean of conventional hardware like pen drive, disk drives, CDs, DVDS etc can be accessed easily.

c) Proposed System

The proposed system will use SD/MMC cards for secured data storage. The system will be divided into two units viz. Hardware & Software. The Hardware will have a socket for inserting the SD/MMC card. It will be connected with the PC using serial port. The software will have the user interface for file or message storing. User will insert the card and will just enter the "Storing Password" and "Encryption Password". Then he/she can select a file to be stored or just type the desired message on the screen. After pressing the upload button it will send to the hardware which will store the information in the card. Now the data is secured and no one will retrieve it without the same hardware & software combination along with both the passwords. Again the information or file will not be visible by any operating system or card reader.

III. The Proposed System



Author α : Smt. Indira Gandhi College of Engineering Navi Mumbai, India.

a) Block Diagram

The block diagram of the system is attached behind.

b) Explanations of Block

The following are the brief explanation of the working principle of the various major block or sections used in the system…

- Power Supply

This unit will supply the various voltage requirements of each unit. This will be consist of transformer, rectifier, filter & regulator. The rectifier used here is bridge rectifier. It will convert 230VAC into desired 5V/12V DC.

- Microcontroller

This unit is the heart of the complete system. It is actually responsible for the all process being executed. It will monitor & control all the peripheral devices or component connected in the system. In short we can say that the complete intelligence of the project resides in the software code embedded in the microcontroller.

The controller here user will be of 8051 family. The code will be written in embedded C and will be burned or programmed into the code memory using a programmer. This unit requires +5V DC for its proper operation.

- MAX 232

This section will be used to convert TTL logic into RS232 logic and vice-versa. IN TTL--- logic 1 is +5V and logic 0 is 0V. In RS232---logic 1 is -10V & logic 0 is +10V. This unit will provide interface that is required to communicate microcontroller with RS232 based devices using serial communication link. The MAX232 IC is dedicated for the logic conversion. This unit is also called as a logic converter or a level converter. This unit requires +_5V DC for its proper operation.

- SD/MMC Card

This is the normal SD/MMC (Data Storage) card used in the mobile to store various type of data like text, Image, Videos etc. The microcontroller will store its data stream in its various blocks. This unit works on SPI (Standard Peripheral Interface) Protocol for its communication. It will be interfaced with microcontroller using 4 wire interface. This unit provide a huge amount of non-volatile memory the embedded system. This unit require +3.3VDC for it proper operation.

c) Features

The following are the prominent feature of the above discussed system…

- Two level of data protection i.e. hardware & software,
- Password Protected storage,
- Password based encryption,
- Data can be retrieved only with the same hardware software combination along with both passwords,
- No system can detect the existence of data on the SD/MMC card.
- No change in the blank space shown by the operating system – hence no one can predict if there is some information on card or not.

d) Technology & Programming Language

As microcontrollers are the core of these days digital circuit design in industry, this system uses it for the centralized operation & digital processing. The technology used here is embedded technology which is the future of today's modern electronics.

The following are the various programming languages & Technologies that are going to be used in the proposed system…

For embedded system…

- Embedded Technology,
- 8051 family Based controller,
- Embedded C- Keil Compiler,
- SPI Protocol for SD/MMC card interfacing,
- Eagle software for PCB Designing,

For PC system…

- VB.net 2008 Based Application software,
- File handling,
- Serial communication protocol,

e) Project development methodology or steps

The following will be development steps so as to achieve the working prototype model of the above proposed system…

- Defining the problem,
- Understanding the need & usability in industry and society(Market Analysis),
- Development Block Diagram,
- Designing circuit of individual blocks,
- Testing circuit in LAB & finalizing,
- Developing PCB on PC,
- Getting the PCB printed from market,
- Soldering the component,
- Performing the various basic experiment to test the PCBs,
- Developing flow chart for the entire process,
- Writing actual software program,
- Compilation and burning,
- Testing and Debugging,
- Development software for PC side software,
- Developing Data Flow Diagram,
- Writing actual code,

- Finally running the system and,
- Documentation

IV. Scope & Applications

Only the imagination can limit the application of the above proposed system.

Though the following are some example…

- Military sensitive data storage,
- Private information storage,
- As storage Media within a campus of college or company.
- Etc,

V. Conclusion

By the realization of the above proposed system one can learn many aspect of a digital electronics circuit. This will give the complete knowledge of designing microcontroller based system and developing embedded software. We will also learn the software development strategies and various programming techniques for pc based applications.

VI. Enhancement

a) Limitation

As generally all system have some limitation, here are some listed for the proposed system…

- Multiple data may lead corruption of previous data,
- Only SD/MMC cards can be used for storage,
- Large file can't be stored.

b) Drawbacks

This system has certain drawbacks also as listed.

- User serial port for interfacing
- Only text file can be stored,
- Speed of data transfer is slow.

c) Future Modification

There is always chance to improve the any system as research development is an endless process. Our system is no exception to this phenomenon. The following improvement can be done....

- USB can be used,
- Any type of file can be stored,
- Data transfer rate can be increased,
- Large file support can be integrated,
- Can be designed for a pen drive.

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Comparative Study of Bloom Filter Architectures

By Ritu Chhabra & Dr. Vandana Nath
Indra Gandhi Institute of Technology, IPU, Delhi

Abstract - Hardware based virus protection systems are required for identifying the malicious content and further removing it from network streams. Network Intrusion Detection System(NIDS) is needed to protect the end user machines from threats. An effective NIDS is therefore a network security system capable of protecting the end user machines well before a threat affects.NIDS requires a space efficient data base for detection of threats in high speed conditions. Bloom Filters are one of the security filters that consume significant power to detect and then filter out malicious content. A Bloom filter is a space efficient randomized data structure for representing a set in order to support membership queries. The aim of this paper is to compare the different architectures of Bloom filter like Standard Bloom filter, pipelined bloom filter, counting Bloom filter and parallel processing architecture of bloom filter in terms of their merits and demerits by using algorithmic & architectural techniques.

Keywords : *Bloom filters, network intrusion detection, universal hash function, FPR (False positive rate)*

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Comparative Study of Bloom Filter Architectures

Ritu Chhabra [α] & Dr. Vandana Nath [σ]

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I. Introduction

As the usage of portable devices continues to increase, more and more user applications catering to these device platforms are being developed. Also more often than not such devices are connected to one or more communications networks and must process a significant amount of incoming data. It is therefore becoming increasingly essential to secure these devices from malware of all kinds. The traditional approach for solving this problem on desktop computers is to provide for specialized antivirus software, firewall software and more recently anti-spyware software etc. However as opposed to a desktop computer the limited amount of computational power packed into a small footprint portable device precludes the use of resource intensive security software. It is therefore necessary to provide for alternate means to perform these functions on a small footprint device. Central to the ability to detect a malicious piece of code, a malicious packet in a data stream etc. is the ability to quickly determine if a given string of tokens belongs to a dictionary of known signatures. If we think of this dictionary of known signatures as a set, we have essentially reduced the problem of detecting malware to a problem of resolving set membership [1]. In this paper we give a recent survey on different types of bloom filter used for network Intrusion Detection system to benefit the research community to analyze and develop an efficient Bloom Filter which can have a prominent role in Network security, each having its own merits and demerits. The details of standard Bloom filter, pipelined Bloom filter, parallel processing bloom filter, counting Bloom filter is explained below. This paper also present the hardware architectures for the implementation of different Bloom filters. A Bloom Filter is a data structure that stores a given set of signatures by computing multiple hash functions on each member of the set and testing strings for membership of that set[3]. It acts as hardware antivirus device and connected with the CPU to remove the malicious input data. It consists of a set of hash functions, a hash function buffer to store hash results temporarily, a look up array to signify hash values and a decision component made of an AND to test the membership of testing string as shown in Fig.1.

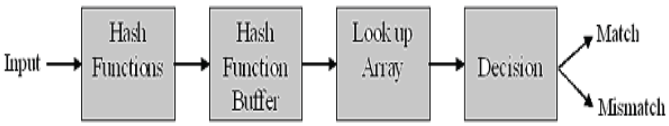

Fig.1 : Block Diagram

II. Standard Bloom Filter Architecture

Standard Bloom filter is an important and widely used tool for supporting efficient query services in networking because of its ability to represent a set of items by using a bit array with several independent hash function[6].Bloom filter provide an effective tool for saving the space when space is at a premium. For pattern matching Bloom filters are used. They are hashed based structures which have a certain degree of accuracy for considerable savings in memory. Two basic operations are defined for Bloom Filter. First is programming for programming the look up array using hash functions of strings in data set and second is testing for checking the membership of test string[2].

a) Programming

Bloom Filter represents the set of n-signatures $X = \{X_1, X_2, X_3 \ldots\ldots X_n\}$ in an m-bit array. The elements in this array are set to '0' before programming. Each signature is of b bits and is hashed k-times by independent hash functions $H_1, H_2, H_3 \ldots\ldots\ldots H_k$. It is assumed that each hash function maps uniformly to a random number in range $\{0, 1, 2\ldots\ldots m\text{-}1\}$ where m defines the number of bits in look up array as shown in Fig. 2. The random number describing hash function value indicates a bit location in m-bit look up array,

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which is then set to '1'. A particular bit location in *m*-bit look up array can be set to 1 more than once[2,3].

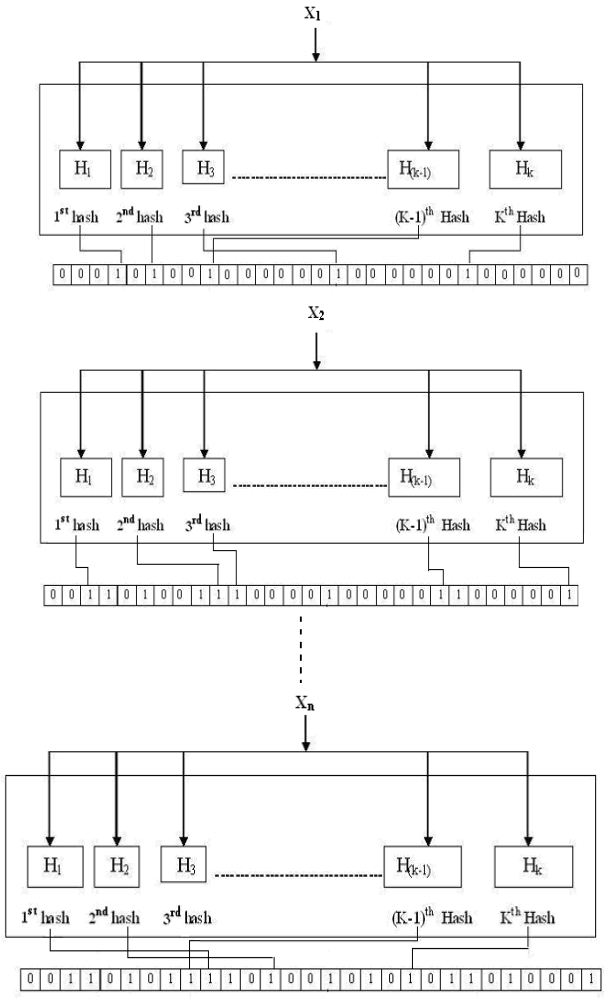

Fig. 2 : Programming of m-bit array in Bloom Filter

i. *Hash Function*

A class of universal hash functions described here found to be suitable for hardware implementation. Following is a description of how this hash matrix is calculated [2,3,7].

Given dataset of inputs $X = \{X_1, X_2, X_3 \ldots\ldots\ldots X_n\}$

Each input is of *b* bits $X_j = \{x_1, x_2, x_3 \ldots\ldots\ldots\ldots x_b\}$

*i*th hash function over string Xj is given in eqn. (2.1)

$$H_i(X_j) = d_{i1}.x_1 \wedge d_{i2}.x_2 \wedge \ldots\ldots\ldots\ldots\ldots \wedge d_{ib}.x_b \qquad (2.1)$$

$H_i(X_j)$ is the *i*th hash function of *j*th input string of input set

d_{ij} is a random coefficient ranging 1 to *m*

x_j's are the bits in particular input string

Where '.' is a bitwise AND operator, i.e.

$$d_{ij}.x_i = \begin{cases} d_{ij}, & if \quad x_i = 1 \\ 0, & otherwise \end{cases} \qquad (2.2)$$

'^' is a bitwise XOR operator.

Note that the hash value can be out of the range $[0 \ldots m-1]$ if m is not a power of 2. Hence, m must be a power of 2. Computation of a hash function is shown in Fig. 3

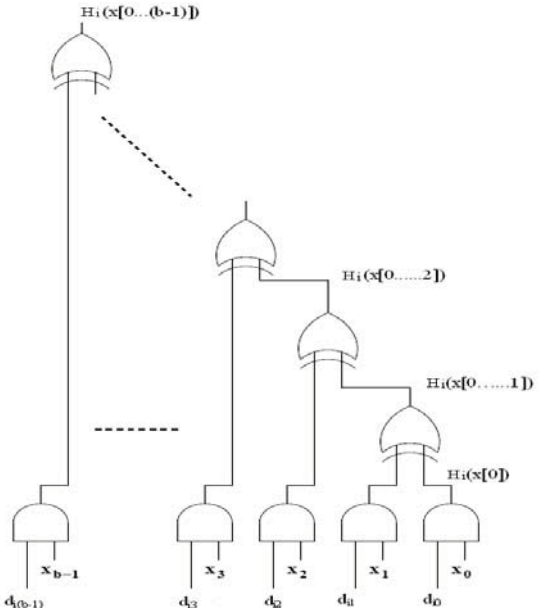

Fig. 3 : Computation of Hash Function

b) Testing

In testing phase a string is tested for membership of programmed Bloom Filter. The test string ts, is hashed *k*- times as before. If all the hash values point to the bit locations that are set to '1' then this indicates that test string may be member of the set with a certain probability (false positive probability) which is called as match. If any one of the hash values points to a bit location that is set to '0' then the test string is definitely not a member of the set and is called as mismatch. The testing phase of Bloom filter is shown in Fig 4.

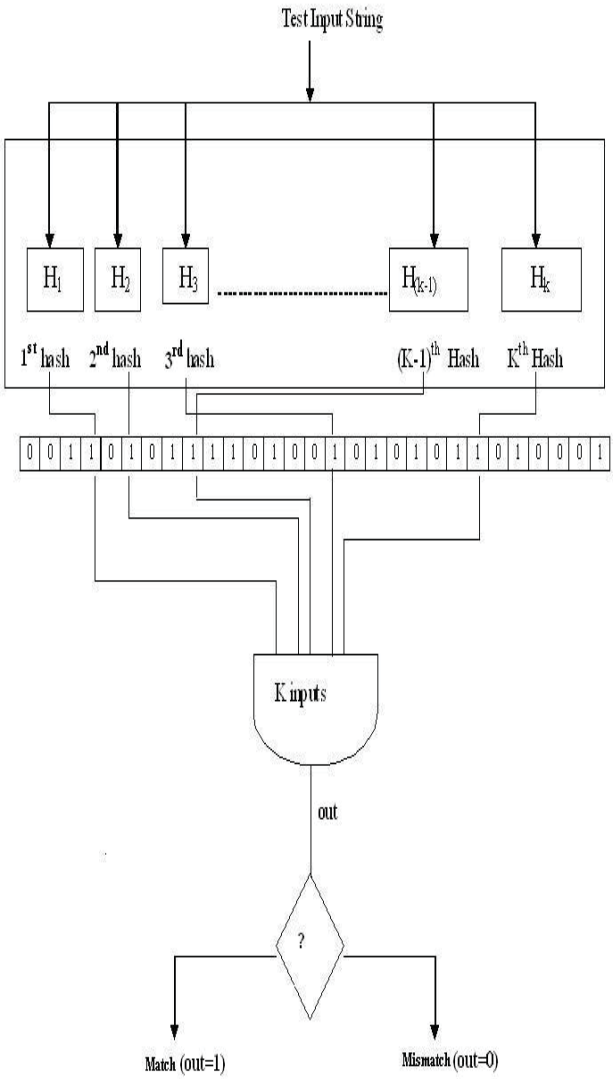

Fig.4 : Testing in Bloom Filter

III. Pipelined Bloom Filter

In some application such as network intrusion detection due to very low rate of malicious traffic there is no need to compute all the hash functions to get a result of non membership. To exploit this pipelined architecture is intruduced. Pipelined architecture of bloom filter consists of several group of hash function that are utilized in different stages.The first stage always compute the hash values. The second and further stages are used only if there is a match in the previous stage[3].

Advantage of Pipelined Bloom Filter

The advantage of using a pipelined Bloom filter is if the first stage pruduces a mismatch there is no need to use the second satge in order to decide whether the input string is a member of signature set because a bloom filter never pruduces a false nagatives. This saves the power consumed by pipelined bloom filter as compared to the standard bloom filter.

Draw Back of pipelined Bloom filter

Power saving ratio diminishes when there are high no of matches in the first stage and second stage is utilized more.To remove this problem we use fully pipelined architecture of Bloom filter[4].

a) Fully Pipelined Architecture of Bloom Filter

In fully pipelined Architecture number of stages equals to the number of hash functions .Each stage has only one hash function. Programming Phase is same as in case of regular Bloom Filter. In query phase, test string is progressed to next stage only when a previous hash function produces a match. Fully pipelined architecture of bloom filter is shown in fig 5.

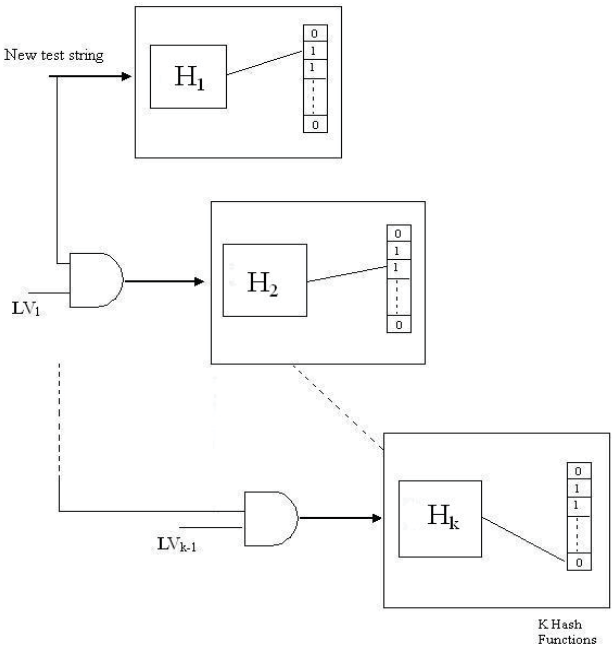

Fig.5 : Fully pipelined architecture of bloom Filter

Advantage of Fully pipelined Architecture

Pipelined architecture of bloom filter minimizes the false positive probability because first stage utilize more no of hash function increases the probability of mismatch thus second stage is not utilized but more no of hash function consume the more power which becomes the drawback of this architecture. Hence fully pipelined architecture remove this drawback as each of its stage has only one hash function. Fully pipelined architecture has the same no of hash function as the regular bloom filter hence its false positive probability is same as the regular bloom filter[3].

IV. Parallel Processing Architecture

A standard bloom filter architecture can effectively represent the items with a single attribute but it cannot support the representation and querying of items that have multiple attributes. To allow the operation on multi attribute items we proposed a simple structure called Parallel Bloom filter [5] .In this

architecture a number of testing strings inputs can be tested at the same time. Let test string inputs be ts_1, ts_2, ts_3……ts_L. Each test string is a b bit long .Hash values for all of the test strings are tested by checking particular bit locations in m bit look up array as in case of regular bloom filter. Bit location values in look up array are ANDED separately for different hash values of different test string. Parallel processing architecture of bloom filter is shown in fig 6.

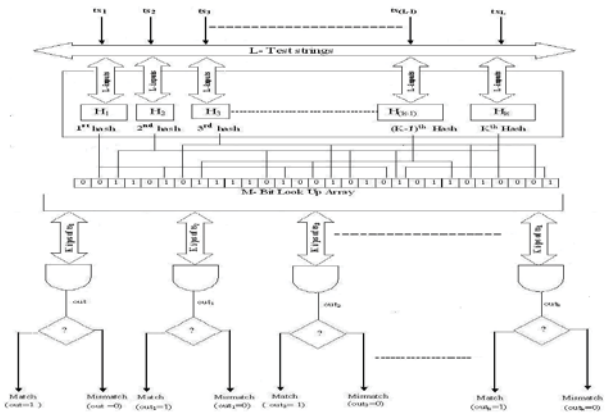

Fig. 6 : Parallel Processing Architecture

V. Counting Bloom Filter

One property of Bloom filter is that it is not possible to delete a member stored into the filter. Deleting a particular entry requires that the corresponding *k* hashed bits in the bit vector be set to zero. This could disturb other members programmed into the filter which hash to any of these bits. In order to solve this problem, the idea of the Counting Bloom Filters was proposed in. A Counting Bloom filter maintains a vector to counters corresponding to each bit in the bit-vector. Whenever a member is added to or deleted from the filter, the counters corresponding to the *k* hash values are incremented or decremented respectively. When a counter changes from 0 to 1, the corresponding bit in the bit-vector is cleared. It is important to note that the counters are changed only during addition and deletion of strings in a Bloom filter. For applications like network intrusion detection, these updates are relatively less frequent than the actual query process itself [6]. Architecture of counting bloom filter is shown in fig. 7

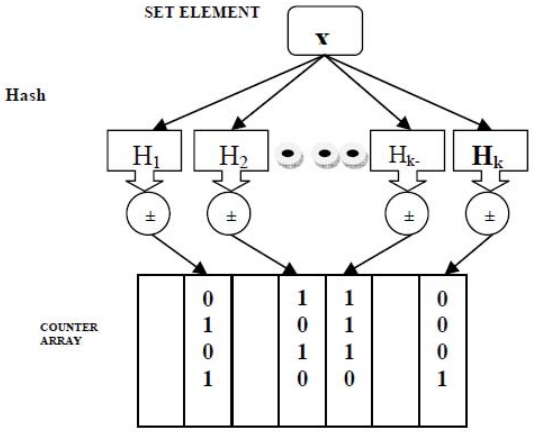

Fig.7 : Counting Bloom Filter

VI. Conclusion

A Bloom Filter can be used in variety of Network applications. Different architectures of Bloom filter have been described in terms of merits and demerits. Pipelined architecture of bloom filter minimizes the false positive probability because first stage utilize more number of hash function increases the probability of mismatch thus second stage is not utilized but more number of hash function consume the more power which becomes the drawback of this architecture. Hence fully pipelined architecture remove this drawback as each of its stage has only one hash function.counting bloom filter remove the problem of deleting a member stored in filter.

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3G Network Connectivity

By Madhurya Mudiar
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Abstract - 3G is the third generation of wireless technologies. It comes with enhancements over previous wireless technologies, like high-speed transmission, advanced multimedia access and global roaming. 3G is mostly used with mobile phones and handsets as a means to connect the phone to the Internet or other IP networks in order to make voice and video calls, to download and upload data and to surf the net. 3G phones commonly have two cameras since the technology allows the user to have video calls, for which a user-facing camera is required for capturing him/her. Unlike with Wi-Fi which you can get for free in hotspots, you need to be subscribed to a service provider to get 3G network connectivity. We often call this kind of service a data plan or network plan. Thus this paper not only aims to contribute to the already vast field of 3 G Network Connectivity in an effective manner to help but also summarizes.

GJRE-F Classification : FOR Code: 291799p

Strictly as per the compliance and regulations of:

3G Network Connectivity

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- Various Data Network
- 3G Overview
- IuCS Interface
- IuPS Interface
- DCN Interface
- Troubleshooting Guidelines

I. Introduction

a) *Various Data Networks*

RDN
Reliance Data Network

RIN
Reliance Internet Network

DCN
Data Communication Network

MEN
Metro Ethernet Network

b) *3G Functional Entities*

- Node B – Base Station
- UE – User Equipment
- RNC – Base Station Controller
- The Iu interface is an external interface that connects the RNC to the Core Network (CN).
- The Uu is also external, connecting the Node B with the User Equipment (UE).
- The Iub is an internal interface connecting the RNC with the Node B
- The Iur is an internal interface connecting two RNCs with each other.

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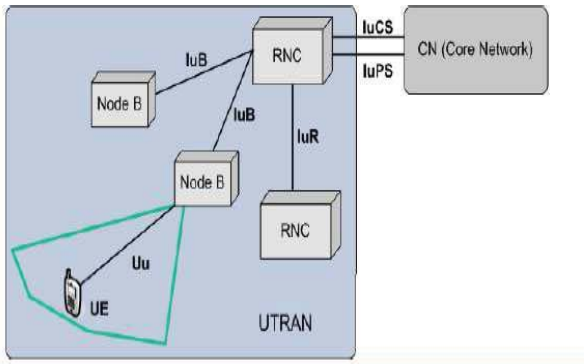
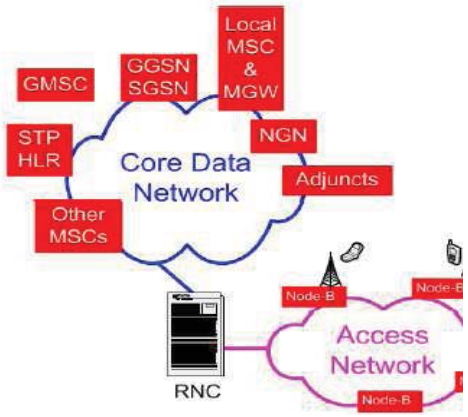
- Reliance MEN network is acting as a IP mobile backhaul Transport connectivity between IuB interface at RNC & NodeBs



II. 3G Overview

In a 3G Setup

- The NodeBs{BTSs (Base Transceiver Stations)} are connected on Access DataNetwork to the RNCs (RadioNetwork Controller)
- The RNCs Connect to 3G Core components (Like MSC /STP / HLR / SGSN/CGSN) on a Core Data Network



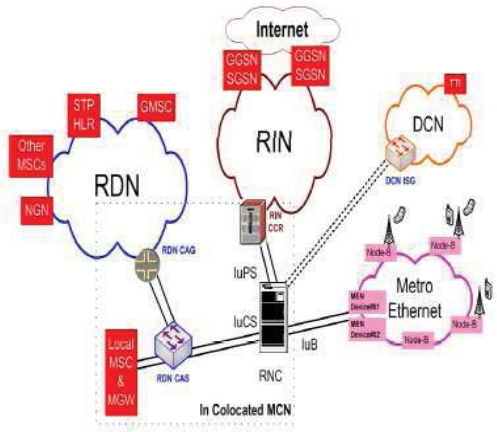
In a 3G Setup on the RNC Side

- The Interface from the RNC towards the Core voice infrastructure is called the IuCS Interface
- The IuCS talks to MSCs / STP / HLR etc for signaling purpose
- The IuCS talks to MGW (Media Gateway) for transmitting voice & video traffic

- The interface from RNC towards the Core Packet infrastructure is called the IuPS interface
- Through the IuPS interface the RNC talks to SGSN/CGSN
- The Interface from RNC to NodeB is the IuB Interface
- It carries both Voice + Video & Data on the same interface towards RNC from the NodeB devices
- There is separate management interface on RNC to give management information to centralized management infrastructure

Various traffic components on a 3G RNC are as under:

- The Voice Traffic (IuCS) flows on RDN
- The Packet data traffic (IuPS) flow on RIN
- The NodeB traffic comes to RNC on the MEN
- The Management traffic flows on DCN

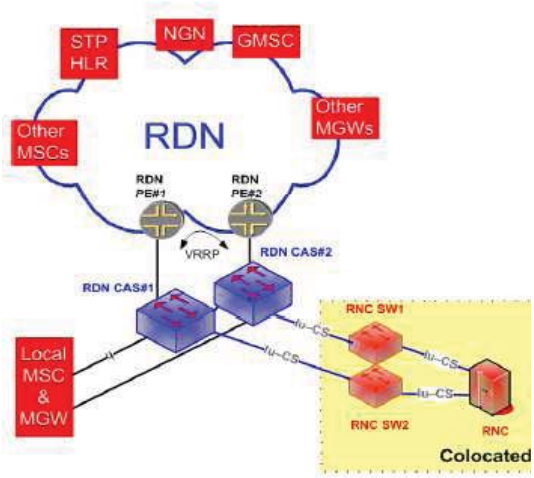


- Two RNC Vendor are selected
- Huawei for the RCOM Circles
- ZTE for the RTL Circle
- From the connectivity
- Architecture perspective there is no difference between two vendors
- There are total 45 RNC across 31 Locations
- RNC is connected to network through RNC Switches
- For HUW RNC the RNC Switch is Cisco 7606 / Cisco 3800
- For ZTE RNCs the Confidential Slide RNC Switch is Cisco 3750

III. IuCS Interface

a) *3G RNC : IuCS Traffic – Collocated Sites*

- The RNCs have dual IuCS interface towards the RNC switch
- For HUW RNC the interface is Optical Gig
- For ZTE RNC the interface is Electrical Gig
- The RNC Switch is a L3 Device
- It runs VRRP for redundancy towards RDN
- And also towards the IuCS ports of RNC
- It runs VRF instance for each traffic type i.e. IuCS –CP i.e. Signaling & IuCS – UP i.e. Bearer traffic (Voice + Video)
- The Uplinks from RNC Switches are terminated on the RDN CAS Switches in a redundant Fashion
- From the RDN CAS to RDN PE it goes on the existing connections
  - The VLANs from RNC to RDN PE are
  - Vlan 416 for Signaling i.e. IuCS - CP
  - Vlan 417 for Media i.e. IuCS - UP
  - Each instance has VRRP on RDN Confidential Slide
- This is applicable for RNC collocated in MCN where RDN presence is there



b) *3G RNC : IuCS Traffic – Non Collocated Sites*

- Wherever the RNC is not collocated with the RDN, the RNC is extended on the Transport Link as shown (e.g. Jamshedpur / Gwalior /Rourkela etc.)
  - Transport links (GEoSDH) are provisioned with 2CNO
  - As per the requirement appropriate VC4s are allocated on the Transport network
- Rest of the architecture is same as the collocated RNC
- The IuR is InterRNC traffic
  - Where all the RNCs are Collocated the IuR traffic doesnot flow on RDN, it gets switched on RNC Switch itself
  - Where all the RNCs are not collocated the IuR traffic gets switched through the RDN (e.g. Faridabad)

IV. IuPS Interface

a) *3G RNC : IuPS Traffic – Collocated Sites*

- The RNCs have dual IuPS interface towards the RNC switch

- For HUW RNC the interface is Optical Gig
- For ZTE RNC the interface is Electrical Gig

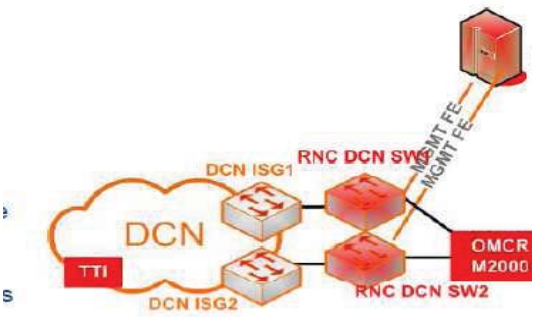
- The RNC Switch is a L3 Device
  - It runs VRRP for redundancy towards RIN
  - And also towards the IuPS ports of RNC
  - It runs one VRF instance forIuPS-CP (Signaling traffic) & IuPS-UP (Data Traffic)
- The Uplinks from RNC Switches are terminated on the RIN in a redundant Fashion
- The VLANs from RNC to RDN PE are
  - Vlan 464 for Signaling i.e. IuPS – CP & bearer traffic i.e. IuPS - UP
- Each instance has VRRP on RIN
- This is applicable for RNC collocated in MCN where RIN presence is there

b) 3G RNC : IuPS Traffic –Non Collocated Sites

- Wherever the RNC is not collocated with the RIN, the RNC is extended on the Transport Link as shown (e.g. Jamshedpur / Gwalior /Rourkela etc.)
  - Transport links GEoSDH are provisioned with 2CNO
  - Appropriate number of VC4s are provisioned as per the bandwidth requirement
- Rest of the architecture is same as the collocated RNC

c) 3G RNC : DCN Traffic –

- The RNCs have dual DCN interface towards the RNC DCN switch
  - For HUW RNC the interface is Electrical Gig
  - For ZTE RNC the interface is Electrical Gig
- The RNC DCN Switch is a L3 Device
  - It runs VRRP for redundancy towards DCN
  - And also towards the DCN ports of RNC
- The Uplinks from RNC DCN Switches are terminated on the DCN Switches in a redundant Fashion
- The RNC DCN Switch & DCN Switch runs VRRP protocol to give redundancy
- On the same RNC DCN Switch OMCR is connected
- At all RNC Locations Dual DCN Switches are present & functional



Redundancy & Fast Convergence

- Path redundancy - MSTP – BN Ring
- Fast convergence triggering mechanism such as VRRP with BFD is proposed to be implemented at RNC to MEN connecting interfaces.

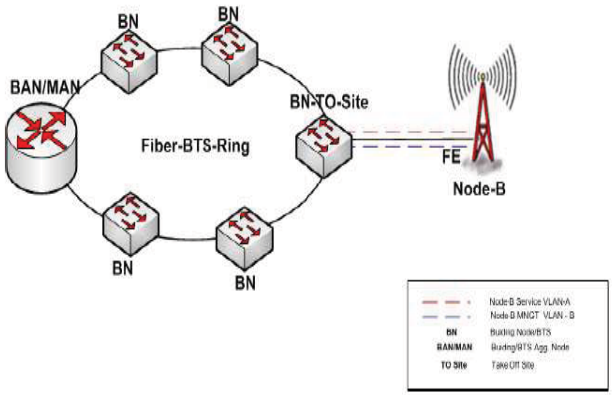
VLAN Assignments

- Management VLAN for Node-B
- Management Vlan for both Huawei and ZTE Node-Bs – VLAN 56
- Node-Bs under one BAN will be placed on a separate management VLAN (VLAN56).
- Management VLAN of Node-B to be passed start from the connecting interfaces of BN nodes till Parenting BAN in the corresponding ring.
- Service VLAN for Node-Bs
- Range of Service Vlan for both Huawei and ZTE Node-Bs – VLAN 1600 –1900
- Each Node-B under one BAN is assigned with separate VLAN for services and attached with the common service VRF created in the BAN.
- Service VLAN of Node-to be passed start from the connecting interfaces of BN nodes till Parenting BAN in the corresponding ring.

Scenario 1 BTS on fiber site

- Node-B Connectivity

- At fiber BTS site MEN NE will be available and it will be part of MEN Ring.
- To keep the FE-FE-14 identical architecture for 3G , Port Number FE 08 to FE are proposed (in case the proposed ports are in use, circle FA deploy team to assign new ports) for connecting the Node-B to MEN switch.
- These ports will be configured as a trunk port. By default Node-B management VLAN 56 will be allowed and service VLAN to be configured against the Node-B service SONode-B to RNC



Scenario Node-B Connectivity

- Node-B is connected behind 1st Hop SDH and

another Node-B connected behind 2nd Hop PDH card.

- For making connectivity from 1st Hop Node-B to Take-off site NE, it has been proposed to install the CX-200 at 1st Hop BTS location below SDH MW connecting to L1 card or IMAP card of SDH NE.
- To make this CX-200 RFS and to carry the Node-B service and Management traffic, bearer needs to be created between this CX-200 to take off site Scenario 3de-B Connectivity
- Two PDH HOP's are terminating on CX-200 installed at 1st Hop BTS location
- FA_DEPLOY_Circle team to give the correct Interface details of take-off site and respective Node-B service SOCo Scenario 4de-B Connectivity
- The IP Radio link terminating on Fiber BTS MEN NE
- Node B –will connect directly to IP Radio for 1st HOP and 2nd Hop Node-B will connect cardto PDH Ethernet card.
- The bearer to be provisioned in each Hop based on availability of bandwidth. In case of IP Radio the bandwidth required other than 2G BTS to be converted to IP radionne

Scenario 5Node-B Connectivity

- The IP Radio link will terminate on Fiber BTS MEN NE and Tail-End NEs are PDH MW
- Deployed CX-200D below IP radio for serving more than one PDH link
- IP Radio has 4 number of ethernet ports , In case of Ethernet port requirement is more than four then we are proposing to commission CX-200D below IP radioc
- Bandwidth Provisioning on NLD path BW to be provisioned in NLD path = (Number of BTS at Bauria x 2) + (Number of BTS in Kulgachia x 2) Mbps aBnWd wtoi dbet hp rPovriosivoniseido inn iMnigcrowave SDH
- 60Mbps on each hop, In case 60Mbps is not available, provisioining can be made based on available bandwidth, provided at least 2Mbps*no. of NodeBs downstream is available.
- BW to be provisioned in IP Radio & Microwave PDH
- Maximum Available Bandwidth (As per NPE-MW guideline IP Radio Port Mapping
- All the ports on IP Radio should be available for carrying traffic. No port should be reserved for CX-200 for OAM. For OAM,

NMS port is available on the IDU.

- Port No. 1 Towards take-off site
- Port No. 2 Towards Tail end
- Port No. 3 Towards Tail end
- Port No. 4 Node-B

V. Troubleshooting Guidelines

Following are the generic troubleshooting guidelines

- Check the physical cabling
- Check the indicators lights of connectivity are glowing at both the ends of the connectivity in subject
- If found ok, ask the RNC team to ping as per the required service
- If issues follow the detailed troubleshooting guidelines given below

a) Troubleshooting Guidelines – IuCS Traffic

- After ensuring Layer1 connectivity is OK, then Login into the RNC Switch & follow the below mentioned guidelines
- Ping the Local IuCS interfaces through appropriate VRF (1)
  - For IuCS-CP traffic it is signaling VRF
  - For IuCS-UP traffic it is Voice VRF
  - If not pinging check the local connectivity
  - If pinging & problem persisting move to following steps
- Ping the Local IuCS RDN interfaces through appropriate VRF (2)
  - If not pinging check the local connectivity
  - If pinging & problem persisting move to following steps
- Ping the End Devices (3)
  - If not pinging escalate to NOC
  - If Pinging the Network connectivity is through, the troubleshooting needs to start on the end devices

b) Troubleshooting Guidelines – IuPS Traffic

- After ensuring Layer1 connectivity is OK, then Login into the RNC Switch & follow the below mentioned guidelines
- Ping the Local IuPS interfaces through appropriate VRF (1)
  - not pinging check the local connectivity
  - If pinging & problem persisting move to following steps
- Ping the Local IuPS RIN interfaces through appropriate VRF (2)
  - If not pinging check the local connectivity
  - If pinging & problem persisting move to following steps 2
  - Ping the End Devices (3)
  - If not pinging escalate to NOC
  - If Pinging the Network connectivity is through, the troubleshooting needs to start on the end 1Devices

c) Troubleshooting Guidelines – DCN Traffic

- After ensuring Layer1 connectivity is OK, then Login into the RNC DCN Switch & follow the below mentioned guidelines
- Ping the Local DCN interfaces (1)
  - not pinging check the local connectivity
  - If pinging & problem persisting move to following steps
- Ping the Local DCN interfaces (2)
  - If not pinging check the local connectivity
  - If pinging & problem persisting move to following steps
- Ping the End Devices (3)
  - If not pinging escalate to NOC
  - If Pinging the Network connectivity is through, the troubleshooting needs to start on the end devices.

VI. Conclusion

Wireless technologies are a way for mobile users to make free or cheap calls worldwide and save a lot of money due to the latest telephony applications and services. 3G networks have the advantage of being available on the move, unlike Wi-Fi, which is limited to a few meters around the emitting router. So, a user with a 3G phone and a 3G data plan is well-equipped for making free mobile calls. She will only have to download one of the free applications and install on her mobile phone and start making calls

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Gate Level Design of a Digital Clock with Asynchronous-Synchronous Logic

By Sheikh Md. Rabiul Islam & Md. Jobayer Hossain
Khulna University of Engineering and Technology, Bangladesh

Abstract - A digital clock has been designed at gate level and is being presented in this paper. The clock architecture consists of three major blocks SECOND,MINUTE and HOUR. The architecture is the amalgam both of synchronous and asynchronous logic. All the flip-flops at each block run synchronously. The triggering operation of a block is asynchronous in nature. It serves the design requiring lower power consumption, provides lesser noise and electromagnetic interference, lower delay and greater throughput. The clock is designed at Xilinx System Generator, synthesized with Xilinx Synthesis Tool (XST) and Simulated by Vegilogger Pro 6.5.

Keywords : *Counter, asynchronous counter, synchronous counter, system level design, gate level design, GALS.*

GJRE-F Classification : *FOR Code: 090601*

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I. Introduction

A digital clock is a type of clock that displays the time digitally. Instead of the rotary mechanism of electromechanical clock, it uses digital counters that count second, minute and hours. Each sixty seconds make a minute and each sixty minutes an hour. After twenty four hours the clock resets and starts from initial condition. The functional unit of a digital clock is a counter that represents a second, minute or hour block. A counter [7] may be defined as a register i.e. a group of flip-flops that goes through a predetermined sequence of states upon the application of input pulses. The logic gates in a counter are connected in such a way as to produce a prescribed sequence of binary states in the register.

There are two types of input/output (I/O) synchronization technique to design a counter [10]: synchronous and asynchronous technique. In an asynchronous counter, the flip-flop output transition serves as a source for triggering other flip-flops. In otherwords, the CP inputs of all flip-flops (except the first) are triggered not only by the incoming pulses but rather by the transitions that occur in other flip-flops. The asynchronous counter is also referred to as overlapped counter. A problem [7] in designing an asynchronous logic is that it cannot be described by Boolean equations developed for describing clocked sequential circuits. Again as output of one flip-flop acts as the input of another one, the system designed at asynchronous logic faces considerable delay. On the other hand, a synchronous circuit [13] is a digital circuit in which the parts are synchronized by a single clock signal. In an ideal synchronous circuit, every change in the logical levels of its storage components is simultaneous. These transitions follow the level change of a special clock signal. Ideally, the input to each storage element has reached its final value before the next clock occurs, so the behavior of the whole circuit can be predicted exactly. Practically, some delay is required for each logical operation, resulting in a maximum speed at which each synchronous system can run [13]. Thus in a synchronous counter [7] all the flip-flops are clocked simultaneously. The decision whether a flip-flop is to be complemented or not is determined from the values of the T inputs at the time of pulse. If T=0, the flip-flop remains unchanged. If T=1, the flip flop complements. Thus the states of the counters get changed. Synchronous logic suffers from some disadvantages: As the clock is usually a high-frequency signal, this distribution consumes a relatively large amount of power and dissipates much heat. Even the flip-flops that are doing nothing consume a small amount of power, thereby generating waste heat in the chip [12]. Again the maximum possible clock rate is determined by the slowest logic path in the circuit, otherwise known as the critical path. This means that every logical calculation, from the simplest to the most complex, must complete in one clock cycle. In spite of these drawbacks synchronous counters are more suited for some reasons.

At an asynchronous counter [11], [14] the output of any flip-flop (except the first) depends solely upon the output of the previous T flip-flop. Due to the RC time delay at each transistor there occurs a large aggregation of delay time after several flip-flops [8]. So to design asynchronous counter is impractical. For this reason synchronous logic has been adopted to construct counter blocks. In addition to this the synchronous technique serves greater throughput and much lower overhead for its design simplicity [9].

In the way to integrated circuit implementation process way can notice two major steps [3]: Design stage and fabrication stage. Design stage includes system design, logic design and mask layout preparation. At the system level design [4] the architecture is checked against the system specification to ensure that all required hardware features and data paths have been included. At the next level of hierarchy, the architectural blocks are expanded into logic

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diagrams. In this stage the whole system is transferred into aggregation of registers [9]. Here each item represents a particular logic function. If that particular logic functions are represented by logic gates such as AND, OR or XOR, then it is called Gate level design [6]. Gate level design realizes intensive aggregation of elements at much lower area. To solve the problems associated both with synchronous and asynchronous logic the author adopted a recently emerged logic structure GALS [1], [2]. Globally Asynchronous Locally Synchronous logic is the amalgam of the two logics. It not only removes the drawbacks but also provides more advantages [16]. The advantages include lower power consumption and electromagnetic interferences.

II. Overview of the Architecture

The digital clock designed as shown in Fig.1 assumes three functional blocks: second, minute and hour. The second and minute block count from 0 to 59. So six T flip-flops are required to construct either second or minute block (2^6=64). The hour block counts from 0 to 23. So it requires five T flip-flops (2^5=32).

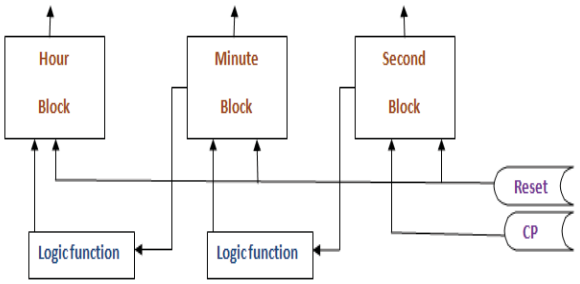

Fig.1 : simplified architecture of the design clock.

The flip-flops inside a block (second, minute or hour) run simultaneously as they are triggered by same clock pulse. But the clock pulse of minute block is a function of the outputs of the second block. Again the clock pulse of the hour block is also a function of the outputs of the minute block. So the block to block logical relation is asynchronous in nature. Thus the design architecture is a combination both of asynchronous and synchronous logic.

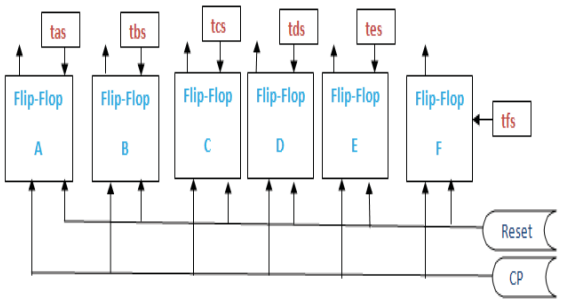

Fig.2 : Logic diagram of SECOND and MINUTE block

III. Model Development

There are three asynchronously operating blocks at the architectural design of the digital clock. But flip-flops at each block are energised synchronously. The SECOND and MINUTE block have six T flip-flops each. When they operate synchronously they are projected to have 64 distinct states. But we want them to go to their primary state after counting 60 states. So we need to modify the input and output relationships of flip-flops. Representing the input as Ta, Tb, Tc etc and A, B, C etc for flip-flops a, b, c respectively as shown in Fig.2, the relations for SECOND and MINUTE blocks are:

Ta=BCEF (A'D+AD')

Tb= ABCD'EF+CDEF (A'+B')

Tc =ABEFCD'+ DEF (A'+B'+C')

Td=EF (A'+C'+B')

Te= F (A'+B'+C'+D')

Tf =1

Similarly we want to make the flip-flops of HOUR block to go to its primary state after counting 24 states instead of 32 states. For this case the input-output relationships of the flip-flops are simplified as follows:

Ta= CDE (A'B+AB')

Tb=A'CDE

Tc=DE (A'+B')

Td=E (A'+B')

Te=1

Thus in the designed architecture sixty seconds make a minute and sixty minute an hour. After twenty four hour the clock resets and starts counting from initial states at another day. It is customary to keep a RESET button so that the user can reset the clock at any time.

IV. Operation

The individual block of the design is an aggregate of several synchronous binary counters. Therefore, the flip-flop in the lowest order position is complemented with every pulse. This means that its T input must be maintained at logic 1. A flip flop in any other position is complemented with a pulse provided all the bits in the lower order positions are equal to 1. As the input functions T's of the flip flops are configured, after the desired sequence (111011 for second and minute block) comes, all the outputs of the flip flops will be 0.

When the second block reaches to 59 (111011 in binary), all the flip flops of this second block resets. Then clock signal of minute block becomes 1. As Tfm =1 now logically, minute block state is increased by one at the next clock pulse. Thus each time second block faces state 111011, minute increases by one. The same thing occurs from minute to hour interaction. After

counting 23 hour (10111), 59 minute and 59 seconds all the flip-flops resets. As shown in Fig.3. Flow chart explaining the operation of digital clock.

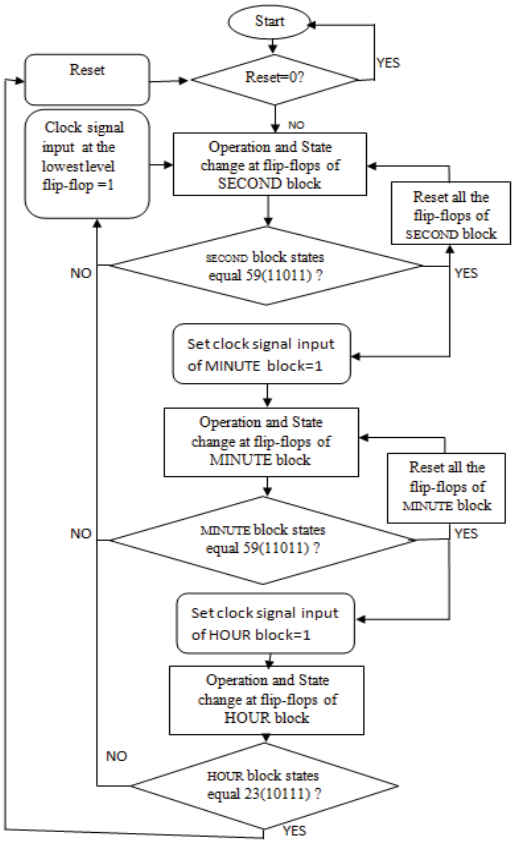

Fig.3 : Flowchart explaining the operation of digital clock.

V. Synthesis

The model is designed at Xilinx System Generator. Then it is synthesized with Xilinx Synthesis Tool (XST) as shown in Fig.4&5.

The outcomes include a IC package with two input ports: RESET and CLOCK PULSE and seventeen output ports. The RTL(Register Transfer Level) schematic of the design is provided as in Fig.6(a),(b),(c)&(d).It assembles logic gates which meet the systems requirements [6]. The details description of Pin numbers for the design of clock is given in Table.1.

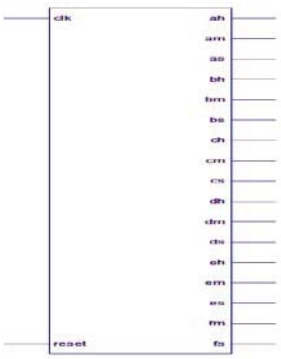

Fig.4 : RTL schematic diagrams found from XST (system level).

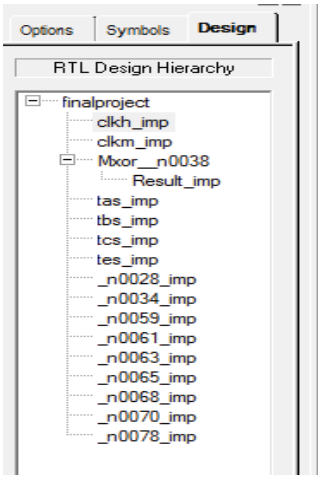

Fig. 6(a) : RTL Design hierarchy

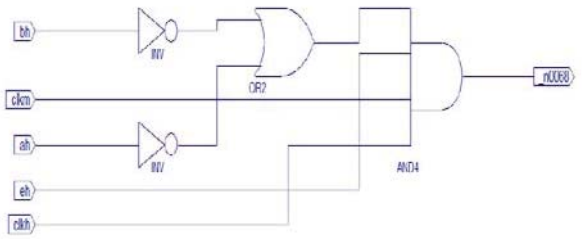

Fig. 6(b) : Gate level logic diagram showing net _n0068

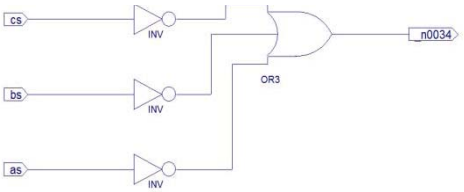

Fig.6(c) : Gate level representation of block FDRE.

Table.1 : Detail Description of the Pin Number Specification

Pin type	Pin name	Pin no.	Description	Function
Input	clk, reset	1,2	Single bit binary	clk is the line with input signal period=1second resets resets the clock to zero state
Output (Hour block)	ah,bh,ch, dh,eh	3,6,9,12, 15,	Single bit binary	Pins that jointly show time in hour
Output (Minute block)	am,bm,c m,dm, em,fm	4,7,10,13, 16,18	Single bit binary	Pins that jointly show time in minute
Output (Second block	as,bs,cs,d s,es,fs	5,8,11,14, 17,19	Single bit binary	Pins that jointly show time in second

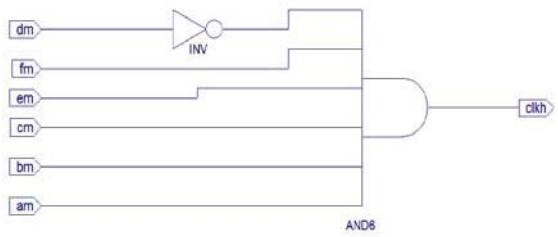

Fig.6(d) : Gate level logic diagram forming *clkh* signal.

A few portion of the total gate level representation is demonstrated in Fig.6(b), 6(c) and 6(d). It shows that all the components of the RTL schematic diagram are at gate level including AND, OR, INVERTER, XOR etc both at single and multiple inputs. The figure clearly demonstrates the interrelation among inputs and outputs.

VI. Simulation

The simulation of the design was run at verilolgger pro 6.5. The result was the exact replica of our expectation. From the timing diagram at Fig.7 we can notice that initially all the flip-flops are at initial state (zero state) when RESET is at state 0. The rest part of the circuitry remains inactive until RESET is at state 1. When RESET is at state 1 the flip-flops are allowed to follow counting. The state of SECOND block changes as 000000, 000001, 000010, 000011 and so on. When it reaches state 111011 (i.e. 59 in decimal), a clock pulse goes to MINUTE block and its state changes from 000000 to 000001 and the SECOND block starts counting again from 000000 state. Thus after 60 minutes when state 111011 appears at MINUTE block it resets and the state of HOUR block changes from 00000 to 00001. After counting 23 hour 59 minutes and 59 seconds, all the flip flops of the system get reseted (i.e. zero state) when the next clock pulse appears at the SECOND block.

VII. Limitations

The digital clock that is designed can count seconds, minutes and hours only. But at the real world people are not satisfied at this. They are interested in having notified other information such as date, month, year etc. It is also expected that the clock will serve some other facilities such as alarm, reminder etc. These features can be added just extending the design a little bit further. Again the design includes lesser number of gates. So it will be cost-inefficient to design on an entire chip. The author wishes to design a complete package of digital clock at the near future that will overcome the remaining drawbacks.

VIII. Conclusion

Logic gate level design of a digital clock has been presented. The design comprises the amalgam of synchronous and asynchronous techniques to attain its purpose. The Gate level design realizes intensive aggregation of components at smaller size of the chip. Again the combinational structure assumes lower power requirement, electromagnetic interference and greater throughput. The designed structure was synthesized using XST and simulated at verilogger pro 6.5. The design was successfully loaded at Xilinx FPGA device, MDA-ASIC2 (XC25150). In spite of having some limitations the design has been found to be useful enough.

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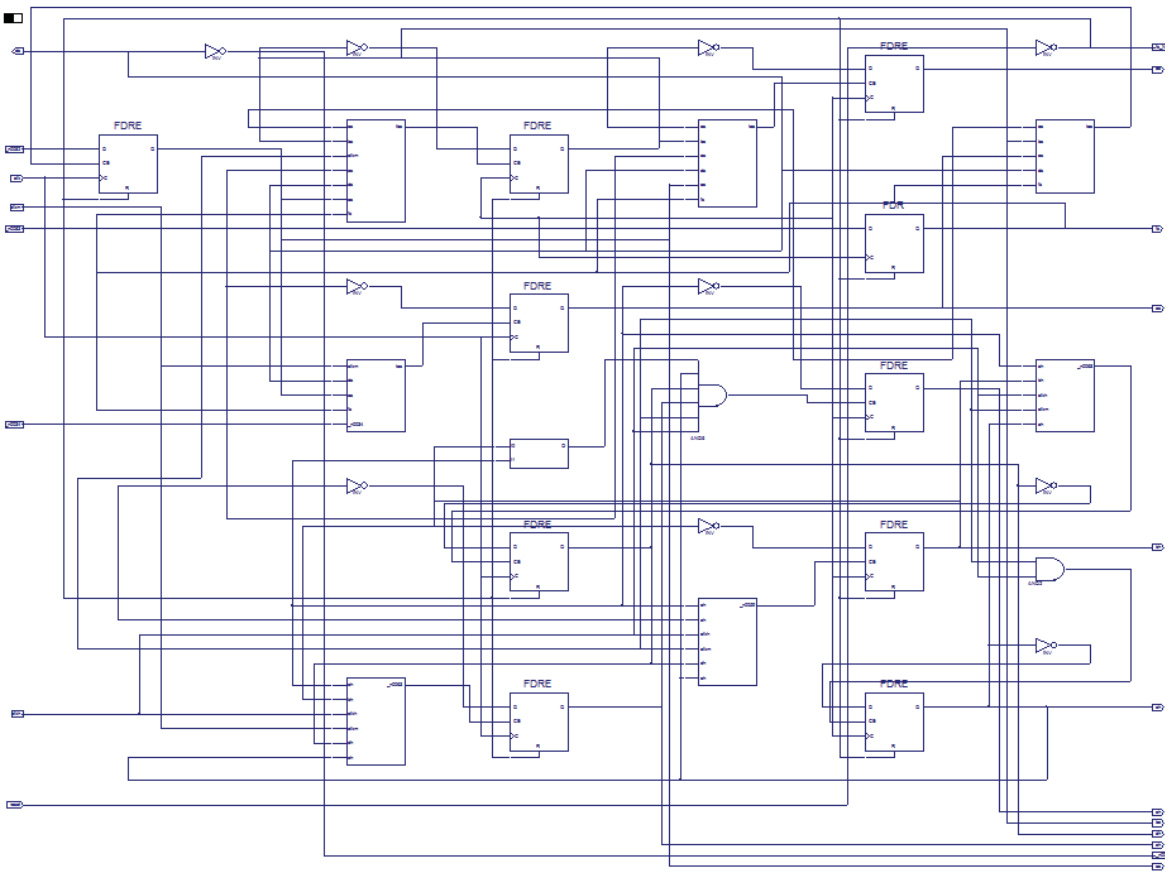

Fig.5 : RTL schematic diagrams found from XST (showing block level)

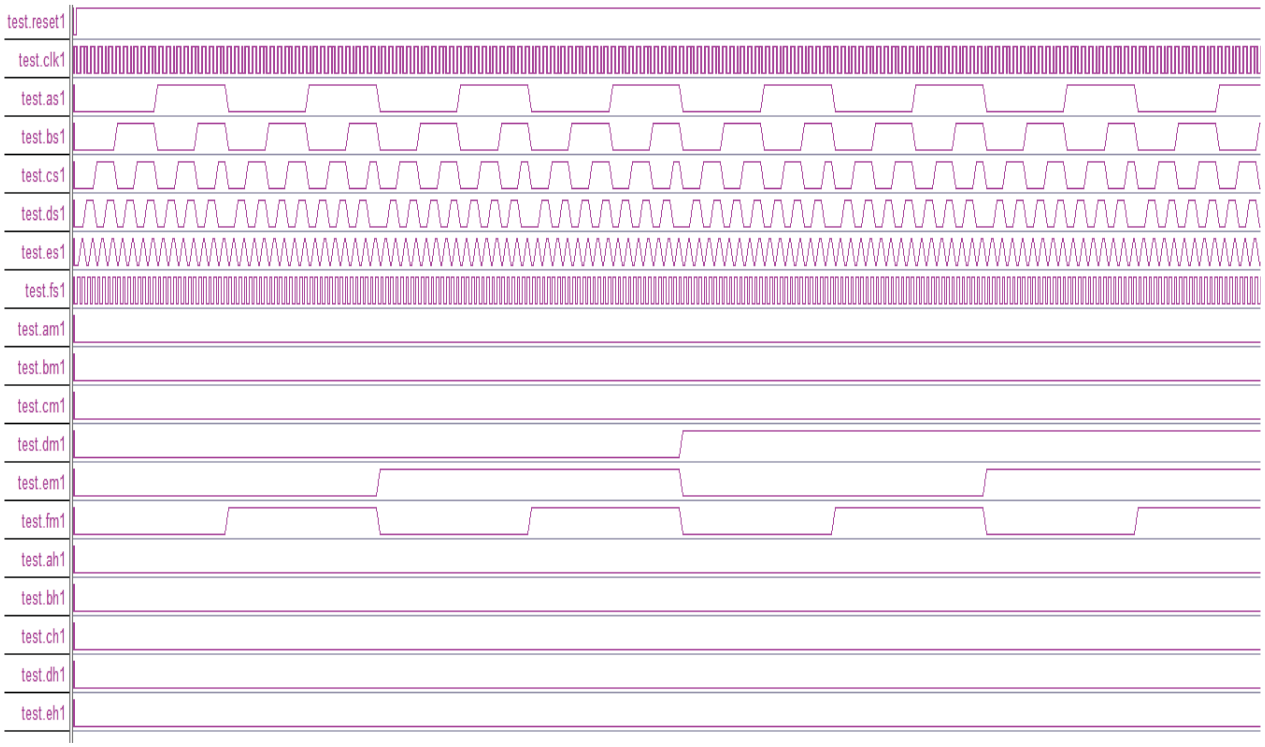

Fig.7 : Timing diagram simulated at Test bench.

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MRI Denoising Using Waveatom Shrinkage

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Abstract - It is well known that noise in Magnetic Resonance Image has a Rician distribution. Unlike additive Gaussian noise, Rician noise is signal dependent, and separating signal from noise is a difficult task. In this paper, a denoising technique is used in order to remove Rician noise from MRI using Waveatom shrinkage. De-noising by any shrinkage technique is highly sensitive to the threshold selection. Here to estimate the noise variance, histogram based technique is used and to calculate the shrinkage threshold a new technique is proposed. This method is applied to both simulated images and real images. Wave atom transform has been applied for different noise levels. This has been done in order to find more accurate results. A comparative analysis of wave atom and wavelet is also performed.

Keywords : *De-noising, Histogram, Magnetic Resonance Image, Rician Noise, Variance Estimation, WaveAtomTransform.*

GJRE-F Classification : *FOR Code: 109999*

Strictly as per the compliance and regulations of:

MRI Denoising Using Waveatom Shrinkage

Geetika Dua[α] & Varun Raj[σ]

Abstract - It is well known that noise in Magnetic Resonance Image has a Rician distribution. Unlike additive Gaussian noise, Rician noise is signal dependent, and separating signal from noise is a difficult task. In this paper, a denoising technique is used in order to remove Rician noise from MRI using Waveatom shrinkage. De-noising by any shrinkage technique is highly sensitive to the threshold selection. Here to estimate the noise variance, histogram based technique is used and to calculate the shrinkage threshold a new technique is proposed. This method is applied to both simulated images and real images. Wave atom transform has been applied for different noise levels. This has been done in order to find more accurate results. A comparative analysis of wave atom and wavelet is also performed.

Keywords : *De-noising, Histogram, Magnetic Resonance Image, Rician Noise, Variance Estimation, WaveAtomTransform.*

I. Introduction

Magnetic resonance imaging (MRI) is a medical imaging technique that measures the response of atomic nuclei of body tissues to high frequency radio waves when placed in a strong magnetic field and that produces images of the internal organs. Magnetic Resonance Imaging has proven to be particularly valuable for examination of the soft tissues in the body and is a commonly used form of medical imaging. Because of the resolution of MRI and the technology being essentially harmless it has emerged as the most accurate and desirable imaging technology. It was shown that pure noise in MR magnitude images could be modeled as a Rayleigh distribution. Afterwards, the Rician model was proposed as a more general model of noise in MR images. Sources of MR noise include thermal noise, inductive losses, sample resolution, and field-of-view. Despite significant improvements in recent years, magnetic resonance images often suffer from low SNR especially in cardiac and brain imaging. Therefore, noise reduction techniques are of great interest in MR imaging.

II. Related Work

The image processing literature presents a variety of de- noising methods. Many of the popular de-noising algorithms suggested are based on wavelet thresholding [1]–[4]. These approaches attempt to separate significant features from noise in the frequency domain and simultaneously preserve them while removing noise. If the wavelet transform is applied on MR magnitude data directly, both the wavelet and the scaling coefficients of a noisy MRI image become biased estimates of their noise-free counterparts. Therefore, it was suggested [2] that the application of the wavelet transform on squared MR magnitude image data would result in the wavelet coefficients no longer being biased estimates of their noise-free counterparts. Although the bias still remains in the scaling coefficients, it is not signal-dependent and can therefore be easily removed. The difficulty with wavelet or anisotropic diffusion algorithms is again the risk of over smoothing fine details particularly in low SNR images [5]. From these points, it is understood that all the algorithms have the drawback of over-smoothing fine details. In [6], stated that oscillatory functions or oriented textures have a significantly sparser expansion in wave atoms than in other fixed standard representations like Gabor filters, wavelets and curvelets. In [7], denoising using Wave Atom is done by estimating the noise variance by trial and error method. In [8], denoising using Wave Atom is done by estimating the noise variance by histogram technique.

III. Rician Noise

Magnetic resonance magnitude image data are usually modelled by the Rician distribution[9]. The magnetic resonance signals are acquired in quadrature channels. Each signal produces an image that is degraded by a zero-mean Gaussian noise of standard deviation as 0. The two images are then combined into a magnitude image and the Gaussian noise PDF is transformed into a Rician noise PDF. The joint probability density of the noise from two quadrature channels can be expressed as [10]:

$$p(n_r, n_i) = \frac{1}{2\pi\sigma_0^2}\exp\left(-\frac{n_r^2 + n_i^2}{2\pi\sigma_0^2}\right) \qquad (1)$$

The expectation values for the mean magnitude and the variance are[2]:

$$\mathrm{I} = \sigma_0\sqrt{\frac{\pi}{2}}\exp\left(-\frac{X^2}{4\sigma_0^2}\right)\times \left[\left(1+\frac{X^2}{2\sigma_0^2}\right)I_0\left(\frac{X^2}{4\sigma_0^2}\right)+\frac{X^2}{2\sigma_0^2}I_1\left(\frac{X^2}{4\sigma_0^2}\right)\right] \qquad (2)$$

$$\sigma_I^2 = X^2 + 2\sigma_0^2 - \frac{\pi\sigma_0^2}{2}\exp\left(\frac{X^2}{2\sigma_0^2}\right)\times$$

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$$\left[\left(1+\frac{X^2}{2\sigma_0^2}\right)I_0\left(\frac{X^2}{4\sigma_0^2}\right)+\frac{X^2}{2\sigma_0^2}I_1\left(\frac{X^2}{4\sigma_0^2}\right)\right]^2 \quad (3)$$

where I_0 and I_1 are modified Bessel functions of the first kind and X denotes the MR magnitude image.

IV. Waveatom Transform

Wavelet transform is a well known multiresolution analysis tool capable of conveying accurate temporal and spatial information. Wavelets better represent objects with point singularities in 1D and 2D space but fail to deal with singularities along curves in 2D. Therefore wavelet representation does not offer sufficient sparseness for image analysis. Following the introduction of wavelet transform, research community has witnessed intense efforts for development of wave atoms, ridgelets[11], contourlets[12] and curvelets[13]. These tools have better directional and decomposition capabilities than wavelets. Wave atoms have a sharp frequency localization that cannot be achieved using a filter bank based on wavelet packets and offer a significantly sparser expansion for oscillatory functions[14]. Wave atoms capture coherence of pattern across and along oscillations whereas curvelets capture coherence only along oscillations. To make our discussion concrete, we need to classify various wave-packet transforms as phase-space tilings. Since a complete collection must span all positions and frequencies, we see that wave packets are actually tiles in phase-space. We say a tiling is universal if it treats democratically all positions and orientations as shown in Figure 1.

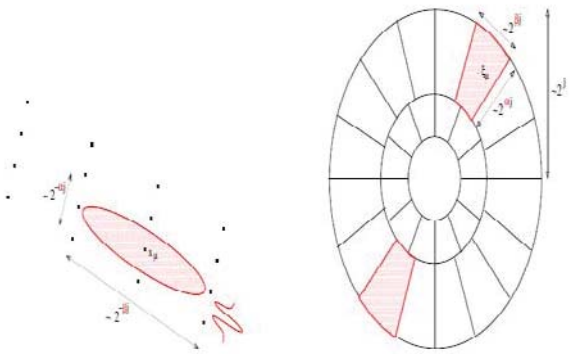

Figure 1 : Essential support of a wave packet with parameters (α,β), in space (left), and in frequency (right).

Two parameters should suffice to index a lot of known wave packet architectures: α to index whether the decomposition is multiscale (α = 1) or not (α = 0); and β to indicate whether basis elements are localized and poorly directional (β = 1) or, on the contrary, extended and fully directional (β = 0). Wave Atoms corresponds to $\alpha=\beta=1/2$, having an aspect ratio $\sim 2^{-j/2}\times 2^{-j/2}$ in space, with oscillations of wavelength$\sim 2^{-j}$ in the codirection ξ_μ.

Wave atoms are a variant of 2D wavelet packets which obey the parabolic scaling law: wavelength$\sim$(diameter)^2.

V. Experiments and Results

This section gives a detailed analysis of the proposed MRI de-noising algorithm. It compares and validates the performance of the proposed method using simulated and Real MR images and also compares the performance of the proposed method with Wavelet shrinkage.

Determination of threshold is very critical in this work. Input elements with absolute value greater than the set threshold value, are set to 1. In this work a new threshold is proposed which is better as compared to old threshold[15].

Old Threshold is given as:

$$\sqrt{\ln\left(\left(\max val\right)-\left(\min val\right)\right)}\sigma \quad (4)$$

New threshold is given as :

$$\sqrt{2*\ln\left(\left(\max val\right)-\left(\min val\right)\right)}\sigma \quad (5)$$

Where σ the noise variance, maxval is the highest pixel value in the image and the minval is the lowest pixel value in the image. Noise variance is estimated by the method Automatic estimation of the noise variance from the histogram of an MR image[16]. Output of thresholding is given by

$$x = (abs(y) > thld).* y). \quad (6)$$

After applying threshold criterion inverse Wave Atom transform and inverse Wavelet transform is applied separately and performance of both is compared using four comparison parameters.

Four comparison parameters mean square error (MSE), peak signal to noise ratio (PSNR), signal to mean square error (S/MSE) and signal to noise ration(SNR) are used which are defined as:

Mean square error (MSE) is given as

$$MSE=\frac{1}{m*n}\sum_{i=1}^{m}\sum_{j=1}^{n}\left(N(i,j)-DN(i,j)\right)^2 \quad (7)$$

Where m is number of rows in the image, N(i, j) is the noisy image and DN(i, j) is the de-noised image.

Peak Signal to Noise ratio (PSNR) is given as

$$PSNR=10\log 10\left(\frac{R^2}{MSE}\right) \quad (8)$$

Here R is the maximum fluctuation in the input image data type.

Signal to Noise ratio (SNR) is obtained by

$$SNR = 10\log 10\left(\frac{\mathrm{var}(x)}{\mathrm{var}(\hat{x}-x)}\right) \quad (10)$$

(Where x is noise free simulated images and $\hat{x}$ is the noisy image or de-noised images).

FOR STIMULATED IMAGES: For experiments with simulated images, images were loaded from Matlab software.

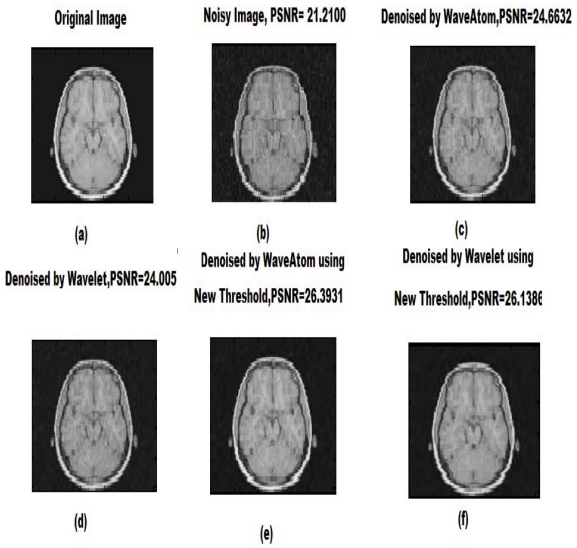

Figure.2 : (a) Stimulated Original Image (b) High Noise image (c) De-noised by Wave Atom with old threshold (d) De-noised by Wavelet with old threshold (e) De-noised by Wave Atom with new threshold (f) De-noised by Wavelet with new threshold.

Table 1 : Parameters for High Noise Image

Parameters	Denoised using Wave Atom with old threshold	Denoised using Wavelet with old threshold	Denoised using Wave Atom with new threshold	Denoised using Wavelet with new threshold
MSE(mean square error)	0.0034172	0.0036304	0.0022945	0.002433
PSNR(peak signal to noise ratio)	24.6632 dB	24.4005 dB	26.3931 dB	26.1386 dB
S/MSE(signal to mean square error)	17.0783 dB	16.8156 dB	18.8082 dB	18.5537 dB
SNR(signal to noise ratio)	12.4240 dB	12.0257 dB	15.2194 dB	14.6561 dB

Table 2 : Parameters for Low Noise Images

Parameters	Denoised using WaveAtom with old threshold	Denoised using Wavelet with old threshold	Denoised using WaveAtom with new threshold	Denoised using Wavelet with new threshold
MSE(mean square error)	3.5587e-005	3.8718e-005	3.3665e-005	3.5996e-005
PSNR(peak signal to noise ratio)	44.4871 dB	44.1208 dB	44.7282 dB	44.4375 dB
S/MSE(signal to mean square error)	36.9022 dB	36.5359 dB	37.1433 dB	36.8526 dB
SNR(signal to noise ratio)	30.6408 dB	30.1310 dB	30.7152 dB	30.1635 dB

FOR REAL IMAGES: The real images were down loaded from the Open Acess Series of imaging Studies (OASIS) database[17].

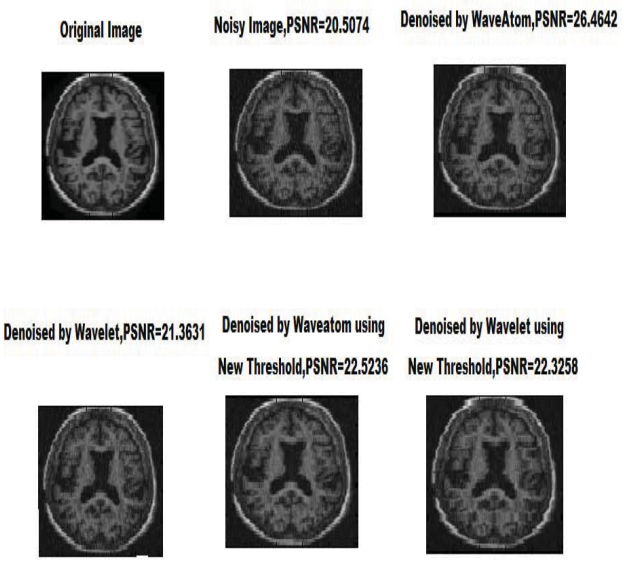

Figure.3 : (a) Real Original Image (b) High Noise image (c) De-noised by Wave Atom with old threshold (d) De-noised by Wavelet with old threshold (e) De-noised by Wave Atom with new threshold (f) De-noised by Wavelet with new threshold.

Table 3 : Parameters for High SNR Images

Parameters	Denoised using Wave Atom with old threshold	Denoised using Wavelet with old threshold	Denoised using Wave Atom with new threshold	Denoised using Wavelet with new threshold
MSE(mean square error)	0.0027496	0.0028503	0.0019821	0.0021131
PSNR(peak signal to noise ratio)	25.6072 dB	25.451 dB	27.0287 dB	26.7508 dB
S/MSE(signal to mean square error)	14.3304 dB	14.1742 dB	15.7519 dB	15.4739 dB
SNR(signal to noise ratio)	10.2556 dB	10.0420 dB	12.2912 dB	11.8558 dB

Table 4 : Parameters for Low Noise Image

Parameters	Denoised using WaveAtom with old threshold	Denoised using Wavelet with old threshold	Denoised using WaveAtom with new threshold	Denoised using Wavelet with new threshold
MSE(mean square error)	0.0071381	0.0073061	0.0055929	0.0058536
PSNR(peak signal to noise ratio)	21.4642 dB	21.3631 dB	22.5236 dB	22.3258 dB
S/MSE(signal to mean square error)	10.1873 dB	10.0863 dB	11.2468 dB	11.0489 dB
SNR(signal to noise ratio)	6.3210 dB	6.1699 dB	7.8936 dB	7.5525 dB

It is clear from table 1 and 2,3and 4 that de-noised image using wave atom with new threshold has lowest mean square error (MSE), highest peak signal to noise ratio (PSNR), highest signal to mean square error (S/MSE) and highest signal to noise ratio (SNR). It is also clear from the table that quality parameters of image de-noised by wave atom is better as comparison to the quality parameters of image de-noised by wavelet.

VI. Conclusion

It have been concluded that noise removal on MRI by the proposed new threshold gives better results as compared to the old threshold. Also it is clear that wave atom transform gives better results as comparison to wavelet transform. Results are verified by taking Stimulated MRI images and Real images downloaded from Open Access Series of imaging Studies database. Four comparison parameters are taken which are: MSE, PSNR, S/MSE, and SNR. Comparison is shown in the form of tables in which wave atom transform provides lower mean square error (MSE), higher peak signal to noise ratio (PSNR), higher signal to mean square error (S/MSE) and higher signal to noise ratio (SNR) as comparison to wavelet transform.

VII. Future Scope

The field of image processing has been growing at a very fast pace. The day to day emerging technology requires more and more revolution and evolution in the image processing field. The work proposed in this paper also portrays a small contribution in this regard. This work can be further enhanced to de-noise the other type of images, like CT, Ultrasound, X ray images. It will provide a good add on to the already existing denoising techniques. Moreover, for future work we can train our algorithm using various techniques like fuzzy logic or neural network, in order to attain the best output without performing calculations for each and every combination.

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The Design and Construction of a low cost Propeller Led Display

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Abstract - This paper explains the project which is a special kind of circular LED display. With the help some mechanical assembly, LED count, hardware requirement, and hence overall cost is cut to very affordable price. Also, maintenance and repairing of the display is so easy, that anyone having a little electronics knowledge can take care of this. All the synchronizing can be implemented through software. First of its kind, made using the 20-pin 8051 series microcontroller, this project use the principle of Space Multiplexing. This propeller display is mechanically scanned and displays the characters in digital format. Made from scrap it can be used anywhere and everywhere and the most amazing fact about this display is its crystal clear display. This display consists of just 7 bright LEDs which are rotated to show the display. For building this project, requirement is just a small 20 pin microcontroller, a position encoder, and LEDs. This display can show the messages, which will require a whopping 525 LEDs. So hardware and cost minimization is achieved.

Keywords : *Propeller; Persistence of Vision; Space Multiplexing.*

GJRE-F Classification : *090606, 090601, 090699*

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The Design and Construction of a low Cost Propeller Led Display

Sheikh Rafik Manihar [α], Mr. Komal Prasad Dewangan [σ] & Mr. Ajay Kumar Dansena [σ]

Abstract - This paper explains the project which is a special kind of circular LED display. With the help some mechanical assembly, LED count, hardware requirement, and hence overall cost is cut to very affordable price. Also, maintenance and repairing of the display is so easy, that anyone having a little electronics knowledge can take care of this. All the synchronizing can be implemented through software. First of its kind, made using the 20-pin 8051 series microcontroller, this project use the principle of Space Multiplexing. This propeller display is mechanically scanned and displays the characters in digital format. Made from scrap it can be used anywhere and everywhere and the most amazing fact about this display is its crystal clear display. This display consists of just 7 bright LEDs which are rotated to show the display. For building this project, requirement is just a small 20 pin microcontroller, a position encoder, and LEDs. This display can show the messages, which will require a whopping 525 LEDs. So hardware and cost minimization is achieved.

Keywords : Propeller; Persistence of Vision; Space Multiplexing.

I. Introduction

Propeller is a term associated with a circular rotating object. As this project needs to rotate whole circuit assembly, there must be some prime mover attached to it. So, the term 'Propeller'. This project using bright light emitting diodes for displaying the characters and symbols on its assembly. That's why this project is named as 'PROPELLER LED DISPLAY. ' This is the phenomenon which is related to vision capability of human eye by which an afterimage is thought to persist for approximately 1/25th of a second. So, if someone is observing the images at a rate of 25 images per second, then they appear to be continuous. The best example of this property is the red circle we observe when we rotate the firecracker or incense stick in circle. This project was started with a simple principle which is frequently encountered in our everyday life, which is Persistence of Vision. This phenomenon makes one feel fast moving/changing objects to appear continuous. A television is a common example; in which image is re-scanned every 25 times, thereby appear continuous. Further, a glowing objects if rotated in a circle at fast speed, it shows a continuous circle. By modifying this basic idea, 7 LEDs can be rotated in a circle, showing 7 concentric circles. But if these LEDs are switched at precise intervals, a steady display pattern can be shown. Existing systems do employ POV principle, but for displaying each pixel, individual LED is used. This results in a huge number of LEDs even for small sized displays.

By using a propeller type display, LED count can be kept to a bare minimum. Even 7 LEDs can perform a task of over 525 LEDs.Applications can find their way into cost effective solutions for large public displays, information systems. It can directly replace Railway station information displays, bus stands and many more places.

II. Methodology

a) Hardware Description

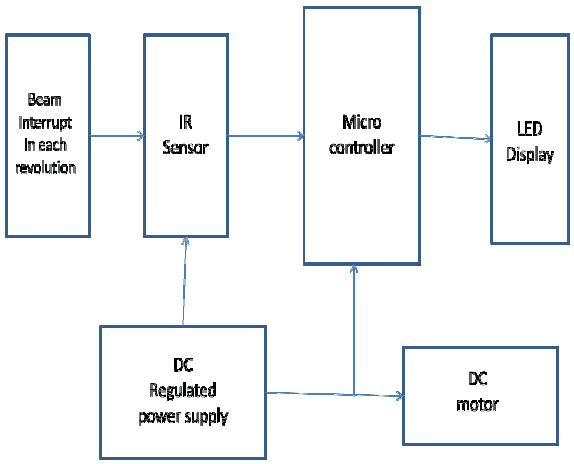

Figure1 : Block Diagram

In this section we will emphasize on detailed overview of each of the block shown in above block diagram. In every description of the block respective schematics and working is explained. The propeller display consists of following blocks, as shown in the block diagram.

- Microcontroller AT89C2051

This project is based around the microcontroller AT89C2051, which is a derivative of 8051 family, from Atmel Inc. This is a 20 pin IC packaged in DIP package. This small sized IC is used, mainly because of its reduced weight. This improves the performance of the display, because reduced weight gives advantage of increased RPM.

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- Led Module

LED module consisting of 7 bright LED is fixed in another side of the arm of our project. These LEDs are connected with each of the port pin of microcontroller, with a series current limiting resistor of 470 ohm.

- DC Motor

Repeated scanning of the display is must for continuous vision. This task is achieved using circular rotation of the whole circuit assembly. So, we used a DC motor as the prime mover.

- Interrupter Module

Interrupter module is our sensor module, consisting of the IR interrupt sensor MOC7811, from Motorola Inc. This sensor was selected from a variety of other alternatives, because of its small size, precise interrupt sensing, and study casing. One great advantage of using this module is, interfacing it with the microcontroller is just a matter of two resistors and a general purpose transistor. Following is the complete circuit diagram of our interrupter module. MOC7811 is the sensing part of the interrupter module, while rest of the circuitry works as signal conditioning ckt. 3 wires emerge out from the module, respectively Vcc, Signal and Ground. Output of the module is LOW, if interrupt occurs, otherwise it remains HIGH. It consists of IR LED and Photodiode mounted facing each other enclosed in plastic body. When light emitted by the IR LED is blocked because of some completely opaque object, logic level of the photo diode changes. This change in the logic level can be sensed by the microcontroller or by discrete hardware.

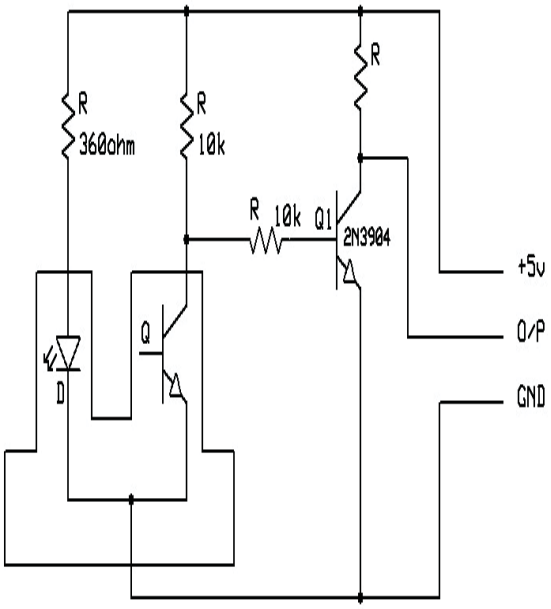


Figure1 : Circuit Diagram of Interrupter Module

- Mechanical Assembly

Mechanical assembly plays a vital role in proper functioning of this project. The display is scanned each time, by rotating the whole assembly in a circular path. The basic idea we developed is on our own, by implementing and modifying different ways to do this. Following diagram shows the most reliable way, that we finally selected. Here, one major challenge was how to bring +5V supply to the spinning circuit. We tried the same by adopting twothree different methods, but finally concluded on the method, as shown in the figure. As seen in the diagram, one supply connection (GND) is provided through the motor's shaft. Other terminal (Vcc) is connected, by arranging a friction disc-brush arrangement. The brush keeps its contact with the disc, so that current can be supplied. Most critical objective was to achieve pristine balance and overall good mechanical strength. For weight adjustment, we have provided one long screw, and weight can be attached or removed by adding / removing metallic bolts. If the assembly is balanced perfect, then it can achieve stability, and rotate at high RPMs too. This will improve the overall efficiency of this display

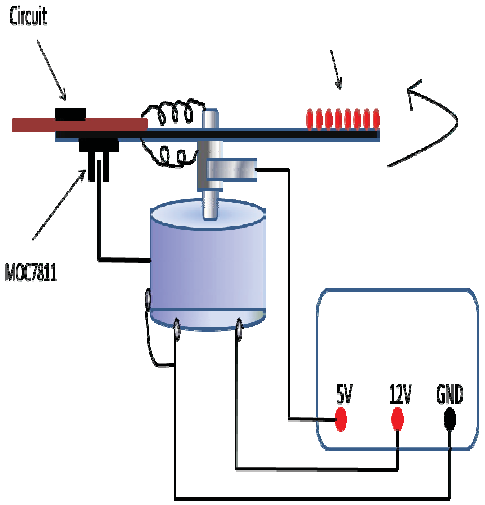


Figure3 : Mechanical Assembly

- DC Power Supply

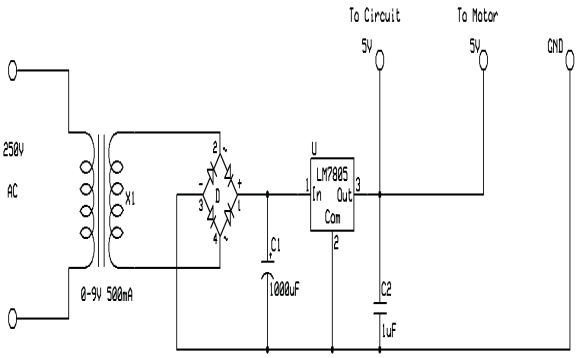


Figure2 : circuit Diagram of Power Supply.

A fixed voltage power supply producing constant +5V consists of step down transformer, a bridge rectifier, filter capacitors C1 and 3 terminal regulator IC LM7805. A step down transformer is selected in such a way that it produces 9V at the input of IC. This power supply is capable of supplying +5v and load current up to 500m A. The capacitor C2 connected between output terminal and ground cancels out any inductive effect due to long distribution leads. Input capacitor C1 is used to improve transient response of the regulator IC, i.e. response of regulator to sudden changes in load. It is also helpful in reducing the noise present in the output. Dropout voltage (Vin-Vout) needs to be at least 2V under all operating conditions for proper operation of regulator.

b) Software Description

- Ride IDE

The Resonance 8051 Development Kits are a complete solution for creating software for the 8051 family of microcontrollers. The Development Kits comprise many different tools that allow projects ranging from simple to highly complex to be developed with relative ease. You will find that with the Resonance Development Kits you can rely on tools that have been tested by real users over a long period of time. Ride provides a familiarity to the tools that will provided a basis for using more complex features. It is assumed that the user is familiar with Windows and has at least some familiarity with the 8051 microcontroller family and the C programming language.

- Algorithm

i. *Main routine*

1. Load proper value in IE register, so that the interrupts INT0 and T0 are enabled. (IE = 83H)
2. Offer higher priority to the INT0 (External) interrupt. (IP = 01H)
3. Configure timer 1 as 16-bit timer, and timer 0 as 8-bit auto reload mode timer. (TMOD = 12H)
4. INT0 should be configured as edge interrupt. (IT0 = 1)
5. Configure port 3 as input port. (P3 = 0FFH)
6. Move input string to the video RAM area. (call 'ramc' function)
7. Start the timers.
8. Initiate an infinite loop.

ii. *Interrupt Routines*

a. External Interrupt

1. Stop the timers.
2. Move th1 and tl1 into convenient registers.
3. Divide this 16 bit value by our total number of segments.
4. Subtract the answer from 256, and load the result in th0.
5. Now, reset the video RAM pointer and character segment pointers to their initial respective positions.
6. Start the timers
7. Return from interrupt

b. Timer 0 Interrupt

1. Call the display routine.
2. Clear timer overflows flag.
3. Return from interrupt

III. Result

- Interrupt Module Testing

This Interrupter module testing is required for detecting exact position of wheel on which whole circuit assembly is mounted. Supply voltage given to Pin. No. 1(Collector) and Pin.No.3 (Anode) of MOC7811=5.5V Output voltage obtained at Pin.No.1 of MOC 7811 without interrupt=5.21v.Output voltage obtained at Pin.No.1 of MOC7811 with interrupt=0.08V

- DC Motor RPM Testing

DC Motor used in this project is 12 V dc motor which is tested by using digital contact-less tachometer. Arrangement was made so that the sensing circuit gives high to low pulse for each completion of revolution. By measuring the time difference between two successive pulses RPS can be calculated which further provide RPM value, as shown below:

Power supply given to DC Motor = 9V

Time interval between two successive pulses as seen on CRO = 30.4ms

- RPS = 1 / (30.4ms) =32.89
- RPS = 33
- RPM= 33x60=1980

- Power Supply Module Testing

Power supply module was designed to provide 5V DC power supply necessary to drive both motor and circuit. AC input is given from 9V 750mA transformer. Results are as follows.

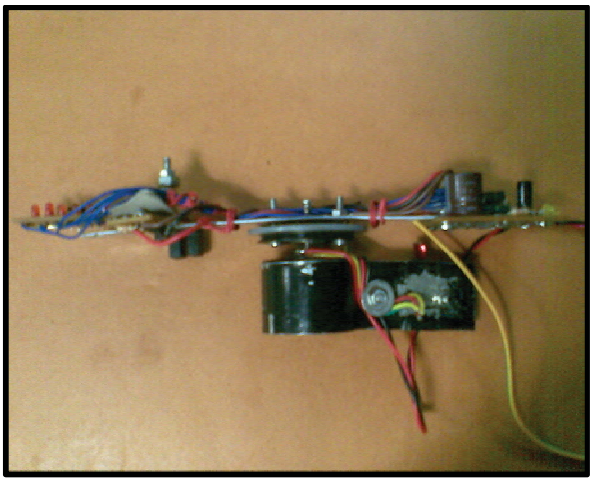
Input voltage, Vs=9V AC.

Output voltage observed, Vo = 4.92V DC

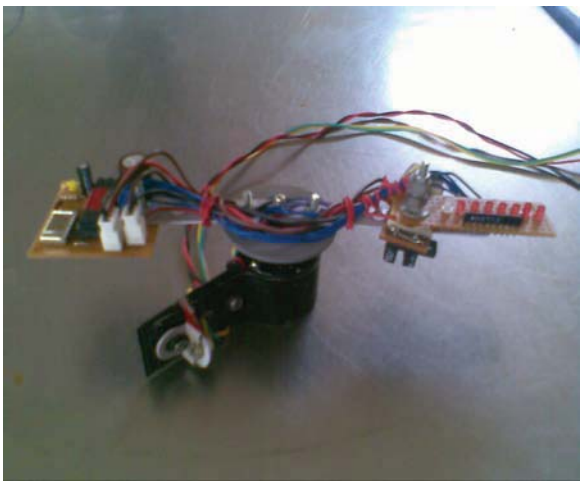
- Display Generated Pattern

Displaying a Quarter circle

Displaying a Half Circle



Displaying a character string



Displaying a number string

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- One should start brainstorming lists of possible keywords before even begin searching. Think about the most important concepts related to research work. Ask, "What words would a source have to include to be truly valuable in research paper?" Then consider synonyms for the important words.
- It may take the discovery of only one relevant paper to let steer in the right keyword direction because in most databases, the keywords under which a research paper is abstracted are listed with the paper.
- One should avoid outdated words.

Keywords are the key that opens a door to research work sources. Keyword searching is an art in which researcher's skills are bound to improve with experience and time.

Numerical Methods: Numerical methods used should be clear and, where appropriate, supported by references.

Acknowledgements: Please make these as concise as possible.

References

References follow the Harvard scheme of referencing. References in the text should cite the authors' names followed by the time of their publication, unless there are three or more authors when simply the first author's name is quoted followed by et al. unpublished work has to only be cited where necessary, and only in the text. Copies of references in press in other journals have to be supplied with submitted typescripts. It is necessary that all citations and references be carefully checked before submission, as mistakes or omissions will cause delays.

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The Editorial Board and Global Journals Inc. (US) recommend that, citation of online-published papers and other material should be done via a DOI (digital object identifier). If an author cites anything, which does not have a DOI, they run the risk of the cited material not being noticeable.

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Tables: Tables should be few in number, cautiously designed, uncrowned, and include only essential data. Each must have an Arabic number, e.g. Table 4, a self-explanatory caption and be on a separate sheet. Vertical lines should not be used.

Figures: Figures are supposed to be submitted as separate files. Always take in a citation in the text for each figure using Arabic numbers, e.g. Fig. 4. Artwork must be submitted online in electronic form by e-mailing them.

Preparation of Electronic Figures for Publication

Even though low quality images are sufficient for review purposes, print publication requires high quality images to prevent the final product being blurred or fuzzy. Submit (or e-mail) EPS (line art) or TIFF (halftone/photographs) files only. MS PowerPoint and Word Graphics are unsuitable for printed pictures. Do not use pixel-oriented software. Scans (TIFF only) should have a resolution of at least 350 dpi (halftone) or 700 to 1100 dpi (line drawings) in relation to the imitation size. Please give the data for figures in black and white or submit a Color Work Agreement Form. EPS files must be saved with fonts embedded (and with a TIFF preview, if possible).

For scanned images, the scanning resolution (at final image size) ought to be as follows to ensure good reproduction: line art: >650 dpi; halftones (including gel photographs) : >350 dpi; figures containing both halftone and line images: >650 dpi.

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Figure Legends: Self-explanatory legends of all figures should be incorporated separately under the heading 'Legends to Figures'. In the full-text online edition of the journal, figure legends may possibly be truncated in abbreviated links to the full screen version. Therefore, the first 100 characters of any legend should notify the reader, about the key aspects of the figure.

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the search? Will I be able to find all information in this field area? If the answer of these types of questions will be "Yes" then you can choose that topic. In most of the cases, you may have to conduct the surveys and have to visit several places because this field is related to Computer Science and Information Technology. Also, you may have to do a lot of work to find all rise and falls regarding the various data of that subject. Sometimes, detailed information plays a vital role, instead of short information.

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21. Arrangement of information: Each section of the main body should start with an opening sentence and there should be a changeover at the end of the section. Give only valid and powerful arguments to your topic. You may also maintain your arguments with records.

22. Never start in last minute: Always start at right time and give enough time to research work. Leaving everything to the last minute will degrade your paper and spoil your work.

23. Multitasking in research is not good: Doing several things at the same time proves bad habit in case of research activity. Research is an area, where everything has a particular time slot. Divide your research work in parts and do particular part in particular time slot.

24. Never copy others' work: Never copy others' work and give it your name because if evaluator has seen it anywhere you will be in trouble.

25. Take proper rest and food: No matter how many hours you spend for your research activity, if you are not taking care of your health then all your efforts will be in vain. For a quality research, study is must, and this can be done by taking proper rest and food.

26. Go for seminars: Attend seminars if the topic is relevant to your research area. Utilize all your resources.

27. Refresh your mind after intervals: Try to give rest to your mind by listening to soft music or by sleeping in intervals. This will also improve your memory.

28. Make colleagues: Always try to make colleagues. No matter how sharper or intelligent you are, if you make colleagues you can have several ideas, which will be helpful for your research.

29. **Think technically:** Always think technically. If anything happens, then search its reasons, its benefits, and demerits.

30. Think and then print: When you will go to print your paper, notice that tables are not be split, headings are not detached from their descriptions, and page sequence is maintained.

31. Adding unnecessary information: Do not add unnecessary information, like, I have used MS Excel to draw graph. Do not add irrelevant and inappropriate material. These all will create superfluous. Foreign terminology and phrases are not apropos. One should NEVER take a broad view. Analogy in script is like feathers on a snake. Not at all use a large word when a very small one would be

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33. Report concluded results: Use concluded results. From raw data, filter the results and then conclude your studies based on measurements and observations taken. Significant figures and appropriate number of decimal places should be used. Parenthetical remarks are prohibitive. Proofread carefully at final stage. In the end give outline to your arguments. Spot out perspectives of further study of this subject. Justify your conclusion by at the bottom of them with sufficient justifications and examples.

34. After conclusion: Once you have concluded your research, the next most important step is to present your findings. Presentation is extremely important as it is the definite medium though which your research is going to be in print to the rest of the crowd. Care should be taken to categorize your thoughts well and present them in a logical and neat manner. A good quality research paper format is essential because it serves to highlight your research paper and bring to light all necessary aspects in your research.

Informal Guidelines of Research Paper Writing

Key points to remember:

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- Write your paper in the form, which is presented in the guidelines using the template.
- Please note the criterion for grading the final paper by peer-reviewers.

Final Points:

A purpose of organizing a research paper is to let people to interpret your effort selectively. The journal requires the following sections, submitted in the order listed, each section to start on a new page.

The introduction will be compiled from reference matter and will reflect the design processes or outline of basis that direct you to make study. As you will carry out the process of study, the method and process section will be constructed as like that. The result segment will show related statistics in nearly sequential order and will direct the reviewers next to the similar intellectual paths throughout the data that you took to carry out your study. The discussion section will provide understanding of the data and projections as to the implication of the results. The use of good quality references all through the paper will give the effort trustworthiness by representing an alertness of prior workings.

Writing a research paper is not an easy job no matter how trouble-free the actual research or concept. Practice, excellent preparation, and controlled record keeping are the only means to make straightforward the progression.

General style:

Specific editorial column necessities for compliance of a manuscript will always take over from directions in these general guidelines.

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Mistakes to evade

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· Keep on paying attention on the research topic of the paper

· Use paragraphs to split each significant point (excluding for the abstract)

· Align the primary line of each section

· Present your points in sound order

· Use present tense to report well accepted

· Use past tense to describe specific results

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· Shun use of extra pictures - include only those figures essential to presenting results

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The summary should be two hundred words or less. It should briefly and clearly explain the key findings reported in the manuscript--must have precise statistics. It should not have abnormal acronyms or abbreviations. It should be logical in itself. Shun citing references at this point.

An abstract is a brief distinct paragraph summary of finished work or work in development. In a minute or less a reviewer can be taught the foundation behind the study, common approach to the problem, relevant results, and significant conclusions or new questions.

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shortening the outcome. Sum up the study, with the subsequent elements in any summary. Try to maintain the initial two items to no more than one ruling each.

- Reason of the study - theory, overall issue, purpose
- Fundamental goal
- To the point depiction of the research
- Consequences, including definite statistics - if the consequences are quantitative in nature, account quantitative data; results of any numerical analysis should be reported
- Significant conclusions or questions that track from the research(es)

Approach:

- Single section, and succinct
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- A conceptual should situate on its own, and not submit to any other part of the paper such as a form or table
- Center on shortening results - bound background information to a verdict or two, if completely necessary
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- Explain the value (significance) of the study
- Shield the model - why did you employ this particular system or method? What is its compensation? You strength remark on its appropriateness from a abstract point of vision as well as point out sensible reasons for using it.
- Present a justification. Status your particular theory (es) or aim(s), and describe the logic that led you to choose them.
- Very for a short time explain the tentative propose and how it skilled the declared objectives.

Approach:

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- Explain materials individually only if the study is so complex that it saves liberty this way.
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- Do not take in frequently found.
- If use of a definite type of tools.
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- Simplify - details how procedures were completed not how they were exclusively performed on a particular day.
- If well known procedures were used, account the procedure by name, possibly with reference, and that's all.

Approach:

- It is embarrassed or not possible to use vigorous voice when documenting methods with no using first person, which would focus the reviewer's interest on the researcher rather than the job. As a result when script up the methods most authors use third person passive voice.
- Use standard style in this and in every other part of the paper - avoid familiar lists, and use full sentences.

What to keep away from

- Resources and methods are not a set of information.
- Skip all descriptive information and surroundings - save it for the argument.
- Leave out information that is immaterial to a third party.

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The principle of a results segment is to present and demonstrate your conclusion. Create this part a entirely objective details of the outcome, and save all understanding for the discussion.

The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

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- Sum up your conclusion in text and demonstrate them, if suitable, with figures and tables.
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- Present a background, such as by describing the question that was addressed by creation an exacting study.
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Approach

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Topics	Grades		
	A-B	**C-D**	**E-F**
Abstract	Clear and concise with appropriate content, Correct format. 200 words or below	Unclear summary and no specific data, Incorrect form Above 200 words	No specific data with ambiguous information Above 250 words
Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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