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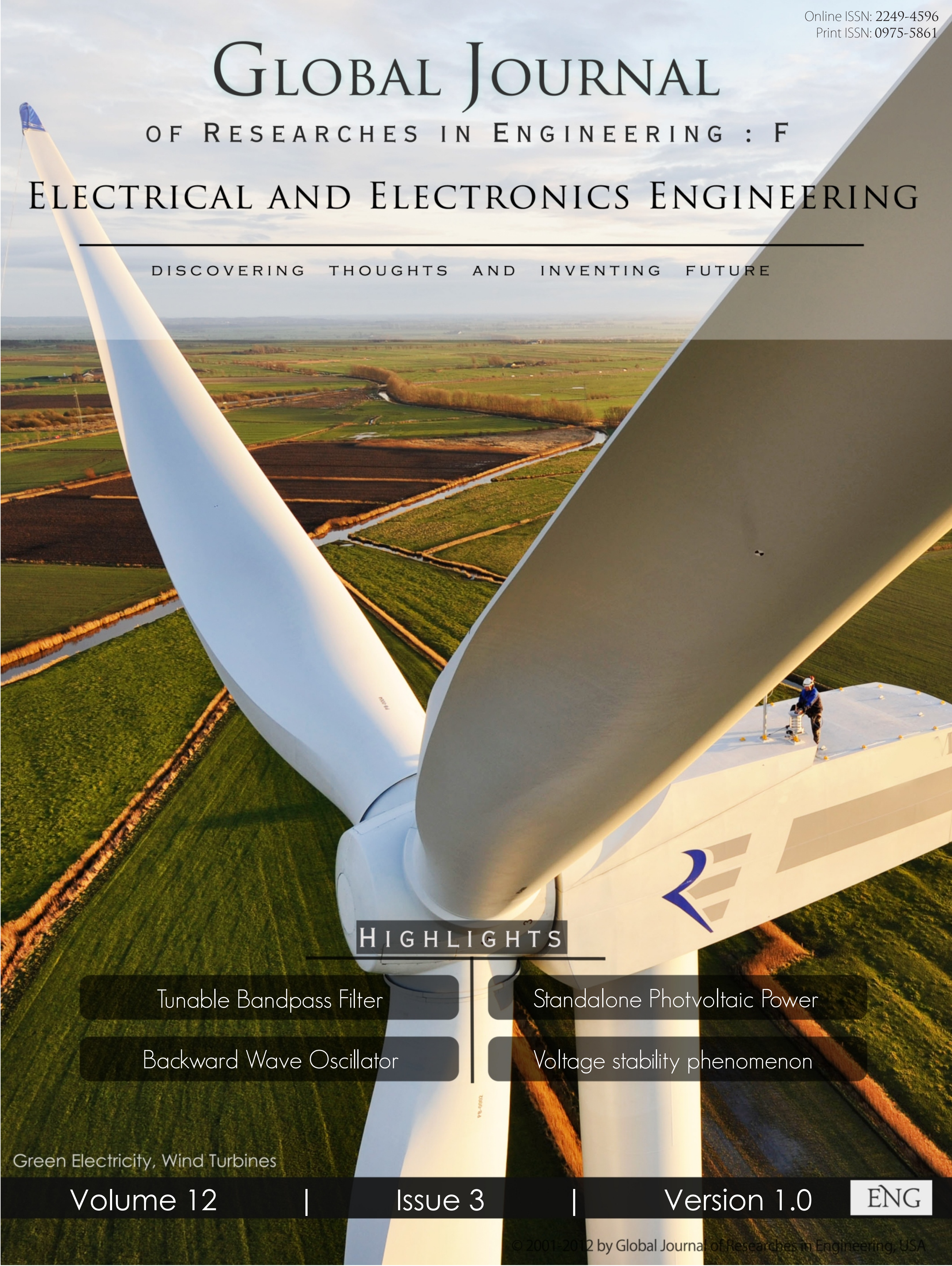
DISCOVERING THOUGHTS AND INVENTING FUTURE



Green Electricity, Wind Turbines

HIGHLIGHTS

- Tunable Bandpass Filter
- Standalone Photvoltaic Power
- Backward Wave Oscillator
- Voltage stability phenomenon

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RF Phase Shifter Using Coupled Microstrip Square Rings Tunable Bandpass Filter

By L. Bousbia, M. Ould-Elhassen, M. Mabrouk, A. Ghazel & Ph. Benech

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Abstract - This paper presents a study, optimization and simulation of tunable bandpass filter centered at 2.4GHz and used as phase shifter based on coupled microstrip square ring loaded by varactor diodes. We have performed an electromagnetic simulation on Momentum software of ADSTM; we have used the power of the Momentum software for the optimization and simulation of our circuit. A good results were obtained; the filter results in an insertion loss of 0.35 dB−0.26 dB over tuning range and 3−dB bandwidth of 300MHz−360MHz. We compute a fractional bandwidth between 13% and 14.5% for our circuit and for different value of capacitance. We compute also a good dynamic range of phase shifting about 90° at operating frequency 2.4GHz for different value of capacitance.

Keywords : Bandpass filter, Square ring, Phase shifter, Microstrip line, Varactor diode, Coupled line, RF engineering.

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RF PHASE SHIFTER USING COUPLED MICROSTRIP SQUARE RINGS TUNABLE BANDPASS FILTER

RF Phase Shifter Using Coupled Microstrip Square Rings Tunable Bandpass Filter

L. Bousbia[α], M. Ould-Elhassen[σ], M. Mabrouk[ρ], A. Ghazel[ω] & Ph. Benech[¥]

Abstract - This paper presents a study, optimization and simulation of tunable bandpass filter centered at 2.4GHz and used as phase shifter based on coupled microstrip square ring loaded by varactor diodes. We have performed an electromagnetic simulation on Momentum software of ADS™; we have used the power of the Momentum software for the optimization and simulation of our circuit. A good results were obtained; the filter results in an insertion loss of 0.35 dB–0.26 dB over tuning range and 3–dB bandwidth of 300MHz–360MHz. We compute a fractional bandwidth between 13% and 14.5% for our circuit and for different value of capacitance. We compute also a good dynamic range of phase shifting about 90° at operating frequency 2.4GHz for different value of capacitance.

Keywords : Bandpass filter, Square ring, Phase shifter, Microstrip line, Varactor diode, Coupled line, RF engineering.

I. INTRODUCTION

For almost three decades, tunable filters have been a popular choice to adapt multiple RF bands of operation using a single filter [1]. As consequence, tunable filter can replace the necessity of switching between several filters to have more than one filter response by introducing tuning elements embedded into a filter topology. Depending on type of tuning element, tunable filters can be classified in two categories with discrete and continuous tuning [2]. In this case we interest on continuous tuning device more precisely on varactor diodes, the use of this type of diode as capacitors has been the most popular choice to modify the effective electrical length of the resonator and tune the center frequency of the passband.

The coupling is carefully controlled by coupled microstrip square ring resonators and the tuning is performed by changing the bias on the varactor diodes. As the first step we begin by synthesizing bandpass filter from a prototype low pass filter, this process can be done by implementing frequency transformation and circuit conversions [1].

Bandpass filters can also be used as delay line [4], by using the correct amount of delay; the signal can be shifted for the intended amount of phase shift. In several applications of electronic it is often necessary to change the phase of signals, for this reason RF and microwave phase shifters have many applications in various equipments.

In this paper, we present a combining study design used for two functions as a phase shifter and as tunable band pass filter in the same time. The filter configuration studied, is based on three square ring resonators. Tunable bandpass filters are designed using half wavelength open loop resonators. A bandpass filter with *14.5%* bandwidth centered at *2.4GHz* was designed. In the following, a phase shifter is constructed with filter designed. A good dynamic range of phase shifting of 90° at operating frequency is obtained.

II. CIRCUIT DESIGN

In order to characterize our filter there are different types of approximation (Chebyshev, Butterworth, Elliptic and quasi-Elliptic) [3]. For this purpose we have studied the three cases of filter approximation by using our filter characteristic given as following:

Center frequency $F_c = 2.4$ GHz

Bandpass width $BW = 200$ MHz

Insertion loss $IL \leq 0.3$ dB

Stopband attenuation $L_{As} = 20.0$ dB at normalized frequency $\Omega_s = 2.0$.

a) Filter Synthesis

We start our filter synthesis by choosing the lowpass prototype; we discuss the design of passband filter described by the specifications above. The figure 1, gives three examined filter response, the equation 1 determine the filter n order of chosen Butterworth approximation [4] :

$$n = \frac{\log\left(10^{0.1L_{As}} - 1\right)}{2\log \Omega_s} \qquad (1)$$

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By using equation 1 and the filter specifications, we can calculate the filter order as n = 3. The figure 1 gives the transmission characteristics of different approximations Butterworth, Chebyshev and Elliptic.

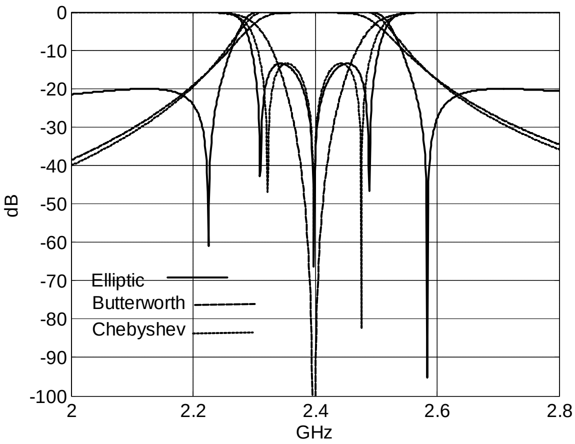

Fig.1 : Transmission characteristics of different approximations

We chose Butterworth approximation for satisfaction of our fixed filter characteristics. The figure 2 presents Butterworth lowpass prototype [4] filter and the bandpass calculated filter.

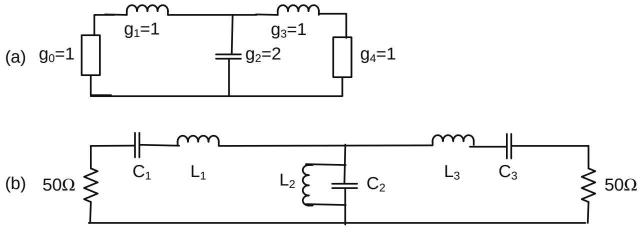

Fig.2. (a) : Three poles lowpass prototype, (b): Lumped components bandpass filter

The parameters of the Butterworth lowpass prototype [4] i.e. are $g_0=1$, $g_1=1$, $g_2=2$, $g_3=1$ and $g_4=1$ are determined by using the known formulas in [4], this lowpass prototype is given by the figure 2-a and transformed to lumped element bandpass filter given by figure 2-b when the series and shunt lumped elements were calculated as follows:

$$L_s = \frac{\Omega_c}{\omega_0 FBW}\gamma_0 g_i,\quad C_s = \frac{FBW}{\omega_0 \Omega_c}\frac{1}{\gamma_0 g_i} \tag{2}$$

$$L_p = \frac{FBW}{\omega_0 \Omega_c}\frac{\gamma_0}{g_i},\ C_p = \frac{\Omega_c}{\omega_0 FBW}\frac{g_i}{\gamma_0},\ \gamma_0 = \frac{Z_0}{g_0} \tag{3}$$

L_1=40nH, C_1=0.1pF, L_2=0.13nH, C_2=32pF, L_3=40nH and C_3=0.1pF.

The figure 3 gives lowpass prototype obtained by impedance inverters. This figure consists of J-inverters and shunt resonators only. The derived formulas [4] permitted to calculate the (B_i, g_i) lumped components that are given by the equations (1-5).

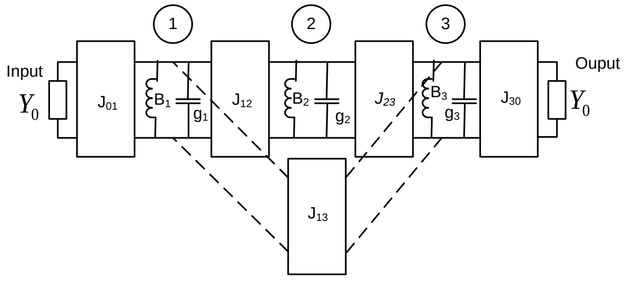

Fig.3 : Lowpass filter admittance inverter

The frequency transformation lowpass-bandpass is given by the equation (4), B_i is invariant susceptance.

$$\frac{1}{FBW}\left(\frac{j\omega}{\omega_0}+\frac{\omega_0}{j\omega}\right)g_i + jB_i = j\omega L_i - \frac{1}{j\omega C_i} \tag{4}$$

$$B_i = \omega_0 C_i - \frac{1}{\omega_0 L_i} \tag{5}$$

$$\frac{1}{FBW}\left(\frac{2}{\omega_0}\right)g_i = C_i + \frac{1}{\omega_0^2 L_i} \tag{6}$$

$$C_i = \frac{1}{\omega_0}\left(\frac{g_i}{FBW}+\frac{B_i}{2}\right) \tag{7}$$

$$L_i = \frac{1}{\omega_0}\left(\frac{g_i}{FBW}-\frac{B_i}{2}\right)^{-1} \tag{8}$$

$$\omega_{0i} = \frac{1}{\sqrt{L_i C_i}} = \sqrt{1-\frac{B_i}{g_i/FBW + B_i/2}} \tag{9}$$

$$b_i = \omega_{0i} C_i = \frac{\omega_{0i}}{\omega_0}\left(\frac{g_i}{FBW}+\frac{B_i}{2}\right) \tag{10}$$

The external quality factor and the coupling coefficients can be found by the equation (9):

$$M_{ij} = \frac{J_{ij}}{\sqrt{b_i b_j}} \text{ and } Q_{ext} = \frac{b_1}{g_0} \tag{11}$$

With normalized cutoff frequency Ω_c=1, the following figure 4 gives the general coupling graph of our filter, while the parameters M_{ij} are the inter-resonator coupling parameters.

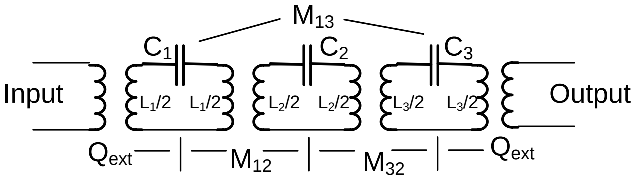

Fig.4 : General bandpass filter coupling structure

b) Filter optimization and method engineering

In the following part, we describe the optimization methodology engineering of our circuit; its principle is given by the figure 5. In this engineering process, we use the filter specifications to determine lumped elements of bandpass filter, and then we introduce the coupling coefficient and the J-inverters. We have used the LinCalc program of Advanced Design System (ADS^{TM}) software to design the circuit and to calculate the geometrical parameters, and by using Momentum we can compare the lumped components and coupled resonator model in order to get more efficient bandpass filter. The proposed engineering method reduces the computational cost with respect to the theory filter synthesis. Moreover the output EM simulation results could be feed back in order to adjust the parameters such resonator dimensions, input feed positions and coupling distances for a better filter performances.

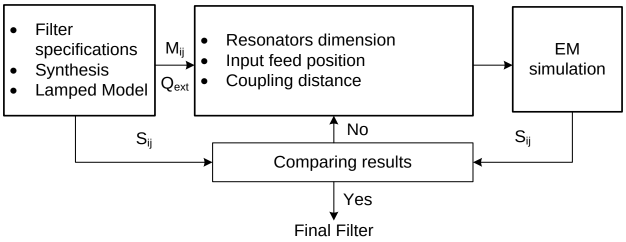

Fig.5 : Bandpass filter optimization

Microwave ring resonators are proposed components for designing our filter. Fig 6 illustrates the filter using three cascaded half wavelength square ring resonators. By using lineCalc program we can calculate the coupling distances (S*)* for three square rings in order to perform the electromagnetic simulation.

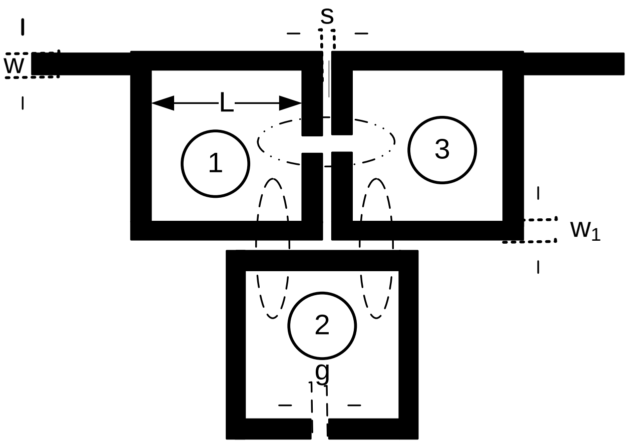

Fig.6 : Three square rings filter and phase shifter

The geometrical parameters of square resonator can be determined by using the equation (10); the characteristic impedance of the resonator is given by:

$$Z_c = \sqrt{L_i / C_i} \tag{10}$$

The excitation inputs have been placed to get a maximum power transferring and have been matched to reference impedance. To insure a maximum power transferring, we use a tapering input section. We change the width of input transmission line to have the same width of main transmission line that constitutes the resonator.

c) Loaded square ring resonator

In this part, with the aim of moving the operating frequency of our circuit as to vary the phase, we load the ring resonators with varactors diodes [5]. The choice of the location of the diodes is made according to the constraints of geometry. The originality of our work is that we load the varactor diode inside of the open loop ring resonator; because in the literature we charge the open loop rings in the slots. The following figure illustrates the location of the varactor diodes and gives the diode model and the via-hole model used to connect the diode to ground.

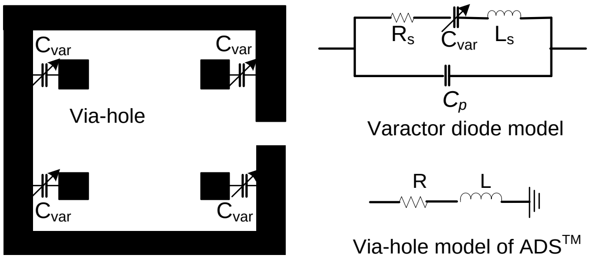

Fig.7 : Loaded varactor diode square ring with varactor diode model and via-hole model

To load the square ring resonator by the varactor diode, we use a via-hole that allows to be connected to the ground through the substrate layer. In this study we have used a model given by the ADS software constituted by serial inductance L and resistor R, this via-hole is defined by $R=0.2\Omega$ and $L=0.55nH$ [6,8].

The model of diode varactor has variable capacitance Cvar and a series resistance $Rs=0.4\Omega$, parasitic series inductance $Ls=0.45nH$, and parasitic parallel capacitance $Cp=0.015pF$ [7].

III. RESULTS AND DISCUSSION

This section contains simulated results obtained for the proposed filter and phase shifter. This structure has been designed using electromagnetic simulator Momentum of ADS^{TM}. The bandpass filter is designed at fundamental resonant frequency $F_C=2.4GHz$, and with bandwidth of *360MHz*. It is built on a microwave Rogers Duroid 4003 substrate having relative permittivity ε_r of *3.36* and height of *0.813mm*.

For this filter, structure of passive filter is realized using microstrip ring resonator. Fig. 8 illustrates the transmission frequency response of bandpass filter simulated with Momentum of ADS. By observing the frequency response, the simulated return loss of the filter in the bandwidth was better than 15dB. The bandpass filter has *3-dB* bandwidth of *360MHz*.

The coupling parameters as: $M_{12}=M_{23}=0.058$, $M_{13}=0.083$ and the quality factor $Q_{in}=Q_{out}=12.05$.

From *2.25GHz* to *2.9GHz* the obtained insertion loss is better than *0.18dB*.

By choosing $C_i=5pF$ and using the equation (10) we can calculate $L_i=34nH$, and $Z_c=82.46\Omega$, from these parameters and by using LineCalc we can obtain $W_1=0.73mm$, $W=1.23mm$, $L=9.88mm$, $g=0.2mm$ and coupling distance between two resonators 1 and 2 of S=0.4mm.

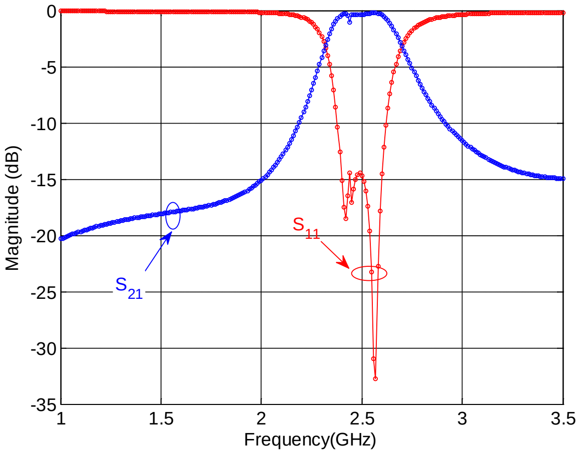

Fig.8 : Simulated frequency responses, transmission and reflection, obtained by three square ring filter

With development of wireless communications system (TX/RX), the bandpass filter is one of most important key components in TX/RX systems, and should also be reconfigurable to meet the system requirements. The filter described previously can be modified to get an electronically tunable filter using varactor diodes.

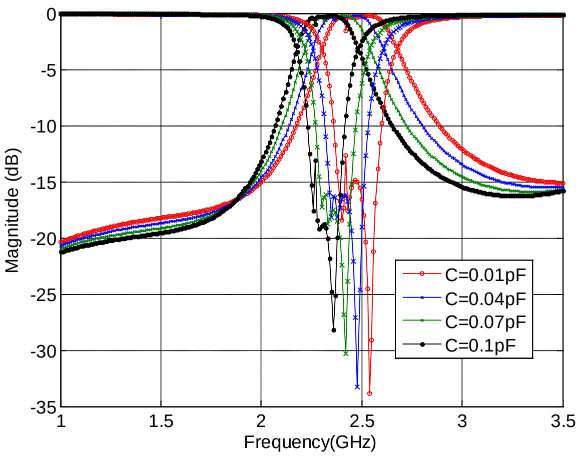

Fig.9 : Retun and insertion losses for three ring resonators filter at the operating frequency (2.4GHz)

The tunable filter is investigated, which implements with varactor diodes placed inside of square ring resonator as shown in Fig.7. The S_{11} and S_{21} simulation results of this filter are shown in Fig.8. The capacitances of varactor diodes C which are varied from 0.01 pF to 0.1 pF, have a fundamental role to tune filter center frequency. To reach a fractional bandwidth range from 13% to 14.5%, a variation of C is required. Fig.9 shows bandwidth tuning was controlled by capacitance C, which modifies the resonator capacitive coupling from the main transmission line. The filter center frequency from 2.48 GHz to 2.32 GHz, is changing by modifying capacitance bias from 0.01 to 0.1 pF. The Fig 9 shows the insertion and return loss variations of three square rings phase shifter given by the Fig. 6 versus frequency for different values of capacitance. We notice in the Fig. 9, the variation of insertion loss versus frequency for different values of capacitance. The maximums |S11| and |S21| losses, for C = 0.01pF are about |S11(2.48GHz)|=15.0dB, |S21(2.48GHz)| =0.35dB; for C = 0.1pF are about |S11(2.32GHz)| =19.0dB, |S21(2,32GHz)|=0.26dB. If we decrease the value of capacitance we get lower quantity of losses.

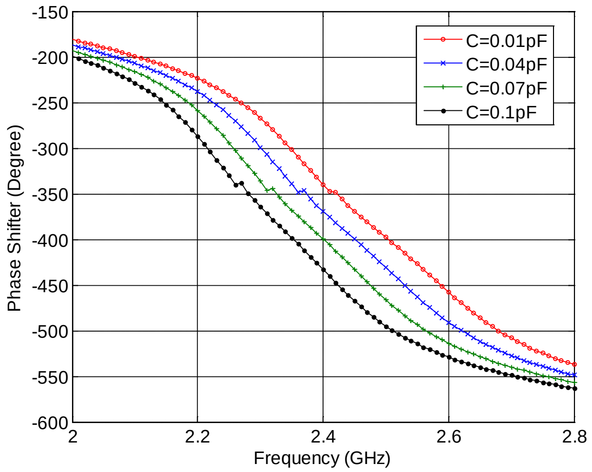

Fig.10 : Phase shifting in degrees versus frequency

Figure 10 shows the phase shift variation versus frequency, the capacitance varies between 0.01pF and 0.07pF. A linear phase shift variation is performed by the phase shifter for different value of capacitance. For C=0.01pF the maximum value of differential phase shift is about 10° while for C=0.07pF the phase shift varies from 0° to -80° at the frequency 2.4GHz. Figure 11 illustrates the linear variation of phase versus capacitances at 2.4GHz.

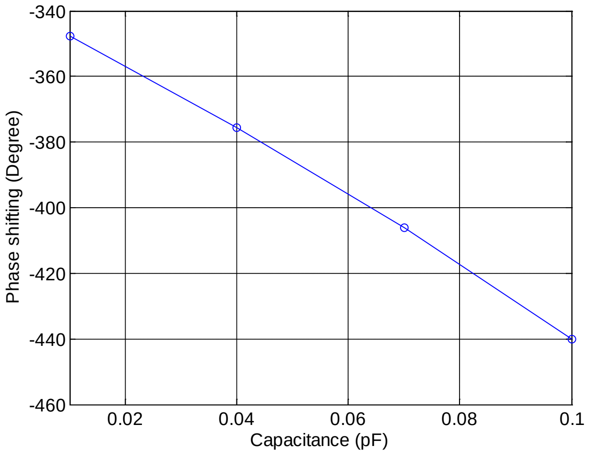

Fig.11 : Phase shifting in degrees at the operating frequency 2.4GHz versus variable capacitance.

By examining the figure above, we deduced that the phase dynamic at 2.4GHz is about 90° and linear behavior can be denoted.

IV. CONCLUSION

A new type of tunable filter and phase shifter has been proposed. The varactor diodes have been applied to the design of tunable band pass filter where center frequency and bandwidth can be controlled. A capacitance bias from 0.01 to 0.1pF was applied to shift the filter's center frequency from 2.48GHz to 2.32GHz and its 3-dB fractional bandwidth from 13% to 14.5%. We mention also a good dynamic range of phase shifting about 90° at operating frequency 2.4 GHz. In this study we have designed a circuit that could be used in the same time as tunable filter and phase shifter and good results was obtained.

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Effect of Structure Parameters on the Signal Strength in a Solid Beam Driven Plasma-Loaded Backward Wave Oscillator

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Abstract - The effect of structure parameters on the group velocity and signal strength of a solid beam driven plasmaloaded backward wave oscillator is investigated analytically for a particular mode. The theory of approximate cubic dispersion equation as derived earlier for a solid beam driven plasmaloaded backward wave oscillator (BWO) is used for this investigation. The effect of variation of structure parameters on the temporal and spatial growth rates and group velocity result a change in the signal strength of BWO.

Keywords : structure parameters, plasma, dispersion, growth rates, signal strength.

GJRE-F Classification : FOR Code: 100599p

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Dilip Kumar Sarker $^{\alpha}$, Diponkar Kundu $^{\sigma}$, Pallab Kanti Podder $^{\rho}$, Md. Masudur Rahman $^{\omega}$ & Kallol Krishna Karmakar $^{¥}$

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Keywords : structure parameters, plasma, dispersion, growth rates, signal strength.

I. INTRODUCTION

In this paper, the effects of waveguide parameters on the group velocity and signal strength of a plasmaloaded BWO with sinusoidally corrugated slow wave structure having very smaller corrugation depth driven by a solid intense relativistic electron beam have been investigated analytically. This study is based on the approximate linear theory of absolute instability derived for a solid beam driven plasma-loaded BWO[1]. In the previous works, most of the researchers conducted investigations for efficiency and resonance enhancement, power enhancement and frequency shifting of microwave emission in a plasma filled BWO[2-5]. Most of them carried out their analysis keeping the structure parameters constant. Some of the researchers have devoted their interests on the investigations comprising slow-wave instability by numerical analysis [6 - 10]. Some researchers work on absolute instability for annular electron- beam driven plasma-loaded BWO[11,12]. Here, the authors are interested to study the effect of variation of structuresize parameters on the group velocity and signal strength of a solid beam driven plasma loaded BWO by absolute instability analysis for TM_{01} mode. Formulation of the analytical dispersion relation is presented in Section II. Section III describes the analytical results of the analysis. Discussion and conclusions are stated in section IV.

II. FORMULATION

In deriving the expression of group velocity and arbitrary signal strength, an waveguide model consisting of a sinusoidally corrugated-wall structure having very smaller corrugation depth is considered [1]. The waveguide inner space is filled completely with plasma of uniform density N_p. A relativistic electron beam of density N_b, that is assumed covers the entire inner space of the waveguide, is moving along the waveguide axis with a velocity v_b relative to the background plasma. The entire system is assumed to be immersed in a strong infinite axial guiding magnetic field B_0. The numerical dispersion relation of this beam-plasma waveguide system for TM_{01} mode is $D(k, \omega) = 0$[13]. Where, D is the value of the determinant of a square matrix with elements D_{mn}. and k and ω are respectively the wavenumber and frequency. The approximate dispersion relation of this system for the resonance interaction of the zeroth beam harmonic with the electromagnetic first slow harmonic as shown in Fig.1 can be expressed as,

$$\begin{bmatrix} D_{-1-1} & D_{-10} \\ D_{0-1} & D_{00} \end{bmatrix} = 0 \qquad (1)$$

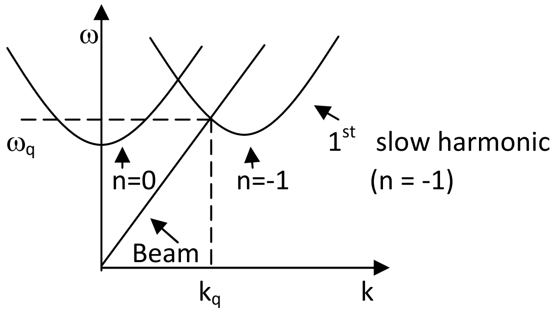

Figure 1 : Resonance of the zeroth beam and electromagnetic first slow harmonic.

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The matrix elements of the above relation are:

$$\left.\begin{aligned}
D_{-1-1} &= J_0(X_{-1})\\
D_{00} &= J_0(X_0)\\
D_{-10} &= \left(1+\frac{k_0 k}{\frac{\omega^2}{c^2}-k^2}\right)\frac{a}{2}X_0 J_0'(X_0)\\
D_{0-1} &= \left(1-\frac{k_0 k_{-1}}{\frac{\omega^2}{c^2}-k_{-1}^2}\right)\frac{a}{2}X_{-1} J_0'(X_{-1})
\end{aligned}\right\} \qquad (2)$$

Here,

$$\frac{X_n^2}{R_0^2} = \left(\frac{\omega^2}{c^2}-k_n^2\right)\left(1-\frac{\omega_p^2}{\omega^2}\right) - \left[\left(\frac{\omega^2}{c^2}-k^2\right)\frac{\omega_b^2}{\gamma^3(\omega-k_n v_b)^2}\right]\delta_{n,0} \qquad (3)$$

where, c, ω_p, ω_b and v_b are light velocity, plasma frequency, beam frequency and beam velocity respectively, and $\delta_{n,0} = 0$ unless $n = -1$; $k_n = (k + nk_0)$.

The oscillation frequency ω_q and hence the wave number k_q can be obtained by solving eq.(1) with $\omega_b = 0$. The cubic equation describing the frequency and wave number perturbations of the three waves involved in the resonance interaction is obtained from the dispersion relation stated in eq. (1) as,

$$(\delta\omega - v_b\delta k)^2(\delta\omega - v_g\delta k) = \Delta \qquad (4)$$

$$\text{where, } \Delta = -\frac{\omega_b^2\gamma^{-3}\beta_1 a^2\lambda_{-1}^2\left(\frac{\omega_q^2}{c^2}-k_q^2\right)}{8\lambda_0\left[\frac{\omega_q}{c^2}-\frac{\omega_p^2(k_q-k_0)^2}{\omega_q^3}\right]}\times\frac{J_0'(\lambda_{-1})}{J_0(\lambda_0)}\left[1+\lambda_0\frac{J_0''(\lambda_0)}{J_0'(\lambda_0)}\right]$$

$$\beta_1 = \left[1+\frac{k_0 k_q}{\frac{\omega_q^2}{c^2}-k_q^2}\right]\left[1-\frac{k_0(k_q-k_0)}{\frac{\omega_q^2}{c^2}-(k_q-k_0)^2}\right]; \qquad a = \frac{h}{R_0}$$

$$\lambda_{-1}^2 = \left[\frac{\omega_q^2}{c^2}-(k_q-k_0)^2\right]\left[1-\frac{\omega_p^2}{\omega_q^2}\right]R_0^2$$

$$\frac{J_0'(\lambda_{-1})}{J_0(\lambda_0)}\left[1+\lambda_0\frac{J_0''(\lambda_0)}{J_0'(\lambda_0)}\right] = \begin{cases} 1 \text{ for} \lambda_0 \text{ is imaginary}\\ -1 \text{ for} \lambda_0 \text{ is real}\end{cases}$$

$$\lambda_n = X_n(\omega_q, k_q, X_b = 0)$$

Expression of group velocity can be stated as,

$$v_g = \frac{\left[\left(1-\frac{\omega_p^2}{\omega_q^2}\right)(k_q-k_0)\right]}{\left[\frac{\omega_q}{c^2}-\frac{\omega_p^2}{\omega_q^3}(k_q-k_0)^2\right]} \qquad (5)$$

At the moment of absolute instability there exists a saddle point in the complex k-plane, where one finds two equal roots of complex wavenumber k for some value of complex frequency ω with $\omega_i > 0$. The imaginary parts of these frequency and wavenumber represent temporal and spatial growth rates respectively. Using these values of complex ω and k within the range of linear analysis, arbitrary value of signal strength can be calculated.

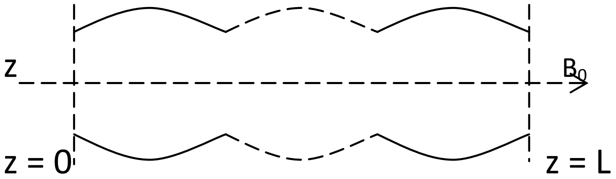

Figure 2: BWO structure showing the position (z = 0), where arbitrary signal strength is calculated. The signal is assumed to originate at z = L.

The expression of signal strength can be written as,

$$f \propto e^{i\left(ik_i L - i\omega_i \frac{L}{v_g}\right)} \qquad (6)$$

Here, L is the distance traversed by the wave in time $t = L/v_g$, and is equal to the axial length of the structure. It is noted that, in calculating t the group velocity v_g is used, because the energy transport velocity of a composite wave in a loss-less waveguide is equal to be the group velocity of the wave.

III. Analytical Results

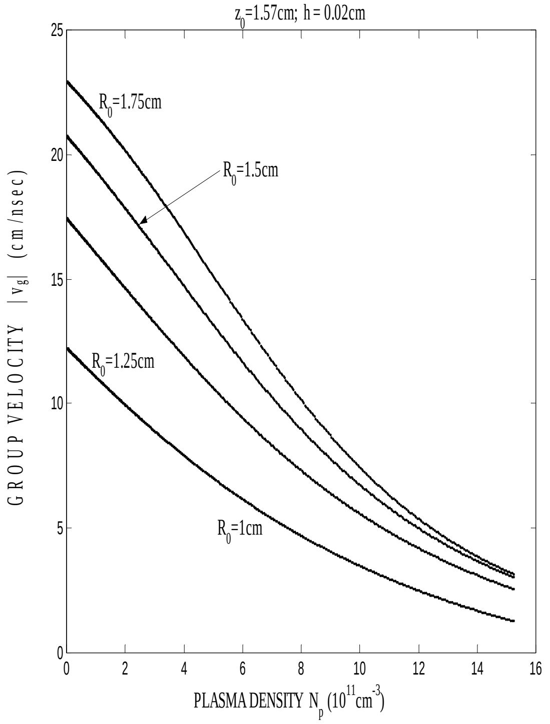

Figure 3 : Group velocity versus plasma density characteristics for different structure average radii.

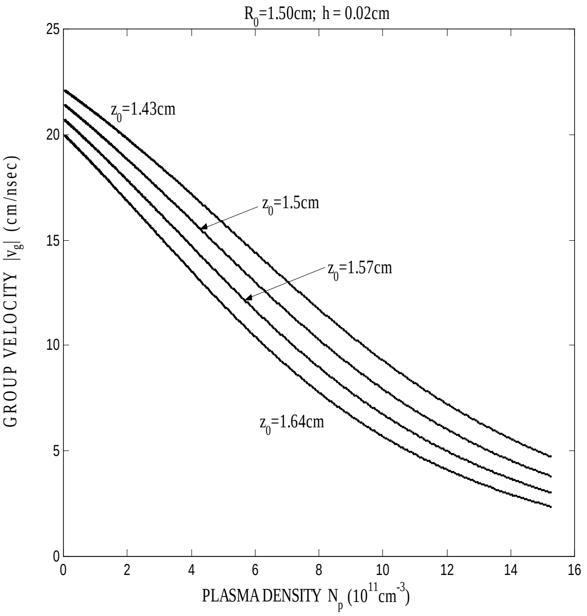

Figure 4 : Group velocity versus plasma density characteristics for different structure corrugation periods.

The effect of plasma density, N_p and structure average radius, R_0 on the group velocity, v_g is shown in Fig. 3. In this observation, the variation of group velocity for various structure average radius are plotted keeping the corrugation period, z_0 and the corrugation depth, h constant. From the figure it is seen that group velocity decreases with plasma density and increases with structure average radius. This figure also depicts that the rate of decrease of group velocity with the increase in plasma density is greater for the larger values of structure average radius. In Fig. 4 the effect of plasma density, N_p and structure corrugation period, z_0 on the group velocity, v_g are shown. In this observation, the variation of group velocity for various structure corrugation periods are plotted keeping the structure average radius, R_0 and the corrugation depth, h constant. This figure reveals that group velocity decreases with the increase in plasma density and structure corrugation period.

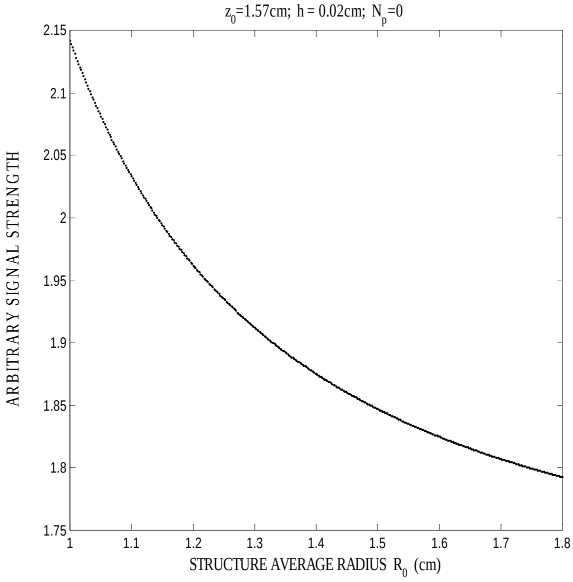

Figure 5 : Structure average radius versus arbitrary signal strength.

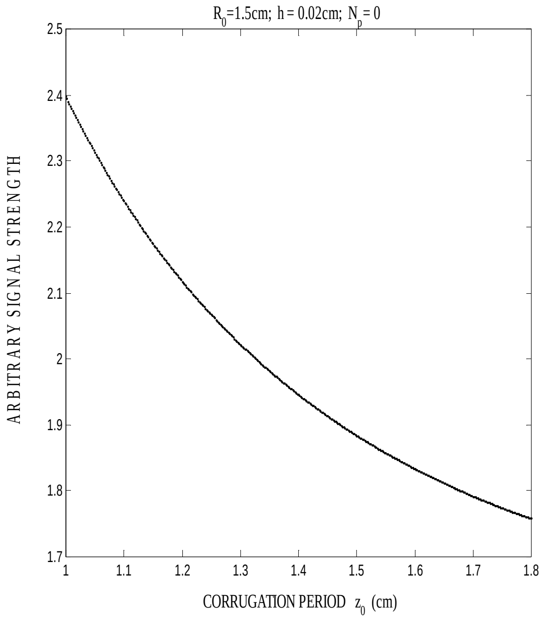

Figure 6 : Structure corrugation period versus arbitrary signal strength.

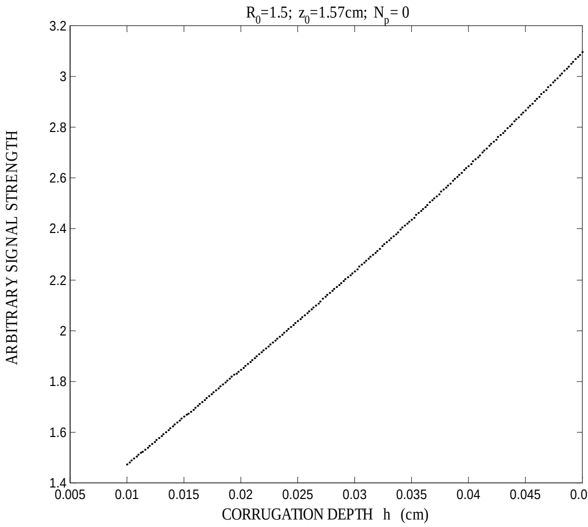

Figure 7 : Structure corrugation depth versus arbitrary signal strength.

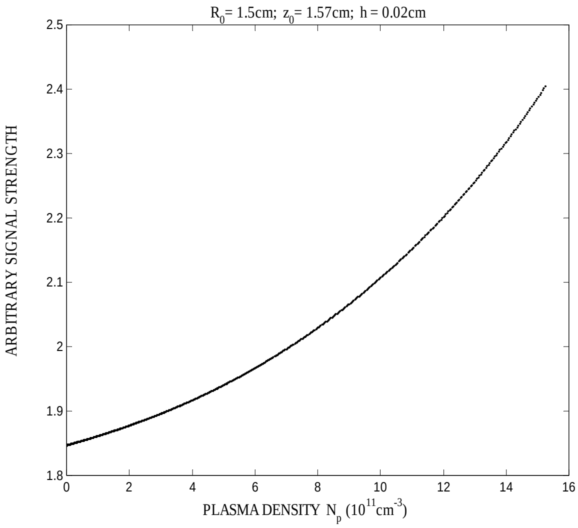

Figure 8 : Plasma density versus arbitrary signal strength.

The variation of the temporal and spatial growth rates and the group velocity result a change in the signal strength of a BWO. The simultaneous effects of these three factors on the arbitrary signal strength, due to the variation of structure parameters are presented in the Figs. 5, 6 and 7 respectively. The figures reveal that the increase in structure average radius and corrugation period cause a decrease in signal strength and the increase in structure corrugation depth causes an increase in signal strength. Fig. 8 depicts that with the increase in plasma density signal strength is also increased. The arbitrary strength of the signal is calculated at $z = 0$, as the signal is assumed to originate at $z = L$ as shown in Fig.2, where the arbitrary value of L is taken as 20cms.

IV. Summary and Discussions

The instability phenomena comprising a plasmaloaded BWO consisting of a sinusoidally corrugated slow wave structure having very smaller corrugation depth driven by a solid intense relativistic electron beam, has been analyzed for investigating the effects of waveguide parameters on the group velocity and signal strength. In this analytical study, the modified theory of instability of three wave interaction for a solid beamdriven plasma-loaded BWO [1] has been employed. The effect of structure-size parameters and plasma density on the group velocity and signal strength have been carefully investigated here using the analytical results of temporal and spatial growth rates[1]. From this study one can get information about the parametric and background plasma effects on the signal strength of a backward wave oscillator operating in the X-band frequency range and it may be helpful in future for further study on BWO.

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Literature Review on Voltage stability phenomenon and Importance of FACTS Controllers In power system Environment

By R.Siva Subramanyam Reddy & Dr.T.Gowri Manohar

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Abstract - Now a days the use of stable, reliable, economical, secure and efficient electrical paper drastically increasing in many sectors but the generated power in not being supported as much as increasing demand. The voltage stability plays major role in power system environment to meet the required demand. In this paper presents the phenomena of voltage stability in power system in which it reviews various reasons for voltage instability, types of voltage stability, characteristic of voltage stability, voltage control methods in power system environment, factors affecting voltage instability and collapse, scenario of voltage collapse and characteristics of reactive compensating devices are primarily discussed. It also reviews overview of major FACTS controllers, types of FACTS controllers, applications of FACTS controllers and their use in power system environment are discussed briefly.

Keywords : Voltage Stability, Voltage Instability, Voltage Collapse, Reactive compensating devices, FACTS Controllers.

GJRE-F Classification : FOR Code: 090607

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I. INTRODUCTION

In recent years greater demands have placed on the transmission network, with this increased demands on transmission lines, hence it is the responsibility of the power suppliers to supply safe and economical electric power to customers with the existing transmission line efficiently.

"*Voltage stability is the ability of a power system to maintain steady acceptable voltages at all buses in the system under normal operating conditions and after being subjected to a disturbance*"[1].

In power system environment voltage stability plays major role, it is integral part of the power system stability. In general Voltage stability problems occur more frequently in a heavily loaded system. The change in voltage is directly proportional to change in load and hence voltage stability is sometimes termed as load stability.

Voltage stability is a part of power system stability and hence is a subset of overall power system stability and is a dynamic problem. Thus voltage instability and collapse cannot be separated from the general problem of system stability. The reactive power compensation close to the load centres as well as at critical buses in the network is essential for overcoming voltage instability. The location, size and speed of control have to be selected properly to have maximum benefits. The SVC and STATCOM provide fast control and help improve system stability [2].

The suitable location of FACTS devices, under contingencies is more important than consideration of normal state of system. Now a day's many literatures are proposed various intelligent techniques to control FACTS devices in optimal manor for enhancing voltage stability which intern enhanced the power system stability.

II. VOLTAGE STABILITY PHENOMENON IN POWER SYSTEM

In recent years, voltage instability has been responsible for several major network collapses in New York, Florida, French, Northern Belgium, Swedish, Japanese, Mississippi, Srilanka, North America, Pakistan and Tokyo etc.[1][3].

a) Major reasons for voltage stability problems in power system

There are some reasons for voltage stability problems in power system as follows

- Large load or large disturbance in a heavily stressed power system.
- Large disturbance between generation and load
- Unfavourable load characteristics
- More distance between Voltage sources and load centres.
- The source voltage is too low.
- In sufficient load reactive compensation.
- Action of ULTC during low voltage conditions and.
- Poor coordination between various control and protective systems.
- High reactive power consumption at heavy loads
- Unsuitable locations of FACTS controllers [3][4].

b) Classifications of voltage stability

The voltage stability may be broadly classified in to two categories:

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i. *Large-disturbance voltage stability*

It is define as the ability of the power system to maintain stable voltages for large disturbances such as such as system faults, loss of load, or loss of generation.

Large disturbance voltage stability may be further subdivided into two types

a) Transient stability
b) Long term stability

ii. *Small- disturbance (Small signal) voltage stability*

Small disturbance voltage stability is concerned with a system's ability to control voltages following small perturbations, such as gradual change in load, this types of stability can be studied with steady-state approaches that use linearization of the system dynamic equations at a given operating point.

c) Factors Affecting voltage instability and collapse

The main factor causing instability is the inability of the power system to meet the demand for reactive power.

i. *Transient voltage instability*

Under low voltage condition the electrical torque of an induction motor is not adequate to meet the required mechanical torque due to this effect the induction motor may not regain the original speed and continue to decelerate leading to stalling of motors which intern aggravates the low voltage problem. This phenomenon is called transient voltage instability. Transient voltage instability is also associated with HVDC links, particularly inverter terminals connected to AC systems with low short circuit capacity [2] [5] [6].

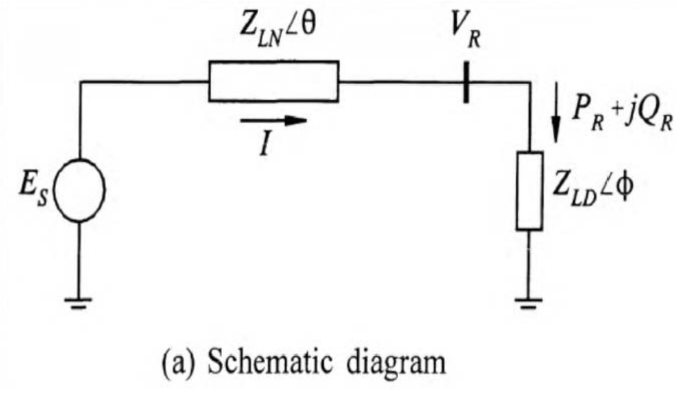
ii. *Long term voltage instability*

On-load tap-changing transformers and distribution voltage regulations act within a time frame of tens of seconds to tens of minutes to regulate the load a voltage is termed as long term voltage instability. An important factor in long term voltage stability is the current limiting generator [2] [7].

d) Typical scenario of voltage collapse

When a power system is subjected to a sudden increase of reactive power demand following a system contingency, the additional demand is met by the reactive reserves carried by the generators and compensators.

Voltage instability may occur in several different ways. In its simple form it can be illustrated by considering the two terminal network of fig.1 it consists of a constant voltage source (Es) supplying a load (ZLD) through a series impedance (ZLN). This is representative of a simple radial feed to load or a load area served by a large system through a transmission line.



(a) Schematic diagram

Fig.1 : A simple radial system for illustration of voltage stability phenomenon.

Voltage stability, in facts, depends on the relationships between P, Q and V. The traditional forms displaying these relationships are shown in fig.2.The V_R-P_R relationship for different values of load power factor. The locus of critical operating points is shown by the dotted line in the fig.Normally; only the operating points above the critical points represent satisfactory operating conditions. sudden reduction in the power factor(increase in QR) can thus cause the system to change from a stable operating condition to an unsatisfactory, and possibly unstable, operating condition represented by the lower part of a V-P curve [1][2][8][9].

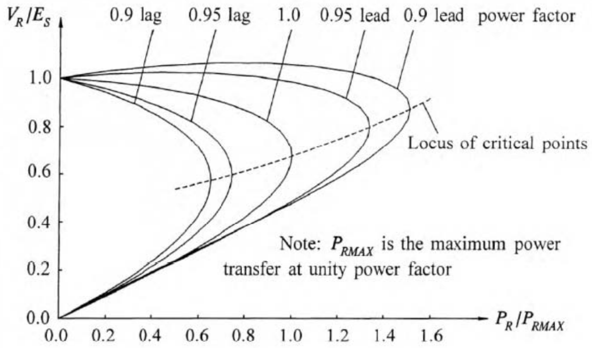


Fig.2 : V_R-P_R characteristics of the system of fig.1 with different load-PF

e) Characteristics of voltage collapse

- The initiating event may be due to a variety of decay of voltage.
- The collapse generally manifests itself as a slow decay of voltage.
- The duration of voltage collapse dynamics in some situations may be much shorter, being on the order of a few seconds.
- The time frame of this class of voltage instability is the same as that of rotor angle instability [1][10].

f) Prevention of voltage collapse in power system

i. System design measures

- Application of reactive power-compensating devices.
- Control of network voltage and generator reactive output.
- Coordination of protections/controls
- Control of transformer tap changers
- Under voltage load shedding

ii. System operating measures

- Stability margin
- Spinning reserve
- Operators' action

g) Voltage control methods in power system

The control of voltage levels is accomplished by controlling the production, absorption, and flow of reactive power at all levels in the system. The devices used for this purpose may be classified as follows

- Sources or sinks of reactive power, such as shunt capacitors, shunt reactors, synchronous condensers, and static var compensators (SVCs)
- Line reactance compensators, such as series capacitors.
- Regulating transformers, such as tap-changing transformers and boosters [1].

h) Characteristics of compensating devices

i. Shunt capacitors

- They can be effectively used up to a certain point to extend the voltage stability limits by correcting the receiving end PF.
- Shunt capacitors, however, have a number of inherent limitations from the viewpoint of voltage stability and control.
- In heavily shunt capacitor compensated system, the voltage regulation tends to be poor.
- Beyond a certain level of compensation, stable operation is unattainable with shunt capacitor.
- The reactive power generated by a shunt capacitor is proportional to the square of the voltage; during system conditions of low voltage the var support drops, thus compounding the problem.

ii. Series capacitors

- Series capacitors are self-regulating.
- The reactive power supplied by series capacitors is proportional to square of the line current and is independent of the bus voltages.
- This has favourable effect on voltage stability.

The present trend is to operate the existing transmission system more close to their stability and thermal limits with reliable and optimal. Power electronics based Flexible AC transmission system (FACTS) gives efficient solution for optimal utilization of transmission systems with minimal installation and operational cost [1][4].

III. OVERVIEW OF MAJOR FACTS CONTROLLERS

The development of FACTS-devices has started with the growing capability of power electronics components. Devices for high power levels have been made available in converters for higher and even highest voltage levels. Several FACTS have been introduced for various applications worldwide.

a) Basic Types of FACTS controllers

- Shunt controllers
- Series controllers
- Combined shunt-series controllers
- Combined series-series controllers

The shunt controllers are applied to control voltage at and around the operating point by injecting reactive current.

Series controllers are applied to improving voltage profile in a cost effective way ware voltage fluctuations are large. However the series controllers are several times more powerful than the shunt controllers.

The combined controllers provide the best of both i.e. an effective power/current flow and line voltage control.

FACTS-devices provide a better adaption to varying operational conditions and improve the usage of existing installations

b) Applications of FACTS controllers

- Control of power flow in a transmission line
- Increase the loading capability of line to their thermal limit.
- Control of voltage in a line
- Control of reactive power in a power line
- Improvement of system stability, security & reliability
- power quality improvement in a line
- Provide greater flexibility insisting new generation
- Upgrade of lines
- Reduce reactive power flows
- Increase utilization of lowest cost generation
- Rapid dynamic response
- Ability for frequent variation in output
- Smooth adjustable output
- Minimized transmission losses.

The voltage and stability limits shall be shifted with the means of the several different FACTS-devices shown in below fig.[11][13]-[16].

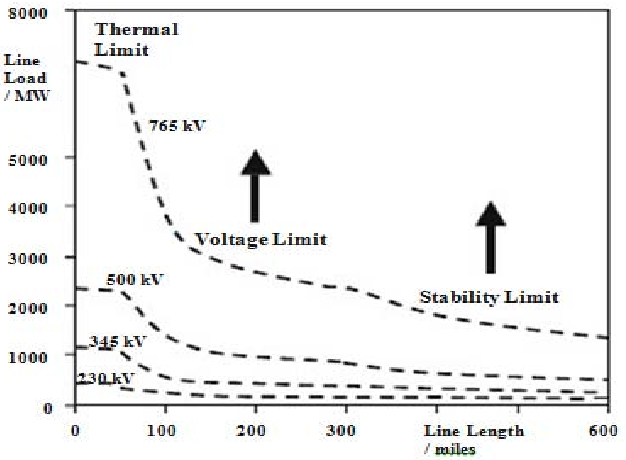


Fig. 3 : Operational limits of transmission lines for different voltage levels

The ability of FACTS controllers to control the interrelated parameters that govern the operation of transmission systems including series impedance, shunt impedance, current, voltage, phase angle and the damping of oscillations at various frequencies below the rated frequency. These constraints cannot be overcome, while maintaining the required system reliability, by mechanical means without lowering the useable transmission capacity.

There are a number of stability issues that limit the transmission capacity these include transient, dynamic, steady state stabilities, frequency collapse , sub synchronous resonance and voltage collapse. The FACTS technology can certainly be used to overcome any of the stability limits. An over-view of problems occurring in the grid and which FACTS to be used to solve these problems are given in the table blow. The application of these devices depends on the problem which has to be solved, below table shows various problems in the grid and which FACTS device to be used to solve these problems [12][16].

Subject	Problem	Corrective action	FACTS
Voltage limits	Low voltage at heavy load	Supply reactive power	SVC, STAT-COM
		Reduce line reactance	TCSC
	High voltage at low load	Absorb reactive power	SVC, STAT-COM
	High voltage following an outage	Absorb reactive power, prevent overload	SVC, STAT-COM
	Low voltage following an outage	Supply reactive power, prevent overload	SVC, STAT-COM
Thermal limits	Transmission circuit overload	Increase transmission capacity	TCSC,SSSC, UPFC
Load flow	Power distribution on parallel lines	Adjust line reactance	TCSC,SSSC, UPFC
		Adjust phase angle	TCSC,SSSC, PAR
	Load flow reversal	Adjust phase angle	TCSC,SSSC, PAR
Short circuit power	High short circuit current	Limitation of short circuit current	TCSC, UPFC
Stability	Limited transmission power	Decrease line reactance	TCSC,SSSC

Table 1 : Examples of use of FACTS

IV. Conclusion

This paper gives a summary of voltage stability analysis, importance of voltage stability & voltage instability in power system, and various reasons for voltage instability, methods of preventing voltage instability, characteristics of reactive power compensating devices (shunt & Series) and also explains the importance of FACTS controllers in power system environment enhancing voltage stability which intern enhance the power system stability.

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Comparison of Packet Delivery for Black Hole Attack in ad hoc Network

By Yatin Chauhan, Prof Jaikaran Singh & Prof Mukesh Tiwari

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Abstract - Black hole attack is a serious threat in a mobile ad hoc network (MANET). In this attack, a malicious node injects a faked Route Reply message to deceive the source node so that the source node establishes a route to the malicious node and sends all the data packets to the malicious node. The black hole attack can degreed the performance of different routing protocols. During this attack, a malicious node captures packets and not forwards them in the network. This paper illustrates how black hole attack can affect the performance of Mobile Ad hoc networks by using NS-2.34 simulator.

Keywords : MANET; Black hole attack.

GJRE-F Classification : FOR Code: 291704

Comparison of Packet Delivery for Black Hole Attack in ad hoc Network

Yatin Chauhan [α], Prof Jaikaran Singh [α] & Prof Mukesh Tiwari [α]

Abstract - Black hole attack is a serious threat in a mobile ad hoc network (MANET). In this attack, a malicious node injects a faked Route Reply message to deceive the source node so that the source node establishes a route to the malicious node and sends all the data packets to the malicious node. The black hole attack can degreed the performance of different routing protocols. During this attack, a malicious node captures packets and not forwards them in the network. This paper illustrates how black hole attack can affect the performance of Mobile Ad hoc networks by using NS-2.34 simulator.

Keywords : MANET; Black hole attack;

I. INTRODUCTION

Mobile ad hoc network (MANET) is one of the recent active fields and has received spectacular consideration because of their self-configuration and self-maintenance. Early research assumed a friendly and cooperative environment of wireless network. As a result they focused on problems such as wireless channel access and multihop routing. But security has become a primary concern to provide protected communication between mobile nodes in a hostile environment. Although mobile ad hoc networks have several advantages over wired networks, on the other side they pose a number of non-trivial challenges to the security design as they are more vulnerable than wired networks [1]. These challenges include open network architecture, shared wireless medium, demanding resource constraints, and, highly dynamic network topology. In this paper, we have considered a fundamental security problem in MANET to protect its basic functionality to deliver data bits from one node to another. Nodes help each other in conveying information to and fro and thereby creating a virtual set of connections between each other. Routing protocols play an imperative role in the creation and maintenance of these connections[4,5]. In contrast to wired networks, each node in an ad-hoc networks acts like a router and forwards packets to other peer nodes. The wireless channel is accessible to both legitimate network users and malicious attackers. As a result, there is a blurry boundary separating the inside network from the outside world.

Many different types of routing protocols have been developed for ad hoc networks and have been classified into two main categories by Royer and Toh (1999) as *Proactive* (periodic) protocols and *Reactive* (on-demand) protocols. In a proactive routing protocol, nodes periodically exchange routing information with other nodes in an attempt to have each node always know a current route to all destinations [2]. In a reactive protocol, on the other hand, nodes exchange routing information only when needed, with a node attempting to discover a route to some destination only when it has a packet to send to that destination [3]. In addition, some ad hoc network routing protocols are hybrids of periodic and on-demand mechanisms.

Wireless ad hoc networks are vulnerable to various attacks. These include passive eavesdropping, active interfering, impersonation, and denial-of-service. A single solution cannot resolve all the different types of attacks in ad hoc networks. In this paper, we have evaluated MANET with and without black hole attack. In Section II of this paper, we summarize the basic operation of AODV (Ad hoc On-Demand distance Vector Routing) protocol on which we base our work. In Section III, we describe the effect of blackhole attack in AODV. Section IV presents the performance evaluation based of MANET with and without black hole attack on simulation experiments. Section V presents conclusion and future work.

II. AODV

One of the typical routing protocols for MANET is called Ad hoc On-Demand Distance Vector (AODV) [4]. In this protocol, if a source node wants to send data packets to a certain destination node, the source node broadcasts a Route Request (RREQ) packet. Every node that receives the RREQ packet checks whether the node is the destination for that packet and if it is the case, the node sends back a Route Reply (RREP) packet. If it is not the case, then the node checks with its routing table to determine if it has a route to the Destination. If it does not have such a route, it relays the RREQ packet by broadcasting the packet to its neighbours. If it has a route to the destination, then the node compares the destination sequence number in its routing table with that in the RREQ packet. The number in the RREQ packet was obtained by the source node from the packet transmitted by the destination to the source node. If the number in the routing table is larger

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than that In the RREQ packet, the route is fresher and the data packets can be sent through this route. Then this node becomes an intermediate node and sends back a RREP packet to the source node along the route through which it received the RREQ packet. The source node then updates its routing table and starts to send its data packets through this route. However, this protocol is highly susceptible to routing attacks especially the black hole attack [6] because of the dynamic topology and lack of any infrastructure in the network.

III. BLACK HOLE ATTACK

An ad-hoc routing protocol is a convention, or standard, that controls how nodes decide which way to route packets between computing devices in a mobile adhoc network. Being one of the category of ad-hoc routing protocols, on-demand protocols such as AODV (Ad-hoc On demand Distance Vector) and DSR (Dynamic Source Routing) establish routes between nodes only when they are required to route data packets. AODV is one of the most common adhoc routing protocols used for mobile ad-hoc networks. As its name indicates AODV is an on-demand routing protocol that discovers a route only when there is a demand from mobile nodes in the network.

In an ad-hoc network that uses AODV as a routing protocol, a mobile node that wishes to communicate with other node first broadcasts an RREQ (Route Request) message to find a fresh route to a desired destination node. This process is called route discovery. Every neighbouring node that receives RREQ broadcast first saves the path the RREQ was transmitted along to its It subsequently checks its routing table to see if it has a fresh enough route to the destination node provided in the RREQ message. The freshness of a route is indicated by a destination sequence number that is attached to it. If a node finds a fresh enough route, it unicasts an RREP (Route Reply) message back along the saved path to the source node or it re-broadcasts the RREQ message otherwise. The same process continues until an RREP message from the destination node or an intermediate node that has fresh route to the destination node is received by the source node. Route discovery is a vulnerability of on-demand ad-hoc routing protocols, especially AODV, which an adversary can exploit to perform a black hole attack on mobile ad-hoc networks. A malicious node in the network receiving an RREQ message replies to source nodes by sending a fake RREP message that contains desirable parameters to be chosen for packet delivery to destination nodes. After promising (by sending a fake RREP to confirm it has a path to a destination node) to source nodes that it will forward data, a malicious node starts to drop all the network traffic. An ad hoc network is the assortment of cooperative wireless nodes without existence of any access point or infrastructure. However, none of them deal with the issues of security. The presence of malicious nodes in an ad hoc network deteriorates the network performance.

IV. PERFORMANCE EVALUATION

Some assumptions, which are considered realistic, are presented. First of all, the MANET is based on IEEE 802.11 standards. We consider a rather large scale MANET which is deployed in a hostile environment. Nodes are limited in their storage and computational and communication resources. Every node has the same transmission range and non-directional antenna. The nodes are battery-powered, and hence it is crucial to conserve energy to prolong the lifetime of the network. Due to the wireless communication, each node can overhear the message broadcasted by other nodes in the transmission range. Every node locates randomly and moves randomly, which means the immediate neighboring nodes of any nodes are not known by each other without exchanging any messages. The network is rather dense so that a message in general could be overheard by multiple nodes. We assume that neither source node nor destination node is malicious and the adversary who plays black hole attack is an intermediate node. In addition, we assume there are one or more nodes that perform the black hole attack in the MANET. Moreover, a malicious node has knowledge of other malicious nodes' ID and is able to cooperate with these other malicious nodes. Table summarizes the simulation parameters for our simulation. One of the basic assumptions for the design of routing protocols in MANETs is that every node is honest and cooperative. That means, if a node claims it can reach another node by a certain path or distance, the claim is trusted/true; similarly, if a node reports a link break, the link will no longer be used.

Table - Simulation Parameters

Parameter	Value
Simulator	NS-2.34
MAC Layer Protocol	IEEE 802.11
Mobility Model	Random Way Point
Node Placement	Random Uniform
Terrain Range	1200 × 1200 m^2
Examined Protocol	AODV
Number of Mobile Nodes	25
Simulation Time	500 s
Channel Bandwidth	2 Mbps
Maximum Speed	10 – 500 m/s
Application Traffic	CBR
Packet Size	400 & 512 Bytes
Maximum Connection	29

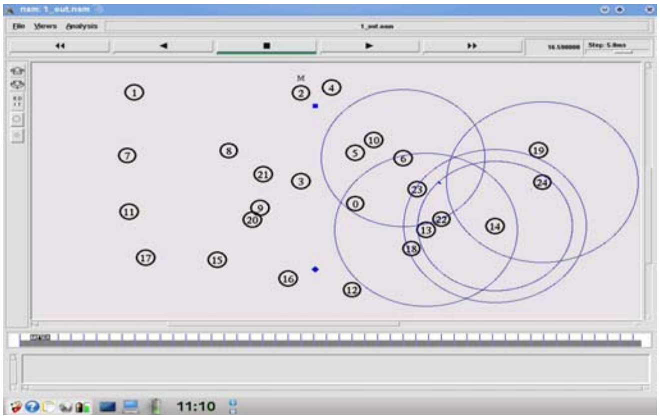

Fig. 1

While this assumption can fundamentally facilitate the design and implementation of routing protocols, it meanwhile introduces a vulnerability to several types of denial of service (DoS) attacks [4], particularly packet dropping attack. To launch such attack, a malicious node can stealthily drop some or all data or routing packets passing through it. Due to the lack of physical protection and reliable medium access mechanism, packet dropping attack represents a serious threat to the routing function in MANETs. A foe can easily join the network and compromise a legitimate node then subsequently start dropping packets that are

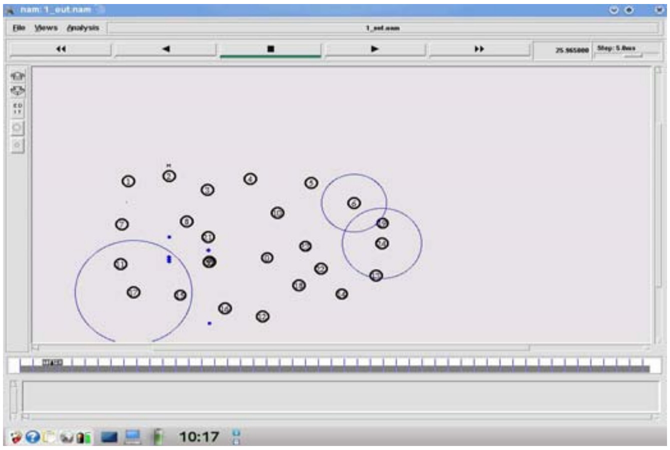

Fig. 2

Expected to be relayed in order to disrupt the regular communications consequently, all the routes passing through this Node fails to establish a correct routing path between the source and destination nodes. Figure 1 and 2 shows the results (snapshots) of our simulation which is performed with NS-2.34[7]. Different nodes are numbered which are written in circles. Blue circles show the coverage area of nodes. Blue Colored Square is packet drop from node. Node 2 is implemented as malicious node. So more packets are dropped by it. Figure 3 shows the packet drop by node when there is black hole attack in Mobile Adhoc Network. As packets are sent constantly, they will reach after some time delay to destination and some number of packets is drop between nodes. As mobility of node increase the packet dropping is also increase. In figure the packet received and drop for nodes for different mobility of node is shown.

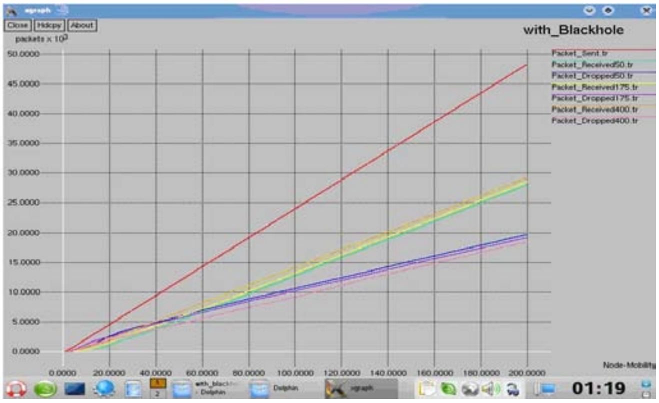

Fig. 3 : With Black hole

In the case when there is no black hole attack in Mobile Adhoc network, the performance is improved as shown in fig. 4. The packet dropping is very less as shown in figure.

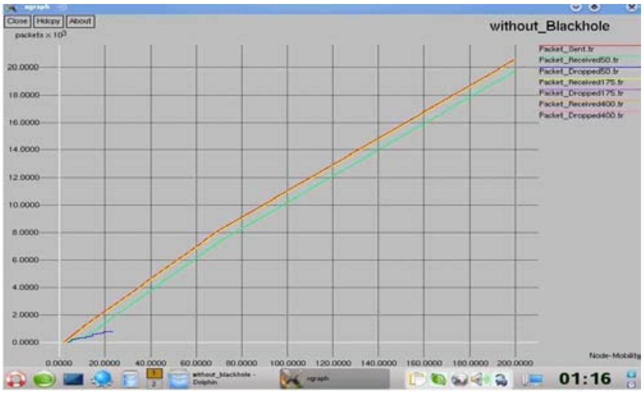

Fig. 4 : Without Black hole

V. CONCLUSION

In this paper we have presented of the state of the art on securing MANETs. The attack in Without Black hole and With Black hole attack schemes, as well as detection have been explored. A comparative study between them was then conducted to highlight their respective effectiveness and limitations. We concluded that the packet drop is more in MANET with black hole attack than without black hole attack. We believe it is an interesting and significant topic for further exploration with more evaluation of performance of MANET. As well as detection and prevention of black hole attack is also an area of future research.

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MTCMOS Design Methodologies and Charge Recycling Process

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Abstract - **MTCMOS** (Multi Threshold **CMOS**) technology provides a solution to the high performance and low power design requirements of modern designs. Low Vth and high Vth transistors are used in **MTCMOS** technology. Low Vth transistors are used to implement the desired functions. High Vth transistors are used to cut off the leakage current. The **MTCMOS** circuits ,however suffer from high energy overhead during the transitions between the active and stand by modes In this paper we (i) propose a new special flip flop which keeps a valid data during the sleep mode, (ii) develop a methodology which takes in to account the new design issues related to the **MTCMOS** technology. (iii).propose two adaptive **MTCMOS** schemes to address the growing leakage and delay spreads found in modern high performance designs. (IV) Propose a technique to lower the energy overhead during the transitions between the active and standby modes. The charge stored at the virtual lines is recycled during the active-to-sleep-to-active mode transitions with the proposed technique.

Keywords : MTCMOS, CPFF, energy recycling, gated power, gated ground, sleep switch, sub threshold leakage.

GJRE-F Classification : FOR Code: 900499

MTCMOSDESIGNMETHODOLOGIESANDCHARGERECYCLINGPROCESS

Strictly as per the compliance and regulations of:

MTCMOS Design Methodologies and Charge Recycling Process

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I. INTRODUCTION

In digital convergence era, Multi threshold CMOS is an important technology that provides high performance and low power operations by using both high and low threshold voltage transistors. MTCMOS technology is a very efficient technology for low power and high performance. However, MTCMOS has a serious problem that the stored data of latches and flip flops in logic blocks cannot be preserved when the power supply is turned off (sleep mode). Therefore extra circuits are provided for holding the stored data. This will effect the performance, area and the leakage current of the logic circuits in the sleep mode cannot be sufficiently suppressed. To avoid such undesirable leakage, Variable Threshold CMOS has been reported. Adaptive MTCMOS by using variable footer length is used for dynamic leakage and frequency control which was discussed in section 3.

A popular low leakage circuit technique is the multi threshold Voltage CMOS (MTCMOS). MTCMOS circuits selectively connect/disconnect the low threshold voltage (low-Vt) logic gates to/from the power supply or the ground via active/cut-off high threshold voltage (high-Vt) sleep transistors. This technique is also known as “power gating”. The power gating technique can be applied as either gated-ground or gated-VDD, as shown in fig 1.

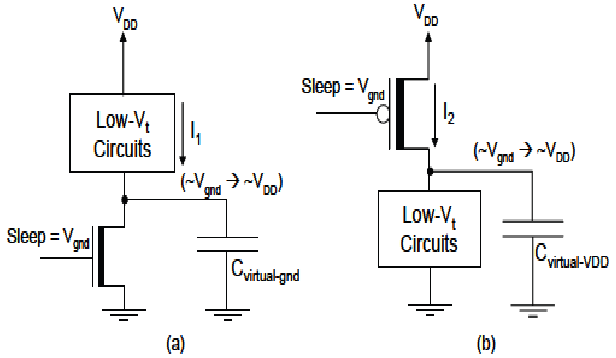

Fig.1 : MTCMOS circuits during the energy consuming mode transitions (a) Gated-ground circuit during the active-to-sleep mode transition. (b) Gated-V_{DD} circuits during the sleep-to-active mode transition. High V_t transistors are represented with a thick line in the channel region.

The leakage current produced by an MTCMOS circuit is significantly reduced by turning off the high-Vt sleep transistors in the standby mode. However, the active-to-sleep-to-active mode transitions consume a significant amount of additional energy in the conventional MTCMOS circuits. The energy dissipation occurs while charging and discharging the parasitic capacitances of the virtual lines and the sleep transistors. The virtual power and ground lines have high capacitance due to the wire parasitics, the large number of transistors sharing a common sleep transistor, and the decoupling capacitors attached to these supply rails for voltage stabilization against bouncing. Furthermore, the sleep transistors are typically large in size for satisfying the performance requirement, thereby further increasing the parasitic capacitance of the virtual lines. The energy consumed during the mode transitions is, therefore, significant in the standard MTCMOS circuits. In this paper, a new charge recycling MTCMOS circuit is proposed for low energy switching between the active and idle modes of operation.

This paper is organised as follows. Section 2 introduces MTCMOS design issues like the data preserving flip flop, the short circuit current due to

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floating inputs. Section 3 introduces adaptive MTCMOS by using variable footer strength for dynamic leakage and frequency control. Section 4 introduces the charge recycling MTCMOS circuit, Conclusions are offered in section 5.

II. PRELIMINARIES

a) The principles of the MTCMOS

The MTCMOS circuit technology can achieve a lower threshold voltage, and therefore higher performance as well as smaller standby leakage current. Basic circuit scheme of MTCMOS is shown in fig 2.

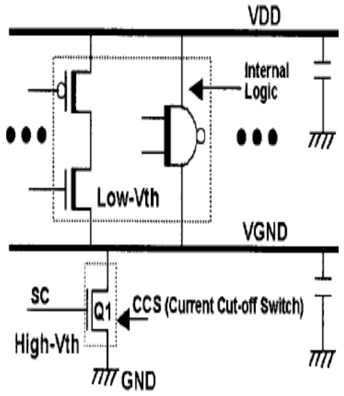

Fig 2 : Schematic Diagram of MTCMOS

The functional logic gates are implemented by using low V_{th} transistors that are powered by the supply line (VDD). A VGND is connected to the real ground line (GND) through a high Vth transistor switch Q1. MTCMOS designs have two operating modes, active and sleep. In sleep modes SC goes to low, and Q1 is turned off. In this state, the leakage current flows to GND through Q1. Due to its low leakage characteristic, the leakage current from the low V_{th} logic gates is almost completely suppressed. The high V_{th} transistor, Q1 acts as a switch that cuts off the leakage current from logic gates in sleep mode. Hence, it can be called as current cut off switch (CCS) The MTCMOS suffer from ground bounce which will decrease the performance or mal function. In order to avoid this channel width is increased but it increases the area and leakage current.

b) MTCMOS Design Issues

i. *Special cells for MTCMOS Design*

a. *Complementary Flip Flop (CPFF)*

MTCMOS is a very effective scheme that uses high V_{th} low leakage transistors to switch on and off the power supplies to low V_{th}, high speed logic blocks. However due to the lack of data preserve ability of standard latches and flip flops, extra circuits must be provided. These will degrade the performance, power and the area. The fig 3 gives the MTCMOS data preserving complimentary pass transistor flip flop.

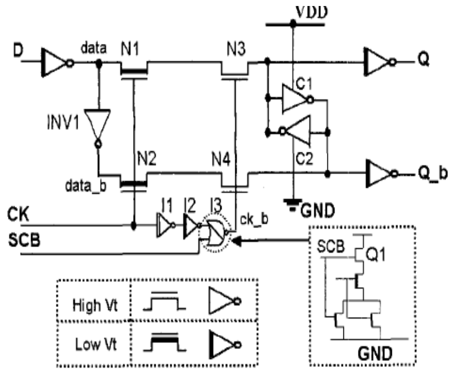

Fig3 : Complimentary Pass transistor Flip Flop(CPFF)

CPFF operates as follows:

Clock 'low': Since N1 and N2 are turned off and N3 and N4 are turned on, the static latch C1-2 holds the previous state. The new state on the complimentary inputs to the latch, **data** and **data_b** should be ready for sampling.

Clock 'High': At the rising edge of the clock, N1 and N2 are turned on while N3 and N4 stay on for a short interval that is determined by the delay of the inverter chain .During this interval data and data_b are passed through N1, N3 and N2, N4 respectively, and sampled in to the latch. After the short sampling interval, N3 and N4 are turned off, and Q and Q_b are decoupled from the data input.

Sleep mode: In the sleep mode SCB goes high, ck_b becomes low, and high Vth NMOS pass transistors, N3-4 are turned off so that the stored in C1-2 can be retained. At the transition from sleep mode to the active mode, SCB is set to low a little later than the power up. This delay prevents the destruction of data on the latch, C1-2 by delaying the turn on of N3-4 until the input data becomes valid.

c) Floating Input Induced Short-Circuit Current

Some of IPs like processors, memories may not be implemented by MTCMOS technology. These non-MTCMOS are directly powered by VDD and GND, and therefore vigilant even in the sleep mode. However, since the output nodes of all MTCMOS gates get floating as VGND gets floating in the sleep mode, the floating inputs to the vigilant IPs can cause very large short circuit current that flows from VDD to GND as shown in fig.4.

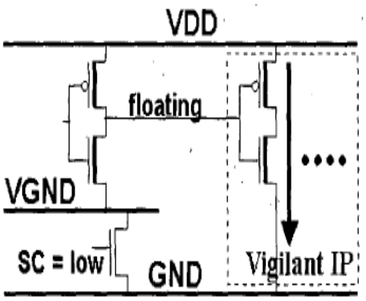

Fig .4 : Floating Input Induced Short-Circuit Current

To eliminate this leakage current, we insert a data holding circuit that is composed of a tri state buffer and a level holder at the output port of an MTCMOS logic gate which is the input to vigilant IP as shown in fig 5. This data holding circuit is a vigilant cell and called Floating prevention circuit.

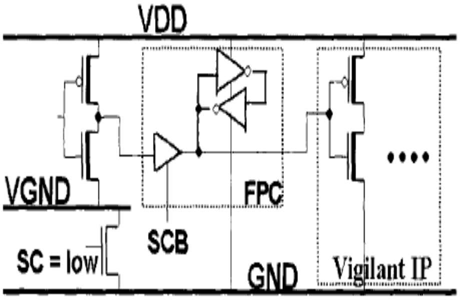

Fig 5 : Floating Prevention Circuit

III. ADAPTIVE MTCMOS

In a modern typical worst case design style, incorporating MTCMOS in to a design requires that the design still meet timing when the logic block is at the slow process corner. By incorporating process monitoring capability on the die, the strength of the footer device can be modulated to slow down dies that are not at the slow corner, representing the vast majority of parts. In doing so, the leakage power consumption of these nominal and fast dies is reduced. The key motivation behind the following two MTCMOS schemes is to enable simple methods of compensating for process variation.

a) Variable Gate Voltage MTCMOS

This design applies a variable gate to source voltage on the footer device shown in fig 6.

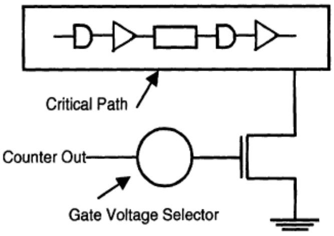

Fig. 6 : Block diagram of VGV-MTCMOS

If the process is tilted towards the fast corner, then the applied gate voltage on the footer device is lowered. Consequently, the amount of current that the device can sink is reduced, slowing down the circuit block to its nominal delay point. Moreover, since the footer device is now only weakly on, its resistance increases which then increases the average ground bounce on the virtual ground line. This rise in the average ground bounce reduces the leakage power consumption in the steady state devices in the circuit block.

When the process is tilted towards the slow corner, the footer device is fully turned on and the circuit block behaves as it would in the nominal base slower corner case.

b) Variable Width MTCMOS

The Variable width MTCMOS design uses several footer devices that can be turned on or off individually as shown in fig7.

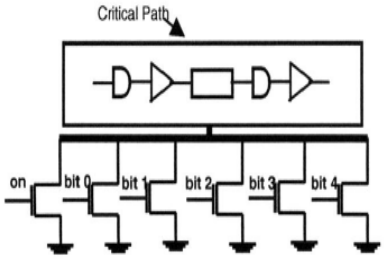

Fig 7 : Diagram of VW-MTCMOS

The Variable-Width MTCMOS (VW-MTCMOS) design incorporates several footer devices that can be turned on or off individually, as shown in fig 7. As the process tilts from one corner to the other, a different number of footers can be turned on or off to provide a varying level of current sinking capability. In standby mode, all footers are turned off as in the normal case for power gating.

For a die at the fast corner, the number of footers on during the active mode is decreased, reducing the pull down width. This reduces the current sinking capability of the footer and increases the delay of the circuit. At slow corner more footers will turn on and equivalent resistance is small between VGND and real GND.

Both GV-MTCMOS, VWMTCMOS reduces runtime leakage via the same ground bounce mechanism. As the process tilts towards the fast corner, the block becomes leakier due to shorter channel lengths and corresponding shifts in V_{th}. In this case, fewer footers are on, creating a greater resistance between the virtual ground and real ground lines which in turn raises the ground bounce. The rise in average ground bounce reduces the leakage of the block as described previously.

IV. CHARGE RECYCLING MTCMOS

A new low energy MTCMOS circuit technique based on charge recycling between the virtual power and ground lines is presented in this section. The technique is shown in fig 8. Both "gated-ground" and "gated-VDD" techniques are employed in a charge recycling MTCMOS circuit. Charge stored at the virtual ground and power lines are recycled through a high-Vt NMOS pass transistor during the mode transitions as shown in Fig. 8. The steady-state voltage difference between the virtual power and ground lines is close to VDD in both the active and the standby modes, thereby potentially producing a high sub threshold leakage current through the pass transistor.

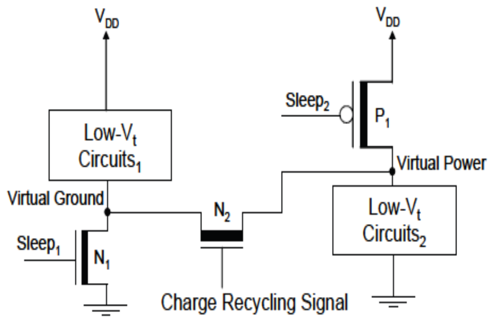

Fig 8 : The schematic of a charge recycling MTCMOS circuit. A pass transistor recycles charge between the virtual ground and power lines. High Vth transistors are represented with thick line in the channel region.

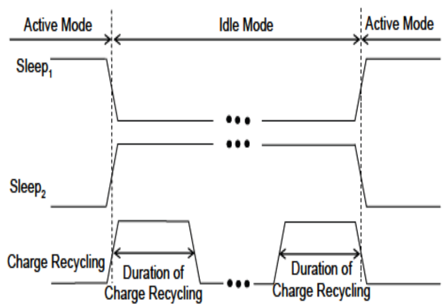

Fig 9 : The signal wave forms representing the operation of a charge recycling MTCMOS circuit during the mode transitions.

A charge recycling MTCMOS circuit operates as follows. In the active mode, the sleep transistors N1 and P1 are turned on. The pass transistor N2 is cut-off. The steady-state voltages of the virtual ground and virtual power lines are close to Vgnd and VDD, respectively. When the circuit enters the idle mode, the NMOS and PMOS sleep transistors (N1 and P1) are both cut off. The pass transistor is turned on for charge recycling. The node voltages at the beginning of the active-to-sleep mode transition are illustrated in Fig 9. Charge is transferred from the virtual power rail to the virtual ground rail through the pass transistor. The charge recycling process continues until the voltages of the virtual rails are equalized. Ilvt-1 and Ilvt-2 are higher than the leakage currents Ihvt-1 and Ihvt-2 produced by the NMOS and PMOS sleep transistors, respectively, until the steady state virtual rail voltages are reached. After the pass transistor is cut-off, therefore, the virtual ground line continues to be charged to a higher steady-state voltage by the leakage current (Ilvt-1) produced by the low-Vt circuitry1. Alternatively, the virtual power line is discharged to a lower steady-state voltage by the leakage current (Ilvt-2) produced by the low-Vt circuitry2. Since the pass transistor transfers a significant amount of charge from the virtual power line to the virtual ground line, the energy drawn from the power supply for charging the virtual ground line to ~VDD during the active-to- sleep mode transition ($E_{active\text{-}to\text{-}sleep}$) is reduced.

During the sleep-to-active mode transition, shortly before the sleep transistors are activated, the pass transistor is turned on as shown in fig 9. The pass transistor transfers charge from the virtual ground line to the virtual power line as shown in Fig. 11. There is a continuous current path through the low-Vt circuits1, the pass transistor, and the low-Vt circuits2 as illustrated in Fig. 11.

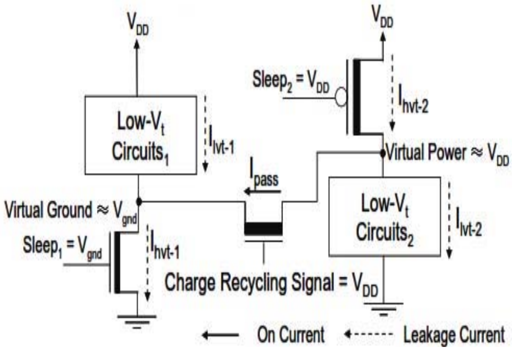

Fig. 10 : The charge recycling MTCMOS circuit at the beginning of the active-to-sleep mode transition. The pass transistor is turned on. High- V_t transistors are represented with a thick line in the channel region

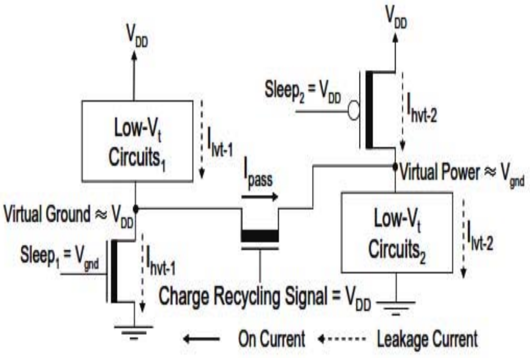

Fig. 11 : The charge recycling MTCMOS circuit at the end of the sleep mode. The pass transistor is turned on for charge recycling prior to the full reactivation of the circuit. High- V_t transistors are represented with a thick line in the channel region

After the charge recycling process is completed, the pass transistor is cut-off. The NMOS and PMOS sleep transistors are turned on for reactivating the circuit. The virtual ground line is discharged to a low voltage ($\approx V_{gnd}$) by the on-current of the high-V_t NMOS sleep transistor. Alternatively, the virtual power line is charged to a high voltage ($\approx$ VDD) by the active high-V_t PMOS sleep transistor. Since the pass transistor transfers a significant amount of charge from the virtual ground line to the virtual power line, the energy drawn from the power supply while charging the virtual power line to ~VDD for reactivating the circuit ($E_{sleep\text{-}to\text{-}active}$) is reduced.

The total energy overhead ($E_{overhead}$) due to a full cycle of mode transitions with a charge recycling MTCMOS circuit is

$$E_{\text{overhead}} = E_{\text{virtual rails}} + E_{\text{sleep transistor}} + E_{\text{pass transistor}}$$

$$E_{\text{virtual rails}} = E_{\text{active to sleep}} + E_{\text{sleep to active}}$$

The total energy overhead is significantly reduced with the proposed MTCMOS technique by suppressing $E_{virtual\text{-}rails}$ as compared to the $E_{virtual}$ consumed by the conventional MTCMOS circuits.

V. CONCLUSIONS

MTCMOS driven techniques such as the CPFF to preserve the data in the sleep mode, the FPC to prevent short circuit current are integrated in to the conventional design flow using the commercially available tools. Two new adaptive MTCMOS design techniques were introduced that reduce leakage and spread of delay. A new charge recycling circuit technique is presented for suppressing the energy overhead of mode transitions in MTCMOS circuits. The proposed technique employs both the "gated-ground" and the "gated-VDD" types of MTCMOS circuits. A pass transistor is utilized for charge recycling between the virtual power and ground lines at the beginning and shortly before the end of the sleep mode.

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