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A Pseudo-PMOS Logic for Realizing Wide Fan-in NAND Gates

By Sherif M. Sharroush
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Keywords: area, energy-delay product, power consumption, power-delay product, propagation delay, pseudo-PMOS logic, wide fan-in.

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Sherif M. Sharroush

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I. Introduction

MOS circuits that can be implemented using the universal NAND or NOR gates may contain a large number of serially connected NMOS or PMOS transistors if the fan-in is wide. Refer to Fig. 1 for such a wide fan-in logic circuit with *n* inputs realized in CMOS logic. The main problem associated with such circuits is the large propagation delay. This is due to the large *RC* time constant associated with charging or discharging the parasitic capacitances at the output node as well as the parasitic capacitances at the internal nodes. Also, the current-driving capability of the transistors degrades due to the reduction of their effective-gate voltages and their drain-to-source voltages in addition to the threshold-voltage increase due to the body effect. To make the matter worse, such gates when realized in logic-circuit families such as domino CMOS and pseudo NMOS suffer from the contention current, thus requiring a large area for the pull-down network (PDN) in order to have an acceptable noise margin and speed. Multi-input exclusive-OR gates that are required in applications such as parity-check and error-correction circuits or some built-in testing circuits and barrel-shifters [1] are types of applications that may include wide fan-in gates.

For realizing wide fan-in NOR gates, it is better to use the pseudo-NMOS logic-circuit family in which the long chain of the PMOS transistors is substituted by an always-activated PMOS transistor. In this paper, the pseudo-PMOS logic-circuit family is adopted in a similar manner in realizing wide fan-in NAND gates in which the long chain of the NMOS transistors is substituted by an always-activated NMOS transistor. The performance of this family is investigated and compared with the conventional CMOS logic. The remainder of this paper is organized as follows: A survey of the previous work related to the problem at hand is presented in Section II. The pseudo-PMOS logic is presented qualitatively in Section III. The circuit design issues and the comparison of this family with the conventional static CMOS realization are presented quantitatively in Section IV. The effects of the technology scaling and the process variations on this family are discussed in Sections V and VI, respectively. The enhancement in performance is verified by simulation in Section VII. Finally, the paper is concluded in Section VIII.

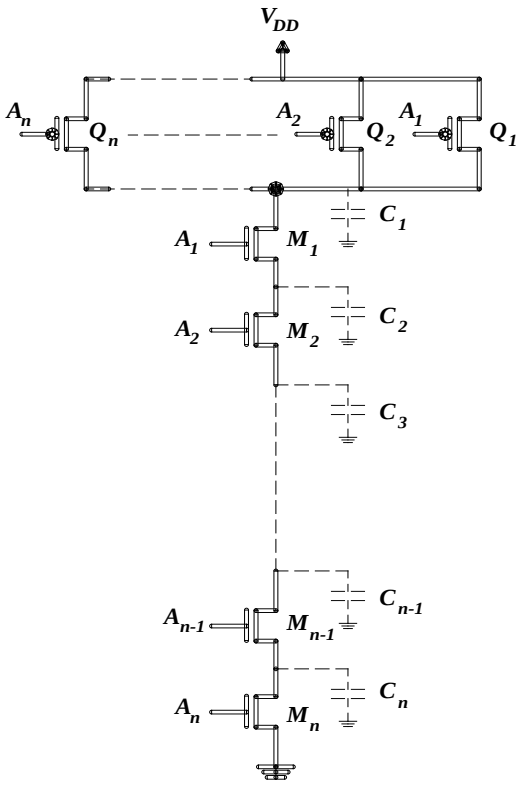

Fig. 1: An *n*-input NAND gate using the static complementary CMOS logic circuit family with the internal capacitances indicated.

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II. Previous Work

In this section, a review on some of the previous techniques for enhancing the performance of wide fan-in gates is presented. M. M. Khellah et al. [2] proposed a technique to lower both the dynamic-switching power consumption and the time delay of wide fan-in dynamic gates. This technique depends on generating a low swing signal at the output node by charging and discharging a small dummy capacitor. By virtue of the principle of charge sharing, a small swing is created on the gate output; finally, this swing is amplified to full rail using a suitable sense amplifier. Several techniques for reducing the power consumption of wide fan-in gates can be found in [3, 4, and 5]. Lowering the power consumption by reordering schemes is usually associated with a delay penalty as reordering is usually associated with a movement of the inputs that arrive lately farther away from the gate output.

A novel conditional isolation technique for reducing the evaluation time of wide fan-in domino gates was proposed by W. H. Chiu et al. [6]. This technique also reduces both the subthreshold and the gate-oxide leakage currents simultaneously. According to [6], reductions on total static power by 36%, dynamic power by 49.14%, and delay time by 60.27% compared to the conventional domino gate can be achieved. H. Mostafa et al. proposed adopting novel negative-capacitance circuits in order to reduce the delay variability under process variations [7]. According to this technique, the timing yield was improved from 50% to 100% for a 64-input wide dynamic OR gate at the expense of an excess power overhead.

In [8], K. Mohanram et al. proposed the reordering of the inputs exploiting the symmetry of the circuit with respect to their inputs in order to minimize the switching activity and hence the power consumption. An average reduction of 16% was achieved in power consumption using this scheme. This technique allows for a tradeoff between the complexity of the computation and the quality of the final output. Also, in order to reduce the glitching-power consumption, an extra dimension is added to the complexity of the problem (specifically, the pipelining) in order to obtain the inputs of the circuit at nearly the same instant. A. A George et al. achieved a better noise immunity and a reduced leakage current without any degradation in speed for wide fan-in domino gates by comparing the worst-case leakage current of the pull-up network (PUN) with a mirrored version of this current [9].

F. Moradi et al. proposed a technique that acts to enhance the performance of wide fan-in domino gates by employing a footer transistor that is initially off in the evaluation phase, thus reducing leakage [10]. Also, his proposed scheme reduces the contention between the keeper transistor and the PDN during the evaluation phase. K. Rajasri et al proposed a 256-bit comparator by adopting a novel technique called current-comparison domino circuit, thus reducing both the time delay and the leakage-power consumption [11]. Anamika et al. adopted the stacking effect to reduce the leakage-power consumption for wide fan-in circuits [12].

Finally, the reader is referred to [13 and 14] for techniques that depend on novel circuits having the same output as the conventional wide fan-in circuit but with improved performance. In the next section, the pseudo-PMOS logic is presented.

III. The Pseudo-PMOS Logic-Circuit Family

The idea of the pseudo-PMOS logic is simply as follows: It is well known from DeMorgan's law that

$$\overline{A_1 A_2 .... A_n} = \overline{A_1} + \overline{A_2} + ... + \overline{A_n} \qquad (1)$$

That is, logic "0" is obtained at the output of a circuit if all the inputs are at logic "1" and logic "1" is obtained at the output if any of the inputs is at logic "0." This can be implemented as well known by the series connection of NMOS transistors in the PDN and the parallel connection of PMOS transistors in the PUN. However, the right-hand side of Eq. (1) can be implemented simply using a parallel connection of PMOS transistors in the PUN. Now, refer to Fig. 2 for illustration of the pseudo-PMOS logic with *n* inputs.

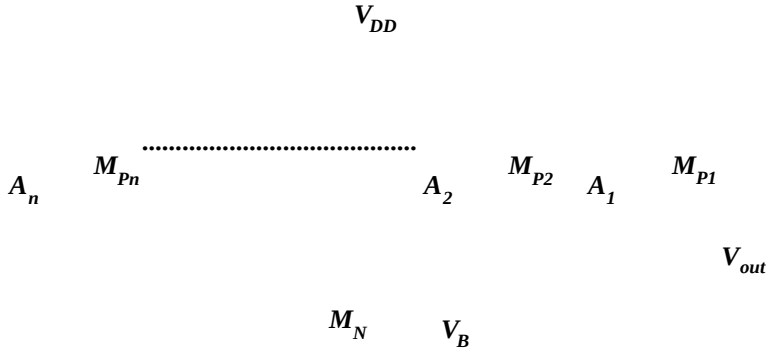

Fig. 2: The pseudo-PMOS logic for realizing wide fan-in NAND gates.

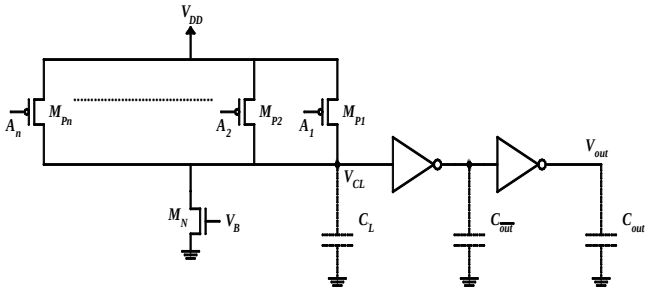

Fig. 3: The pseudo-PMOS logic with the use of two cascaded inverters.

If at least one of the inputs is deactivated, then the corresponding PMOS transistor will conduct. Due to the continuous conduction of the NMOS transistor, M_N, there is a voltage division between these two devices. The equivalent resistance of M_N can be adjusted by properly choosing the biasing voltage, V_B, or adjusting its strength through the aspect ratio, $(W/L)_n$, or the threshold voltage, V_{thn}.

Now, if all the inputs are activated, all the PMOS devices will be deactivated. Thus, the parasitic capacitance at the output node is discharged with no contention from the PMOS parallel network and the output is at logic "0" as it must be. The main advantage of the pseudo-PMOS logic is that increasing the number of the inputs merely increases the parasitic capacitance at the output node, thus not affecting the performance of this family significantly. On the other hand, increasing the number of the inputs in the CMOS logic has a significantly deleterious effect on its performance; a point that was discussed in the preceding section and is returned to in Section IV.

Instead of the application of a different biasing voltage, V_B, a voltage equal to the adopted power supply, V_{DD}, can be applied with either increasing the threshold voltage of M_N or lowering its aspect ratio to obtain a larger equivalent resistance at the lower arm of the voltage divider. Lowering the aspect ratio can be implemented by connecting multi transistors in series as the aspect ratio of the transistor equivalent to n serially connected transistors each with aspect ratio (W/L) is (W/nL) [15]. This is done in order to avoid the need to generate a separate voltage. An important note that is worth mentioning here is the proper choice of the threshold voltage of M_N, V_{thn}. Increasing this voltage, although certainly slows down the discharging process of C_L, makes the equivalent resistance of M_N larger. Thus, the output voltage resulting from the voltage division is larger with the result that the output-high level and consequently the logic swing is larger. Also, the low-to-high transition is faster. These contradictions are returned to in Sections IV and VII.

In order to resolve this contradiction, the scheme of Fig. 3 can be used in which two cascaded inverters were added. The benefits gained from adding these two inverters are to obtain a rail-to-tail voltage swing at the output and to reduce the rise and fall times of the output waveform. This in turn reduces the short-circuit power consumption in the driven stages. If the previously mentioned parameters are properly chosen, then the voltage at the input of the first inverter, V_{CL}, will be relatively high (larger than the threshold voltage of the first inverter, V_{thinv1}) in case only one input is deactivated. If more than one input is deactivated, then more than one PMOS device will be activated with the result that the equivalent resistance of the upper part of the voltage divider decreases. The result is that the voltage at the input of the first inverter becomes larger than that of the previous case and also the output voltage becomes at logic "1." The price paid, however, is the dc current drawn through the first inverter, the short-circuit power consumption of the two inverters, and the additional propagation delays of the two added inverters. Also, the change of V_{CL} with respect to the threshold voltage of the first inverter due to the process variations affects the reliability of the scheme; a point that is returned to in Section VI. *Throughout this paper, the scheme of Fig. 3 is adopted unless otherwise specified.* Note also that in order to inhibit the large power consumption in the standby state due to the continuous current drawn from V_{DD} to ground, the signal, V_B, must be connected to the standby signal. Thus, the path from V_{DD} to ground becomes open during the standby interval.

Two important notes are in order here. The first one is that the pseudo-PMOS logic family can be used in realizing any logic circuit with series or parallel connections in the PUNs or PDNs. In this case, the PUN is the same as that of the conventional CMOS logic. The pseudo-PMOS logic is obviously not suitable for realizing logic circuits containing serially connected PMOS transistors in their PUNs as it requires a significant area overhead. The second note is that the quantitative analysis of the next section can be applied equally well to the pseudo-NMOS logic after substituting the acronyms associated with the NMOS devices by those of the PMOS ones and vice versa.

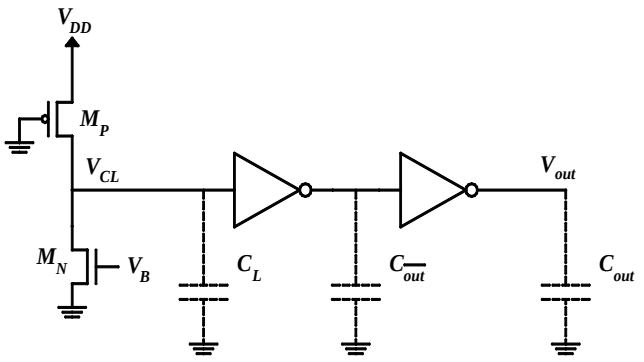

Fig. 4: The circuit schematic representing the worst-case scenario

IV. Circuit Design Issues

In this section, the circuit design issues of the pseudo-PMOS logic are discussed quantitatively from six aspects. The first one is the proper choice of the strength of the NMOS transistor, M_N, and the threshold voltage of the first inverter, V_{thinv1} (if used). The second, third, fourth, and fifth aspects concern the comparisons between the pseudo-PMOS logic and the conventional CMOS logic from the points of view of the area, the average propagation delay, the average power consumption, and the logic swing. Finally, a figure of merit that includes these metrics is defined and adopted in comparing the performance of the pseudo-PMOS logic and conventional CMOS logic.

a) The Proper Choice of the Strength of the NMOS Transistor

In determining the proper range for the values of V_{thinv1}, $(W/L)_n$, V_{thn}, and V_B, we adopt the worst-case scenario. The worst-case scenario is the assumption of only one deactivated input because it represents the minimum strength for the PMOS parallel combination and thus the highest equivalent resistance. If the pseudo-PMOS logic operates properly under this condition, it can be ensured to operate properly for all possible input combinations.

Refer now to Fig. 4 for this scenario. M_N operates in the saturation region for typical values of the adopted NMOS-transistor parameters in the worst case just described. Since V_{CL1}, the final steady-state voltage across C_L (the parasitic capacitance at the input of the first inverter), is chosen to be larger than V_{thinv1}, it is expected to be larger than $V_{DD}/2$. Thus, for the typical values of the PMOS-transistor parameters, M_P is expected to operate in the triode region as its V_D (drain voltage) is larger than its $V_G + |V_{thp}|$, where V_G and V_{thp} are the gate and threshold voltages of M_P, respectively. If the PMOS device is assumed to operate in the deep-triode region, then after equating the currents of the NMOS and PMOS devices in which the Shichman-Hodges square-law MOSFET model is adopted [16], we obtain

$$\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2(1+\lambda_n V_{CL1})=k_p'\left(\frac{W}{L}\right)_p(V_{DD}-|V_{thp}|)(V_{DD}-V_{CL1}) \quad (2)$$

where k_n', $(W/L)_n$, and V_{thn} are the process-transconductance parameter, the aspect ratio, and the threshold voltage of NMOS devices, and k_p', $(W/L)_p$, and V_{thp} are their PMOS counterparts. λ_n is the channel-length modulation effect parameter of NMOS devices. After simple mathematical manipulations, we readily obtain

$$V_{CL1}=\frac{k_p'\left(\frac{W}{L}\right)_p(V_{DD}-|V_{thp}|)V_{DD}-\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2\lambda_n+k_p'\left(\frac{W}{L}\right)_p(V_{DD}-|V_{thp}|)} \quad (3)$$

Alternatively, each of the NMOS and PMOS devices, M_N and M_P, can be replaced by its equivalent resistance. The equivalent resistance, R_{MP}, of M_P in the deep-triode region is [17]

$$R_{MP}=\frac{1}{k_p'\left(\frac{W}{L}\right)_p(V_{SG}-|V_{thp}|)}=\frac{1}{k_p'\left(\frac{W}{L}\right)_p(V_{DD}-|V_{thp}|)} \quad (4)$$

However, the equivalent resistance of M_N, let it be R_{MN}, can be written as the ratio between the average drain-to-source voltage and the average drain current, thus

$$R_{MN}=\frac{\frac{1}{2}(V_{CL1}+0)}{\frac{1}{2}\left[\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2(1+\lambda_n V_{CL1})+0\right]}=\frac{V_{CL1}}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2(1+\lambda_n V_{CL1})} \quad (5)$$

The voltage, V_{CL1}, can be found simply from the voltage division between R_{MN} and R_{MP} as follows:

$$V_{CL1}=\frac{R_{MN}V_{DD}}{R_{MN}+R_{MP}} \quad (6)$$

After substituting by R_{MN} and R_{MP} into Eq. (6), the expression for V_{CL1} can be obtained. Now, putting V_{CL1} larger than V_{thinv1} results in the following inequality (from which the strength of the NMOS device can be determined):

$$\frac{k_p'\left(\frac{W}{L}\right)_p(V_{DD}-|V_{thp}|)V_{DD}-\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2\lambda_n+k_p'\left(\frac{W}{L}\right)_p(V_{DD}-|V_{thp}|)}>V_{thinv1} \quad (7)$$

V_{thinv1} in turn can be evaluated from [17]

$$V_{thinv1}=\frac{\sqrt{\frac{k_p'\left(\frac{W}{L}\right)_{p1}}{k_n'\left(\frac{W}{L}\right)_{n1}}}\left[V_{DD}-|V_{thp1}|\right]+V_{thn1}}{1+\sqrt{\frac{k_p'\left(\frac{W}{L}\right)_{p1}}{k_n'\left(\frac{W}{L}\right)_{n1}}}} \quad (8)$$

where $(W/L)_{n1}$, $(W/L)_{p1}$, V_{thn1}, and V_{thp1} are the aspect ratios and the threshold voltages of the constituting NMOS and PMOS transistors of the first inverter, respectively.

Before leaving this subsection, an important note follows: It is obvious from the qualitative discussion of the pseudo-PMOS logic that increasing the strength of the NMOS device, M_N, causes the low-to-high and the high-to-low propagation delays to increase and decrease, respectively, i.e. to change in opposite directions. Thus, it can be concluded that there is an optimum value for the parameters determining this strength such as the threshold voltage and the aspect ratio at which the average propagation delay is at its minimum. This is really the case and this point is confirmed in Subsection C.

b) The Area Comparison

In comparing the areas of the pseudo-PMOS logic with the CMOS logic, we adopt the approximation that the area of a certain transistor is equal to its channel area [17]. Adopting the convention that the size of the PMOS transistor is twice that of the NMOS one in order to compensate for the mobility difference and that each of the n NMOS transistors in the series connection has an aspect ratio of n in order to compensate for the degradation in delay [17], then the areas of the conventional and the proposed logic-circuit families, A_c and A_p, can be approximated by

$$A_c = WL(n^2 + 2n) \tag{9}$$

$$A_p = (2n+7)WL \tag{10}$$

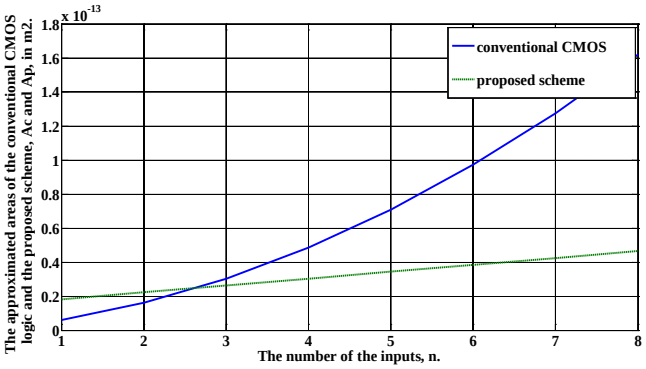

Fig. 5: The plots of the approximated areas of the CMOS logic and the pseudo-PMOS logic versus the number of the inputs.

The plots of A_c and A_p versus n for $W = L = 45$ nm are shown in Fig. 5. It can be concluded from this rough estimation of the area that the area overhead of the two-cascaded inverters is justified when the number of the inputs exceeds 2. Had we adopted the version of Fig. 2 for the pseudo-PMOS logic, the area of this family would have been smaller than that of the CMOS logic for all values of n.

c) The Average Propagation-Delay Comparison

The average propagation delay according to the pseudo-PMOS logic is defined as

$$t_{pavgp} = \frac{t_{PLHp} + t_{PHLp}}{2} \tag{11}$$

where t_{PLHp} and t_{PHLp} are the low-to-high and the high-to-low propagation delays according to the pseudo-PMOS logic, respectively. To determine t_{PLHp}, refer to the circuit shown in Fig. 4. This circuit represents the worst case from the point of view of the delay also as the charging current of C_L is the smallest one and thus the estimated value of t_{PLHp} is the largest one. The time delay, t_{PLHp}, contains there subcomponents, t_{PLHp1}, t_{PLHp2}, and t_{PLHp3}, respectively. These are the time delays required to precharge C_L to a certain steady-state value that depends on the relative strengths of the activated PMOS device and the always activated NMOS device, the high-to-low propagation delay of the first inverter, and the low-to-high propagation delay of the second inverter, respectively. The first subcomponent can be approximated by [17]

$$t_{PLHp1} = \frac{C_L \Delta V_{CL}}{i_{chavg}} \tag{12}$$

where ΔV_{CL} is the voltage change of V_{CL} and i_{chavg} is the average charging current of C_L. To determine C_L, we adopt the assumption that the aspect ratio of the PMOS device is twice that of the NMOS one in order to compensate for the difference in their mobilities and assume that the parasitic capacitance associated with each terminal of the minimum-sized NMOS transistor is C [18], then C_L can be approximated as

$$C_L = \left[3 + 2n + \left(\frac{W}{L}\right)_n\right] C \tag{13}$$

where $(W/L)_n$ is the aspect ratio of M_N. ΔV_{CL} is equal to $0.5V_{CL1}$ (adopting the 50% criterion) and i_{chavg} can be found from

$$i_{chavg} = i_{MPavg} - i_{MNavg}\,, \tag{14}$$

where i_{MPavg} and i_{MNavg} are the average currents of M_P and M_N, respectively. The last two currents can be found as follows:

$$i_{MPavg} = \frac{i_{MP}(atV_{CL} = 0) + i_{MP}(atV_{CL} = V_{CL1})}{2} \tag{15}$$

$$\therefore i_{MPavg} = \frac{1}{2}\left[\frac{1}{2}k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)^2(1 + \lambda_p V_{DD}) + k_p'\left(\frac{W}{L}\right)_p \left[(V_{DD} - |V_{thp}|)(V_{DD} - V_{CL1}) - \frac{1}{2}(V_{DD} - V_{CL1})^2\right]\right] \tag{16}$$

i_{MNavg} is given by

$$i_{MNavg} = \frac{i_{MN}(atV_{CL} = 0) + i_{MN}(atV_{CL} = V_{CL1})}{2} \tag{17}$$

$$\therefore i_{MNavg} = \frac{1}{4} k_n' \left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 (1 + \lambda_n V_{CL1}). \quad (18)$$

Substituting by these two currents into Eqs. (12) and (14) results in

$$t_{PLHp1} = \frac{\left[3 + 2n + \left(\frac{W}{L}\right)_n\right] C(0.5 V_{CL1})}{\frac{1}{2}\left[\frac{1}{2} k_p' \left(\frac{W}{L}\right)_p \left(V_{DD} - |V_{thp}|\right)^2 (1 + \lambda_p V_{DD}) + k_p' \left(\frac{W}{L}\right)_p \left[\left(V_{DD} - |V_{thp}|\right)(V_{DD} - V_{CL1}) - \frac{1}{2}(V_{DD} - V_{CL1})^2\right]\right] - \frac{1}{4} k_n' \left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 (1 + \lambda_n V_{CL1})} \quad (19)$$

The other two subcomponents are given by

$$t_{PLHp2} = \frac{C_{\overline{out}} \Delta V_{\overline{out}}}{i_{avg}} \quad (20)$$

where $C_{\overline{out}}$, $V_{\overline{out}}$, and i_{avg} are the parasitic capacitance at the output of the first inverter, the voltage at the output of the first inverter, and the average discharging current of $C_{\overline{out}}$, respectively. Keeping in mind that the logic "1" feeding the first inverter is V_{CL1}, then

$$i_{avg} = \frac{1}{4} k_n' \left(\frac{W}{L}\right)_{n1} (V_{CL1} - V_{thn1})^2 (1 + \lambda_n V_{DD}) \quad (21)$$

$C_{\overline{out}}$ and $V_{\overline{out}}$ are equal to 6C and V_{DD}, respectively. So,

$$t_{PLHp2} = \frac{6 C V_{DD}}{\frac{1}{4} k_n' \left(\frac{W}{L}\right)_n (V_{CL1} - V_{thn})^2 (1 + \lambda_n V_{DD})} \quad (22)$$

t_{PHLp3} is given by [17]

$$t_{PLHp3} = \frac{2 C_{out}}{k_p' \left(\frac{W}{L}\right)_p \left(V_{DD} - |V_{thp}|\right)} \left[\frac{|V_{thp}|}{V_{DD} - |V_{thp}|} + \frac{1}{2} \ln\left(\frac{3V_{DD} - 4|V_{thp}|}{V_{DD}}\right)\right] \quad (23)$$

C_{out} is the parasitic capacitance at the output of the second inverter and is given by 3C + C_{fan}, where C_{fan} is the parasitic capacitance due to the fan-out.

Now, t_{PHLp} contains three subcomponents also; t_{PHLp1}, t_{PHLp2}, and t_{PHLp3} which are the time delays required to discharge C_L from V_{CL1} to 0 V, the low-to-high propagation delay of the first inverter, and the high-to-low propagation delay of the second inverter, respectively. t_{PHLp1} can be found from

$$t_{PHLp1} = \frac{C_L \Delta V_{CL}}{i_{disavg}} \quad (24)$$

where i_{disavg} is the average discharging current through M_N and is given by

$$i_{disavg} = \frac{i_{MN}(at V_{CL} = V_{CL1}) + i_{MN}(at V_{CL} = 0)}{2} \quad (25)$$

$$\therefore i_{disavg} = \frac{1}{4} k_n' \left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 (1 + \lambda_n V_{CL1}) \quad (26)$$

So, t_{PHLp1} is given by

$$t_{PHLp1} = \frac{2 C_L V_{CL1}}{k_n' \left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 (1 + \lambda_n V_{CL1})} \quad (27)$$

t_{PHLp2} and t_{PHLp3} were estimimted in [17] and were found to be respectively.

$$t_{PHLp2} = \frac{2 C_{\overline{out}}}{k_p' \left(\frac{W}{L}\right)_p \left(V_{DD} - |V_{thp}|\right)} \left[\frac{|V_{thp}|}{V_{DD} - |V_{thp}|} + \frac{1}{2} \ln\left(\frac{3V_{DD} - 4|V_{thp}|}{V_{DD}}\right)\right] \quad (28)$$

and

$$t_{PHLp3} = \frac{2 C_{out}}{k_n' \left(\frac{W}{L}\right)_n (V_{DD} - V_{thn})} \left[\frac{V_{thn}}{V_{DD} - V_{thn}} + \frac{1}{2} \ln\left(\frac{3V_{DD} - 4V_{thn}}{V_{DD}}\right)\right] \quad (29)$$

As discussed in Subsection A and illustrated in Figs. 6 and 7, there is an optimum value for the aspect ratio and the threshold voltage of M_N at which t_{pavgp} is at its minimum. Figs. 6 and 7 show the plots of the average propagation delay of the pseudo-PMOS logic versus the aspect ratio and the threshold voltage of M_N, respectively, according to the scheme of Fig. 3 with V_{thn} = 0.25 V, V_{thp} = -0.32 V, V_{DD} = 0.8 V, and C = 1 fF. As shown in these two figures, the optimum average propagation delay occurs at $(W/L)_n$ and V_{thn} equal to 5.2 and 0.58 V, respectively.

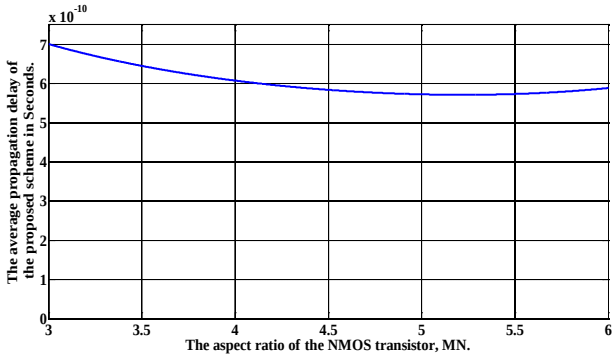

Fig. 6: The plot of the average propagation delay of the pseudo-PMOS logic versus the aspect ratio of M_N, $(W/L)_n$.

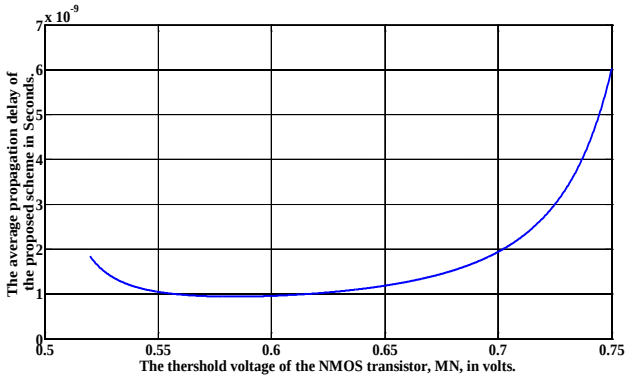

Fig. 7: The plot of the average propagation delay of the pseudo-PMOS logic versus the threshold voltage of M_N, V_{thn}.

Now, refer to Fig. 8 for the plots of the average propagation delay versus the number of the inputs according to the analysis and the simulation results adopting the scheme of Fig. 2 and estimating the time delays up to the 50% point.

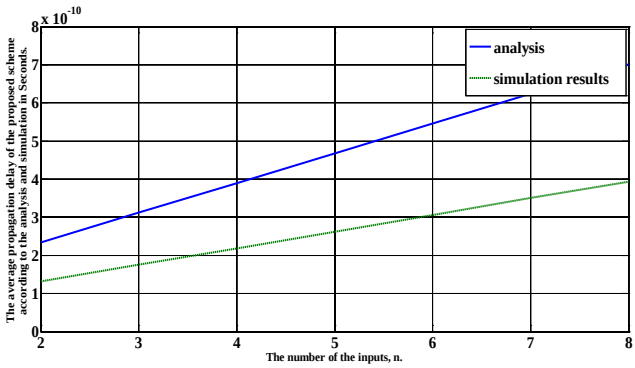

Fig. 8: The average propagation delay versus the number of the inputs according to the analysis and the simulation results.

Now, the average propagation delay according to the CMOS logic, t_{pavgc}, can also be defined in a similar way as the average of the low-to-high and the high-to-low propagation delays, t_{PLHc} and t_{PHLc}, respectively, as follows:

$$t_{pavgc} = \frac{t_{PLHc} + t_{PHLc}}{2} \tag{30}$$

Toward a simplified evaluation for these two time delays, each NMOS and PMOS transistor in the CMOS-logic circuit is represented by an equivalent resistance, R_N and R_P, respectively. In [19], approximate expressions for the equivalent resistances of the NMOS and PMOS transistors are:

$$R_N = \frac{\alpha_n}{\left(W/L\right)_n} \tag{31}$$

and

$$R_P = \frac{\alpha_p}{\left(W/L\right)_p} \tag{32}$$

respectively, where α_n and α_p are process-dependent parameters for the NMOS and PMOS devices, respectively. Simulation results reveal that the best estimates for α_n and α_p are 2.5 Ωk and 18 kΩ, respectively, for the 45 nm CMOS technology. We adopt the worst case in estimating the low-to-high propagation delay in that only one input is assumed to be at logic "0" and corresponds to the lowermost NMOS transistor so that all the internal capacitances will be charged. Applying Elmore's delay formula [20 and 21] to the conventional CMOS circuit shown in Fig. 1 results in the following estimations for t_{PLHc} and t_{PHLc}:

$$t_{PLHc} = (\ln 2)\left[R_P C_1 + (R_P + R_N)C_2 + (R_P + 2R_N)C_3 + ... + (R_P + (n-1)R_N)C_n\right] \tag{33}$$

and

$$t_{PHLc} = (\ln 2)\left[nR_N C_1 + (n-1)R_N C_2 + (n-2)R_N C_3 + ... + R_N C_n\right] \tag{34}$$

According to the estimation of the parasitic capacitances adopted in this paper, we have: $C_1 = C_{fan} + 3nC$, $C_2 = C_3 = ... = C_n = 2nC$. After substituting for the values of these capacitances into Eqs. (33) and (34), we obtain

$$t_{PLHc} = (\ln 2)\left[R_P C_{fan} + n(2n+1)R_P C + n^2(n-1)R_N C\right] \tag{35}$$

and

$$t_{PHLc} = (\ln 2)R_N\left[nC_{fan} + n^2(n+2)C\right] \tag{36}$$

d) The Average Power-Consumption Comparison

The average power consumption is the average of the power consumptions in cases of low-to-high and high-to-low transitions. The power consumption of the pseudo-PMOS logic contains the static and the dynamic power components. The static-power consumption is that associated with the first inverter due to the activation of its two devices in case of low-to-high transition and due to the current drawn through the activated PMOS devices and the always activated NMOS device, M_N, in case of low-to-high transition also. The input voltage of the first inverter certainly depends on the number of the activated inputs. So, we, in order to simplify the dc-power estimation, assume that the first-inverter's input is at $V_{DD}/2$ and that this inverter is matched so that its output will also be at $V_{DD}/2$. The estimated dc-power consumption according to this evaluation is certainly overestimated as the dc current of the first inverter is at its maximum when the inverter's

input is at $V_{DD}/2$ [17]. Thus, the range of the number of the inputs over which the pseudo-PMOS logic is better than the CMOS logic is expected to be larger than that estimated. In case of low-to-high transition, the dc current of the first inverter is (where LH indicates low-to-high transition)

$$I_{DCLH}=\frac{1}{2}k_n^{'}\left(\frac{W}{L}\right)_n\left(\frac{V_{DD}}{2}-V_{thn}\right)^2\left(1+\lambda_n\frac{V_{DD}}{2}\right) \quad (37)$$

The dc-power consumption of the first inverter in the low-to-high transition is thus

$$P_{DCLH1}=\frac{V_{DD}}{2}k_n^{'}\left(\frac{W}{L}\right)_n\left(\frac{V_{DD}}{2}-V_{thn}\right)^2\left(1+\lambda_n\frac{V_{DD}}{2}\right) \quad (38)$$

Similarly, the dc-power consumption through M_N can be written as

$$P_{DCLH2}=\frac{V_{DD}}{2}k_n^{'}\left(\frac{W}{L}\right)_n(V_B-V_{thn})^2(1+\lambda_nV_{CL1}) \quad (39)$$

In the other case (high-to-low transition), all the inputs are activated with the result that all the PMOS devices in the parallel connection become equivalent to an open circuit. So, there is no dc power consumption in this transition (HL indicates high-to-low transition),

$$i_{DCHL}=0 \quad (40)$$

$$P_{DCHL}=0 \quad (41)$$

The average dc power consumption is thus

$$P_{DC}=\frac{P_{DCLH}+P_{DCHL}}{2}=\frac{V_{DD}}{4}k_n^{'}\left(\frac{W}{L}\right)_n\left[\left(\frac{V_{DD}}{2}-V_{thn}\right)^2\left(1+\lambda_n\frac{V_{DD}}{2}\right)+(V_B-V_{thn})^2(1+\lambda_nV_{CL1})\right] \quad (42)$$

The average dynamic-switching power consumption is the average of that associated in cases of low-to-high and high-to-low transitions. In case of worst-case low-to-high transition, all except one of the inputs are activated, thus the dynamic-switching power consumption associated with the charging of the parasitic capacitances at the input of the first inverter, the output of the second inverter, and the gate terminals can be written as

$$P_{dLHp}=\alpha fV_{DD}^2C_{out}+\alpha fV_{DD}V_{CL1}C_L+\alpha fV_{DD}^2[2(n-1)]C \quad (43)$$

where α is the switching activity and f is the frequency of operation. The corresponding value in case of high-to-low transition is

$$P_{dHLp}=\alpha fV_{DD}^2C_{\overline{out}}+\alpha fV_{DD}^2(2n)C \quad (44)$$

Thus, the average dynamic-switching power consumption associated with the parasitic capacitances at the previously mentioned nodes is

$$P_{davgp}=\frac{P_{dLHp}+P_{dHLp}}{2} \quad (45)$$

Note that all these capacitances have the same switching activities and the same frequencies of operation. The second type of the dynamic-power consumption is the short-circuit power consumption associated with the two inverters, P_{sc1avg} and P_{sc2avg}. Assuming that the two inverters are matched, then the average short-circuit power consumption is [21]

$$P_{scavg1}=\frac{\alpha k_n^{'}\left(\frac{W}{L}\right)_n\tau_1f(V_{DD}-2V_{thn})^3}{12} \quad (46)$$

where τ_1 is the rise or fall time of the voltage that feeds the first inverter and is equal to twice the average of the low-to-high and the high-to-low propagation delays at the input of the first inverter. P_{scavg2} can be written as

$$P_{scavg2}=\frac{\alpha k_n^{'}\left(\frac{W}{L}\right)_n\tau_2f(V_{DD}-2V_{thn})^3}{12} \quad (47)$$

where τ_2 is the rise or fall time of the voltage that feeds the second inverter and is equal to twice the average of the low-to-high and the high-to-low propagation delays at the input of the second inverter. Certainly, the short-circuit power consumption is zero in case V_{DD} is smaller than $V_{thn} + |V_{thp}|$ as there is no time interval during which both the NMOS and PMOS devices conduct simultaneously [21].

The average dynamic-switching power consumption of the CMOS logic is also taken as the average of that in cases of low-to-high and high-to-low transitions. Adopting the worst case in case of low-to-high transition (illustrated in Subsection C), the power required to charge the internal capacitances at the gate terminals as well as at the internal nodes is

$$P_{dLHc}=\alpha fV_{DD}^2[2C(n-1)+nC(n-1)]+\alpha fV_{DD}^2[C_1+C_2+...+C_n]_{.}=\alpha fV_{DD}^2\left[C_{fan}+3nC+C(n-1)(3n+2)\right] \quad (48)$$

During the high-to-low transition, all the inputs are activated and thus the associated power consumption is

$$P_{dHLc}=\alpha fV_{DD}^2\left(n^2C+2nC\right) \quad (49)$$

e) The Logic Swing

The logic swing, *LS*, at the output node is simply equal to the difference between the output high and low levels. Since C_L is discharged to 0 V with no contention from the PMOS device, *LS* is equal to V_{CL1}. Refer to Fig. 9 for the plots of *LS* versus V_{thn} according to the analysis and the simulation results (of Fig. 2). Certainly, the logic swing of the CMOS logic is V_{DD}.

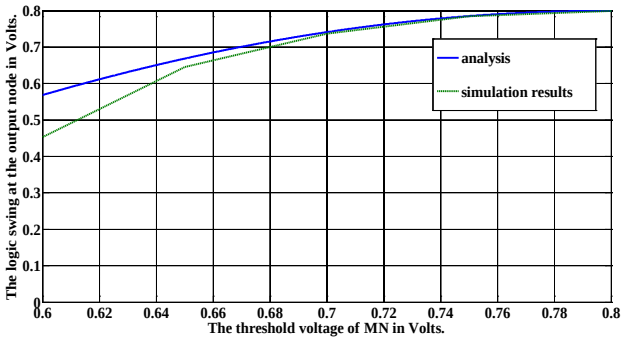

Fig. 9: The change of the logic swing with the threshold voltage of M_N, V_{thn}, according to the analysis and the simulation results.

f) The Figure of Merit

In order to evaluate the performance of the pseudo-PMOS logic compared to the CMOS logic, we define a figure of merit, *FOM*, that includes the four previously estimated metrics; the area, the average propagation delay, the average power consumption, and the logic swing. Since these four metrics are preferred to be at their minimum except the logic swing which is preferred to be at its maximum, the *FOM* is defined as follows according to the conventional and proposed logic-circuit families:

$$FOM_c = \frac{LS_c}{A_c t_{avgc} P_{avgc}} \tag{50}$$

and

$$FOM_p = \frac{LS_p}{A_p t_{avgp} P_{avgp}} \tag{51}$$

respectively. Thus, the larger the *FOM*, the better the performance will be. Refer to Figs. 10, 11, and 12 for the plots of the figures of merit of the CMOS logic and the pseudo-PMOS logic according to the version of Fig. 2 versus *n*, *f*, and V_{DD}, respectively. The parameters adopted with these plots are $n = 8$, $C_{fan} = 10$ fF, and $f = 10$ MHz. As shown, the performance of the pseudo-PMOS logic is better than that of the CMOS logic when *n* exceeds 8. This can be attributed to the degradation of the performance of the CMOS logic when *n* exceeds this value due to the limitations discussed in Section I. However, the matter is not that bad with the pseudo-PMOS logic as mentioned in Section III in which the degradation is merely due to the increased number of the PMOS transistors and the associated parasitic effects at the output node. The same can be said about Fig. 11 in which the performance of the conventional CMOS logic degrades faster than that of the pseudo-PMOS logic with increasing *f*. This is certainly due to the need to deal with numerous parasitic capacitances in the conventional CMOS-logic realization. According to Fig. 11, the pseudo-PMOS logic is better than the conventional CMOS when *f* exceeds 15 MHz. According to Fig. 12, it is apparent that the pseudo-PMOS logic exhibits an optimum behavior versus V_{DD} due to the obvious conflictions associated with changing V_{DD} with the optimum performance occurring at $V_{DD} = 0.7685$ V. Specifically, increasing V_{DD} enhances the logic swing and the propagation delay; however, at the expense of worsening the power consumption. In a nutshell, the pseudo-PMOS logic has a smaller area and average propagation delay but larger power consumption and slightly smaller noise margin compared with the CMOS logic.

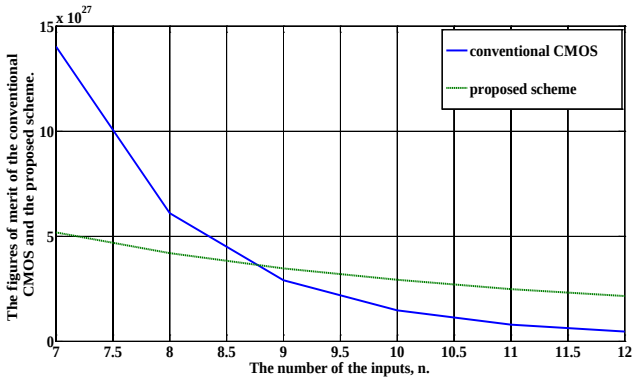

Fig. 10: The plots of FOM_c and FOM_p versus the number of the inputs, *n*.

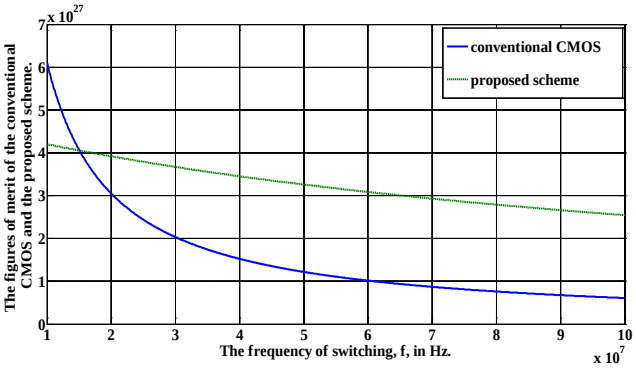

Fig. 11: The plots of FOM_c and FOM_p versus the frequency of switching, *f*.

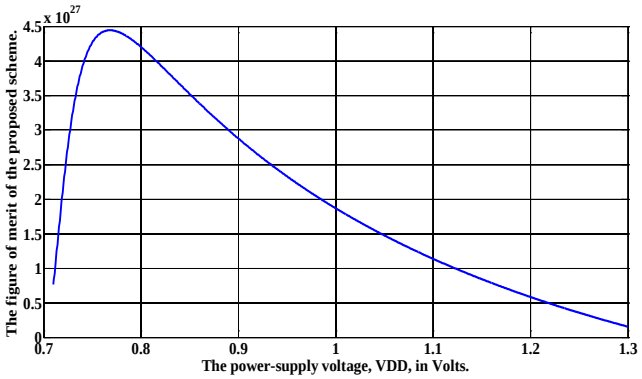

Fig. 12: The plot of FOM_p versus the power-supply voltage, V_{DD}.

V. Effect of Technology Scaling

In this section, the effect of technology scaling on the pseudo-PMOS logic is investigated. The following effects are investigated: velocity saturation, mobility degradation, reduction of the V_{DD}/V_{thn} ratio, increased process variations, and channel-length modulation.

a) Velocity Saturation and Mobility Degradation

These two effects act to reduce the current of the MOS transistor for the same applied voltages. Thus, the time required to develop a certain voltage at the first-inverter input or at the output of the circuit increases. However, this effect is common in both the CMOS logic and the pseudo-PMOS logic. It must be noted that the mobility-degradation effect is more pronounced in NMOS transistors compared to PMOS ones. Thus, the sizing of the PMOS transistors is expected to decrease with technology scaling. Since most of the area of the pseudo-PMOS logic is due to the PMOS network, the area advantage becomes more pronounced.

b) Reduction of the V_{DD}/V_{thn} Ratio

Due to the performance degradation with reducing V_{DD}, V_{thn} also reduces with technology scaling but at a smaller rate, thus the ratio, V_{DD}/V_{thn}, is expected to decrease with technology scaling. This has the effect of reducing the short-circuit power consumption which enhances the performance of the pseudo-PMOS logic.

c) Increased Process Variations

The effect of the process variations increases with technology scaling. This has the effect of narrowing the range within which the threshold voltage of the first inverter lies for the proper operation of the pseudo-PMOS logic. This seems to be the most important degradation associated with the pseudo-PMOS logic as it reduces its reliability if the version of Fig. 3 were used. This effect, however, has no counterpart in the CMOS logic.

d) The Channel-Length Modulation Effect

The Early voltage modeling the dependence of the drain current on the drain-to-source voltage is proportional to the channel length [17]. So, it decreases with technology scaling with the result that the drain current increases. This effect is more pronounced in the CMOS logic due to the division of the voltage across the stacked devices which has no counterpart in the pseudo-PMOS logic. Also, the slope of the voltage-transfer characteristics of the inverters in the transition region decreases. So, for a certain difference that is developed at the inverter input, there is a smaller value for the logic swing at the inverter output. This indicates that a smaller propagation delay is associated with the two cascaded inverters.

VI. Effect of Process Variations

In this section, the effect of the process variations on the reliability of the pseudo-PMOS logic is investigated quantitatively. Specifically, the variations of the aspect ratio and the threshold voltage of the NMOS and PMOS devices composing the voltage divider are taken into account with their effects on the first inverter's input voltage quantified. The equation describing the voltage at the input of the first inverter was derived in Section IV and is repeated here for convenience as follows:

$$V_{CL1} = \frac{k_p'\left(\frac{W}{L}\right)_p \left(V_{DD} - |V_{thp}|\right) V_{DD} - \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 \lambda_n + k_p'\left(\frac{W}{L}\right)_p \left(V_{DD} - |V_{thp}|\right)} \quad (52)$$

Let the variation in the aspect ratio of the NMOS device be $\Delta(W/L)_n$, then after substituting $(W/L)_n$ by $(W/L)_n + \Delta(W/L)_n$ into Eq. (52), neglecting the terms containing $(\Delta(W/L)_n)^2$, using the approximation

$$\frac{1}{1+x} \approx 1 - x \text{ for } x << 1 \quad (53)$$

and performing some algebraic manipulations, we get the percentage variation of the voltage, V_{CL1}, due to the change of $(W/L)_n$ (let it be $\Delta V_{CL11}/V_{CL1}$) as shown in Eq. (54).

The percentage variations of V_{CL1} due to each of ΔV_{thn}, $\Delta(W/L)_p$, and ΔV_{thp} can be evaluated in a similar manner and shown to be (let them be $\Delta V_{CL12}/V_{CL1}$, $\Delta V_{CL13}/V_{CL1}$, and $\Delta V_{CL14}/V_{CL1}$, respectively) as shown in Eqs. (55), (56) and (57).

Refer to Figs. 13, 14, 15, and 16 for the plots of the percentage variations of V_{CL1} due to that in $(W/L)_n$, V_{thn}, $(W/L)_p$, and V_{thp}, respectively. It is obvious that the variation in the threshold voltage of M_P and M_N has the largest effect on V_{CL1}. If these variations cannot be tolerated, the two inverters must be dispensed and the scheme of Fig. 2 can instead be adopted.

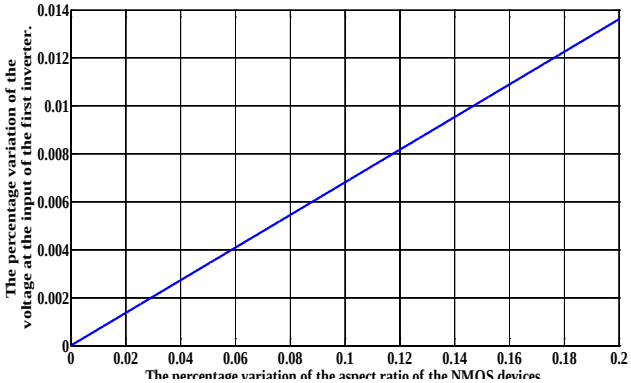

Fig. 13: The percentage variation of the voltage, V_{CL1}, versus that of the aspect ratio of M_N.

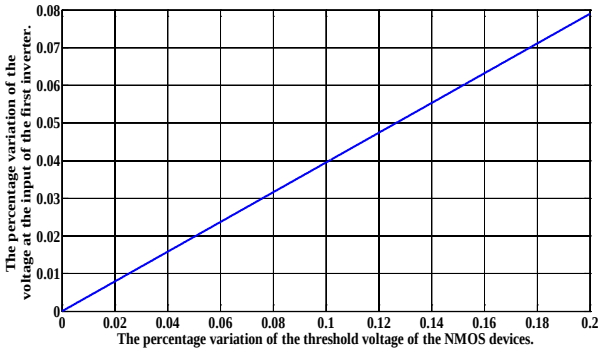

Fig. 14: The percentage variation of the voltage, V_{CL1}, versus that of the threshold voltage of M_N.

$$\frac{\Delta V_{CL11}}{V_{CL1}} = -\Delta\left(\frac{W}{L}\right)_n \left[\frac{-\frac{1}{2}k_n'(V_B - V_{thn})^2}{k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)V_{DD} - \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2} - \frac{-\frac{1}{2}k_n'(V_B - V_{thn})^2 \lambda_n}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 \lambda_n + k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)} \right] \quad (54)$$

$$\frac{\Delta V_{CL12}}{V_{CL1}} = \Delta V_{thn} \left[\frac{k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})}{k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)V_{DD} - \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2} + \frac{k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})\lambda_n}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 \lambda_n + k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)} \right] \quad (55)$$

$$\frac{\Delta V_{CL13}}{V_{CL1}} = \Delta\left(\frac{W}{L}\right)_p \left[\frac{k_p'(V_{DD} - |V_{thp}|)V_{DD}}{k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)V_{DD} - \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2} - \frac{k_p'(V_{DD} - |V_{thp}|)}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 \lambda_n + k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)} \right] \quad (56)$$

$$\frac{\Delta V_{CL14}}{V_{CL1}} = |\Delta V_{thp}| \left[\frac{-k_p'\left(\frac{W}{L}\right)_p V_{DD}}{k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)V_{DD} - \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2} + \frac{k_p'\left(\frac{W}{L}\right)_p}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_B - V_{thn})^2 \lambda_n + k_p'\left(\frac{W}{L}\right)_p (V_{DD} - |V_{thp}|)} \right] \quad (57)$$

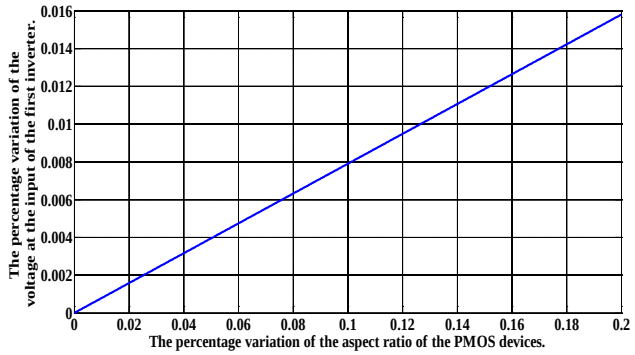

Fig. 15: The percentage variation of the voltage, V_{CL1}, versus that of the aspect ratio of M_P.

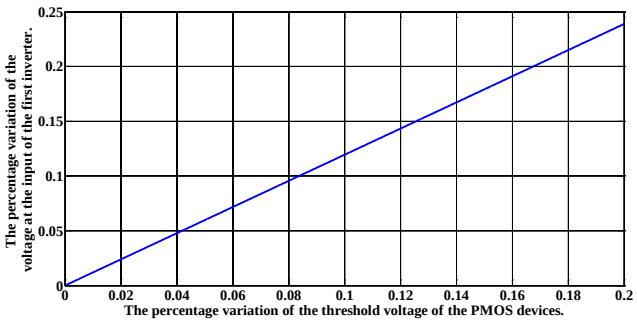

Fig. 16: The percentage variation of the voltage, V_{CL1}, versus that of the threshold voltage of M_P.

VII. Simulation Results

In this section, the pseudo-PMOS logic (Fig. 2) is verified by simulation adopting the 45 nm CMOS technology with V_{DD} = 0.8 V [22]. Assume minimum-sized devices and a frequency of operation equal to 500 MHz. As a compromise between the enhancement of the logic swing and the degradation in the high-to-low propagation delay with increasing V_{thn}, M_N is chosen with a threshold voltage equal to 0.7 V and biased by $V_B = V_{DD}$. In evaluating the low-to-high or the high-to-low propagation delays, the 50% criterion is adopted. The worst-case scenarios are also adopted.

Refer to Figs. 17, 18, and 19 for the low-to-high, the high-to-low, and the average propagation delays, respectively, versus the number of the inputs, n, for the conventional and pseudo-PMOS logic families. The low-to-high propagation delay according to the pseudo-PMOS logic is found to be smaller than that of the conventional one for all values of n. The superiority in performance of the pseudo-PMOS logic during the low-to-high transition is attributed to the need to charge all the internal capacitances of the pull-down network in the conventional CMOS stack. Although the contention current of M_N slows down the charging of C_L in the pseudo-PMOS logic, it does not affect the performance considerably.

On the other hand, the high-to-low transition of the pseudo-PMOS logic is faster than that of the conventional CMOS logic when n exceeds 4. The average propagation delay of the pseudo-PMOS logic is smaller than that of the conventional CMOS logic when n exceeds 3. Finally, note that the degradation in the logic swing compared to the conventional CMOS logic is approximately 63 mV, i.e. only 7.8%, in the worst case.

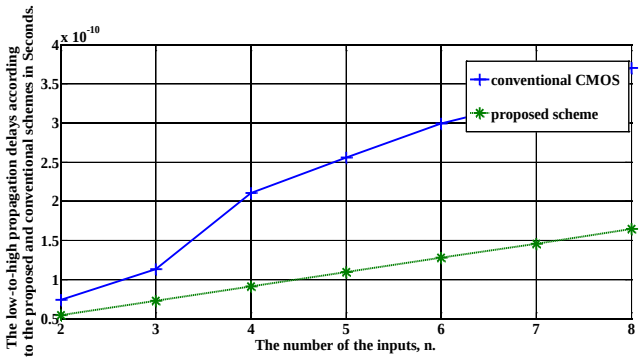

Fig. 17: The plots of the low-to-high propagation delays according to the conventional CMOS logic and the pseudo-PMOS logic versus the number of the inputs.

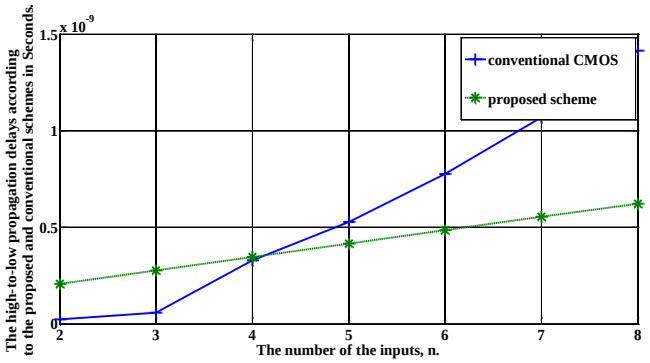

Fig. 18: The plots of the high-to-low propagation delays according to the conventional CMOS logic and the pseudo-PMOS logic versus the number of the inputs.

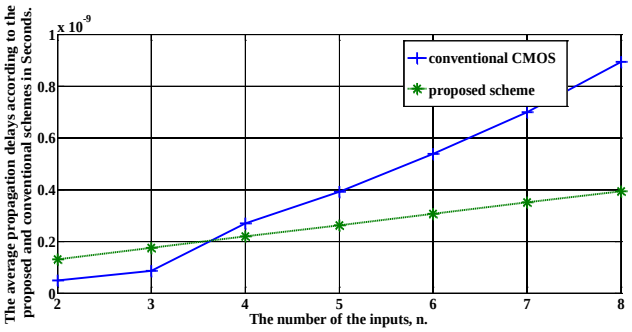

Fig. 19: The plots of the average propagation delays according to the conventional CMOS logic and the pseudo-PMOS logic versus the number of the inputs.

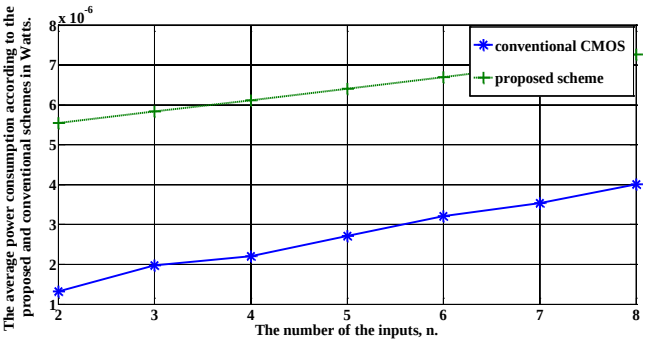

Fig. 20: The plots of the average power consumption according to the conventional CMOS logic and the pseudo-PMOS logic versus the number of the inputs.

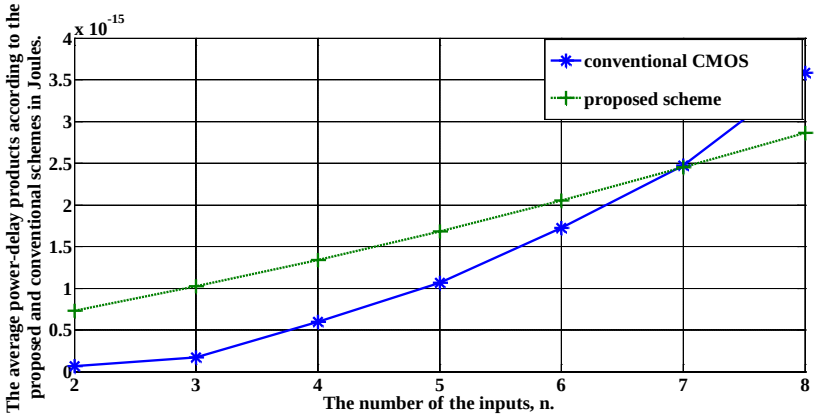

Fig. 21: The plots of the average power-delay products according to the conventional CMOS logic and the pseudo-PMOS logic versus the number of the inputs.

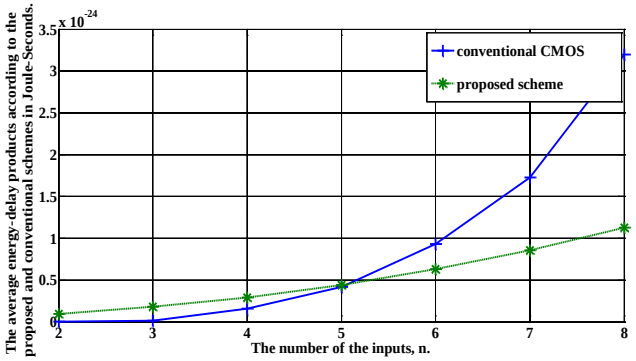

Fig. 22: The plots of the average energy-delay products according to the conventional CMOS logic and the pseudo-PMOS logic versus the number of the inputs.

The average power consumption, the average power-delay products (*PDPs*), and the average energy-delay products (*EDPs*) are plotted versus *n* in Figs. 20, 21, and 22, respectively, for the conventional and proposed logic families. The average power consumption of the CMOS logic rises with *n* at a faster rate compared to that of the pseudo-PMOS logic due to the need to charge the internal capacitances of the CMOS logic circuit. The *PDP* and the *EDP*, however, of the pseudo-PMOS logic are smaller than their counterparts of the CMOS logic when *n* exceeds 6 and 5, respectively.

VIII. Conclusions

The pseudo-PMOS logic family was adopted for realizing wide fan-in CMOS circuits containing long stacks of NMOS transistors. The area, propagation delay, power consumption, power-delay and energy-delay products of this family were compared with those of the conventional CMOS logic. The pseudo-PMOS logic showed superior performance from the points of view of the average propagation delay, power-delay product, and energy-delay product when the number of the inputs exceeds 3, 6, and 5, respectively. In fact, the pseudo-PMOS logic had a smaller area and average propagation delay but larger average power consumption and slightly smaller noise margin (by about 7.8% in the worst case compared to the conventional CMOS logic). According to the estimation performed in this paper using a proper figure of merit, the pseudo-PMOS logic is better than the CMOS logic when the number of the inputs exceeds 8.

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Short Term Load Forecasting of a Region of India using Generalized Regression Neural Network

By Ram Dayal Rathor & Dr. Annapurna Bharagava
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Keywords: short term load forecasting, ANN, GRNN, MAE, MAPE.

GJRE-F Classification: FOR Code: 280212

Strictly as per the compliance and regulations of:

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Ram Dayal Rathor [α] & Dr. Annapurna Bharagava [σ]

Abstract- In this paper the Generalized Regression Neural Network is used for short term load forecasting (STLF) of Rajasthan region, India. It is a power ful technique to schedule plant maintenance, power system control and load flow. Rajasthan state has rich cultural and geographical diversities. It is the biggest state of India and its land area is 342,239 km². The actual data of load and temperature have been collected from Load Dispatch Center, Rajasthan and Meteorological Center Jaipur, Rajasthan, for the duration from January 2008 to December 2008. Load is forecasted with help of Artificial Neural Network and Generalized Regression Neural Network (GRNN) based models for summer, monsoon and winter seasons. Last 24 hours load, maximum and minimum temperature, season code, day type and effect of social celebrations are used as input of the networks. Results have been obtained for different patterns of load. Results show that both models have good performance and reasonable prediction accuracy. Their comparison demonstrates that GRNN model is much faster, more reliable and accurate for effective STLF of Rajasthan region, India.

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I. Introduction

Electrical load forecasting is important for the power industries in the deregulated economy. Operative forecasting is essential for generation control and power dispatch [1]. Operational decisions in power systems, such as unit commitment, economic dispatch, automatic generation control, security assessment, maintenance planning, and energy trading depend on the forthcoming trends of loads [2]. Accurate short term forecasting results in better economic and trouble free operations. The improved efficiency and accurate load scheduling, decreases power system reserves [3]. Short-term load forecasting plays an important role in reliability of power grid, prevent overloading and reduce the occurrence of blackouts [4]. Load forecasting have many applications such as energy trading, power generation, load flow and infrastructure development [5]. It plays an important role to take decisions relating to electrical network. STLF is required for power system control, unit commitment, security assessment, planning spinning reserve, energy exchange, inputs to load flow studies and contingency analysis resulting in predictive assessment of the security of the power system in which effect of loss of each generator on each transmission circuit is evaluated. The accuracy and reliability of load forecast have considerable effect on economics of power system operation [6, 7, 8]. Load forecasting can be categorize in very short term forecasting, short term forecasting, medium forecasting and long term forecasting [9]. Economic load dispatching requires the minute to minute load allocation to the generating units, to meet the varying demand at minimum cost and appropriate degree of system security. It is essential to minimize the cost function, subjected to a large number of operating units, plant characteristics and transmission system limits. There are a number of factors which effects STLF such as temperature variations, climatic conditions, social celebrations, agricultural load demand and tariff structure. Load forecasting remains a difficult task because the system loads generally display periodicity and seasonality at multiple time scales and beside this there are many outside variables, such as weather conditions. Therefore it is concluded that there is not a single forecasting model which can give accurate results for all power systems [10].

Out of many of STLF techniques, in recent years, ANN based techniques are being used due to their good characteristics for high-speed computation, potential methodology for modeling hourly and daily energy consumption, their ability to perform better during rapidly changing weather conditions and the short time requirement for their development. ANN based methods uses a functional relationship between load and affecting factors, and estimate the functional coefficients by using historical data [11]. Neural network based models have mainly the drawback of using simple neuron having summation and sigmoid as transfer functions. These requires large numbers of neurons and hidden layers for complex function approximations and takes large training time and have problem of convergence. Use of the sigmoidal transfer function and ordinary summation or product as aggregation functions in the simple ANN based models fail to cope with the nonlinearities involved in real life

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problems [12, 13].In this research the Generalized Regression Neural Network (GRNN) based model is used for short term load forecasting of Rajasthan state in India. GRNN is related to radial basis function of network and is based on standard statistical technique called Karnel regression. It is a powerful method to solve problems like forecasting, control, plant operation and fault identification and it does not provide negative estimation and approximates the training data with less error [14-16]. Rajasthan region has large variations in climatic, social and geographical conditions. A big part of region is desert which has very low rainfall in comparison of south east part of province. Most of the load is agricultural and domestic and therefore load profile is dependent on temperature variations, rain fall, social celebrations, type of crop and crop cycle.

II. Basic Structure of Artificial Neural Network Based Model

The neural network derives its computing power through its massively distributed structure and has ability to learn and therefore generalization. The flexibility of the generalized neuron can be improved by using more number of activation functions like Sigmoid, Gaussian and straight line. This reduces the size of network. The working of ANN model is explained with the help of Fig. 1

The output of ANN,

$$\text{Output}=f\left(W_i x_i+b\right)$$

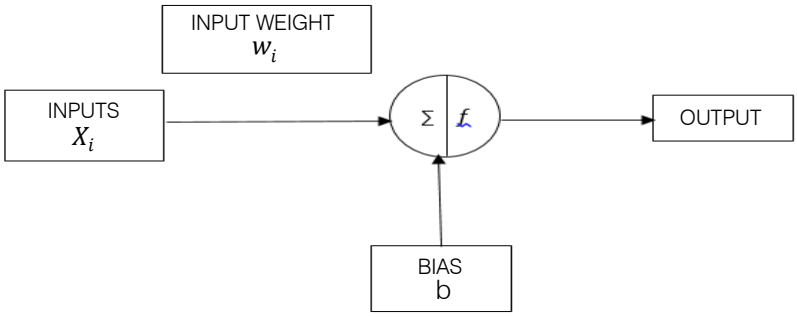

Fig. 1: Block diagram of ANN

In Fig.1,*f*is the transfer function (activation function) and *b* is thresh hold value(bias).

III. Generalized Regression Neural Network Based Model

The working of GRNN model is shown in Fig. 2.

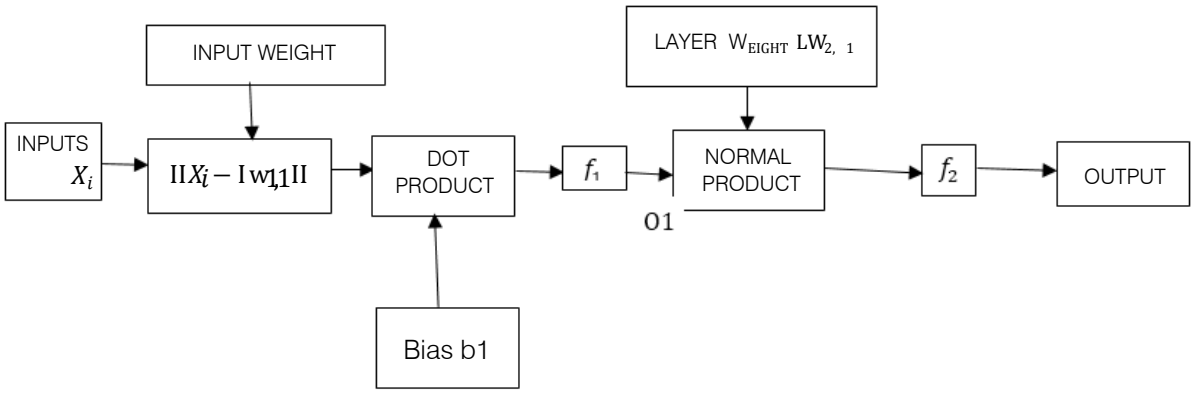

Fig. 2: Block diagram of GRNN

In Fig.2
$LW_{2,1}$ = Weight of signal between layer 1 and 2.
O1 = Output of the first layer
Output= Output of GRNN,

IV. Design of Implementation

a) Data Collection

The real data are collected from January 2008 to December 2008. For ensuring selection of most relevant data and assurance of error free data used for forecasting of electrical load of Rajasthan state, electrical load data and meteorological data are collected from concerned government agencies Rajasthan RajyaVidyutPrasaran Nigam Ltd (RRVPNL), State Load Dispatch Centre (SLDC), Jaipur and India Meteorological department, MausamBhawan, Jaipur respectively. These data are provided by these departments on concession rates applicable to research students. Two types of data have been collected for short term load forecasting of Rajasthan state:

- Every fifteen minute interval data of electrical energy consumption of year 2008
- Maximum and Minimum temperature of the days of year 2008

The load of all four season's spring, summer, monsoon, winter is collected. As Rajasthan is a big state maximum and minimum temperature of zonal head quarter Jaipur, Bikaner and Kota are taken as temperature input.

b) Data Preparation

The use of original data as input to neural network may cause convergence problem. To improve (and sometimes ensure) convergence, the data must be scaled or normalize such that to unify the very different ranges of the data originally collected. Neural network training can be made more efficient if certain preprocessing steps are performed on the network inputs and targets. Before training, the inputs and targets are normalized so that they always fall within a specified range. There is a strong correlation between the behavior of power consumption and weather variables. Here temperature (maximum and minimum) of three stations are considered as weather variables because other factors have weak effect on electric power consumption. In this model three types of variables are used as inputs to the neural network for training: (a) day indicator i.e. date, month and day code, (b) weather related inputs i.e. maximum and minimum temperature of the day, and (c) load of previous 24 hrs.

Total 105 data are given as input to the network, in which first 3 are used to recognize season and day code. Next 6 data are maximum and minimum temperature data and remaining 96 data are loads of every 15 minute in 24 hour of the day, starting from 0.15 AM midnight. During training of ANN and GRNN models, previous day's data are taken as input and same day data are taken as target. After training of models, data of day before forecasting day are taken as input and data of forecasting day are taken as target.

c) Simulation of ANN Model

ANN model has three layers, in which Gaussian, Log Sigmoid and Straight line are used as activation functions. Fig. 1 shows the structure of ANN model. This figure is directly taken from MATLAB during training to show the training parameters.

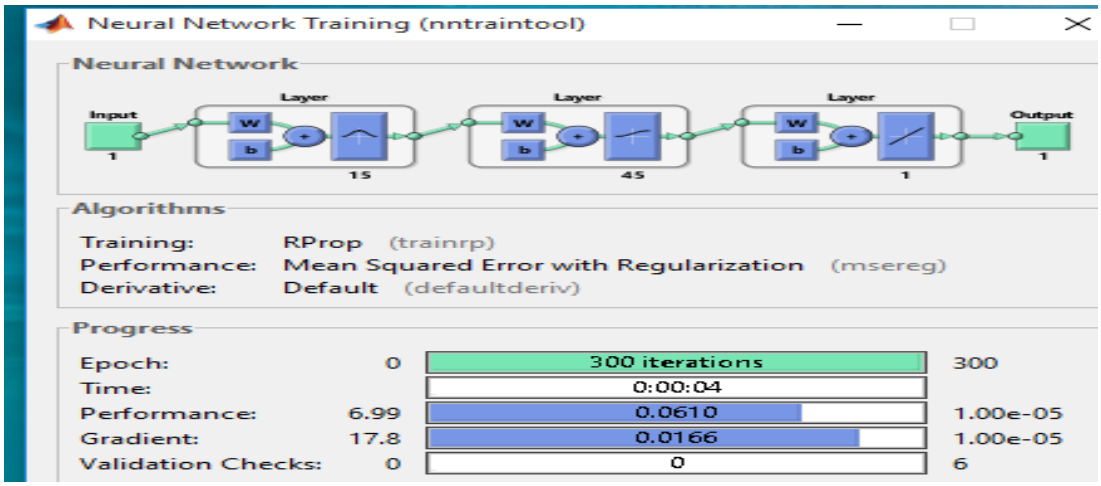

Fig. 3: ANN Model

The parameters of three layer feed forward neural network for network training are as given below:

- Number of layers: 3 (Input, Hidden, Output layer)
- Number of neurons in input layer: 15
- Number of neurons in hidden layer: 45
- Number of neurons in output layer: 1
- Activation function of input layer: *radbas*
- Activation function of hidden layer: *logsigmoid*
- Activation function of output layer: *purelin*
- Training algorithm: *trainrp*
- Number of input variables: 105 (96 + 9)
- Number of output variable: 105

- Number of data sets in each Epoch: 100
- Number of Epochs for training: 300

d) Simulation of GRNN Model

A generalized regression neural network (GRNN) is often used for function approximation. As shown in architecture, it has a radial basis layer and a special linear layer. Fig. 2 shows the structure of GRNN Model. This figure is taken from MATLAB during simulation.

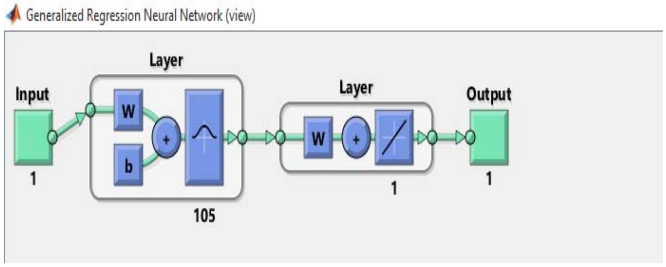

Fig. 4: GRNN Model

The parameters of GRNN for day ahead load forecasting are as given below:

- Number of layers: 2 (Input layer, Output layer)
- Number of neurons in input layer: 105
- Number of neurons in output layer: 1
- Activation function of input layer: radbas
- Activation function of output layer: purelin
- Number of input variables: 105 (96 + 9)
- Number of output variable: 105
- Spread: 0.009

V. Performance Matrices

The accuracy of the forecasting is measured the following Performance Matrices

1. Mean Absolute Error (MAE)

$$\text{MAE} = \frac{1}{M}\sum_{i=1}^{M}|actual(i) - forecast(i)|$$ Where

M is the total number of data points, $actual(i)$ is the i[th] actual value, and $forecast(i)$ is the i[th] forecast.

2. Mean Absolute Percentage Error (MAPE)

$$\text{MAPE} = \frac{1}{M}\sum_{i=1}^{M}\frac{|actual(i) - forcast(i)|}{actual(i)} \times 100\ \%$$

The MAE criterion penalizes all errors equally, whereas MAPE criterion is accepted industry standard for measuring load forecast quality.

VI. Results and Discussion

The load profile is dynamic in nature with temporal, seasonal and annual variations. The load pattern is divided into four categories: week days, weekend days, holidays and social celebration days. Forecasting results of all four seasons of week days have been shown in graphical form. Actual load, forecasted load and percentage forecast error for ANN and GRNN are also shown in tabular form.

Percentage forecasting error is calculated by the relation:

% error = [(Actual load-Forecasted load) /Actual load] * 100

ANN and GRNN models have been tested on data of Rajasthan region of India.

a) Results of Summer Season

In this category load curve of week day (5 June 2008, Thursday) in summer season is selected for forecasting. Fig.3. shows load curve of actual load, load forecasted by ANN and load forecasted by GRNN against day hours (every 15 minute interval). Comparison of forecasting error by ANN and GRNN is also shown in Fig.4.

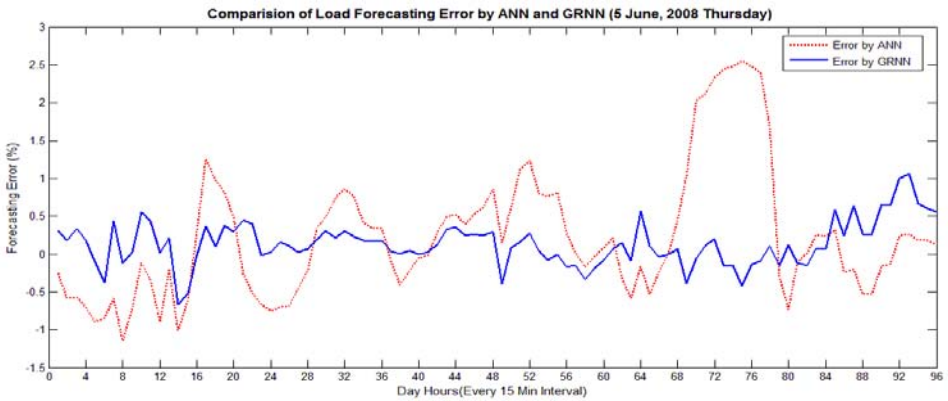

Fig. 5: Comparison of Forecasting Error by ANN and GRNN

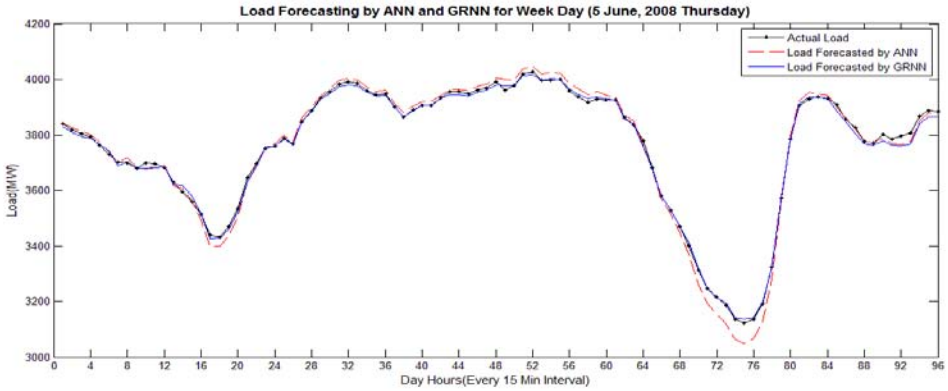

Fig. 6: Comparison of Load Forecasting by ANN and GRNN in summer

b) Results of Monsoon Season

In this category load curve of week day (11 August 2008, Monday) in monsoon season is selected for forecasting. Fig.5 shows load curve of actual load, load forecasted by ANN and load forecasted by GRNN against day hours (every 15 minute interval). Comparison of forecasting error by ANN and GRNN is also shown in Fig. 6

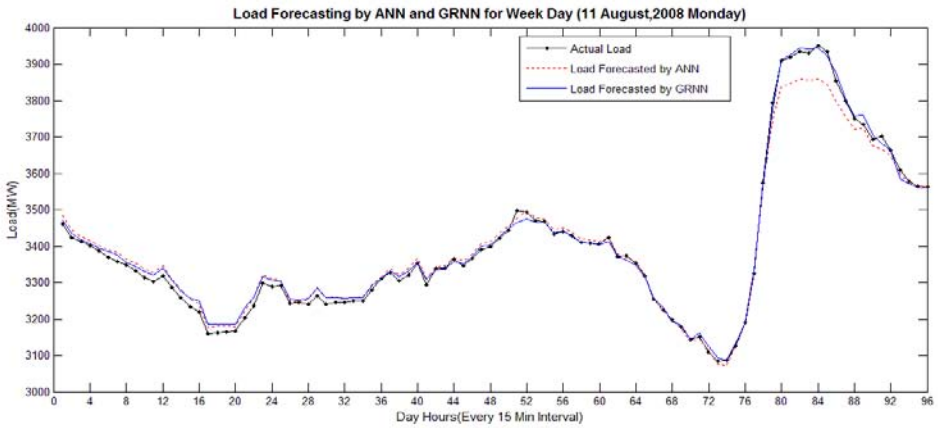

Fig. 7: Comparison of Load Forecasting by ANN and GRNN in monsoon

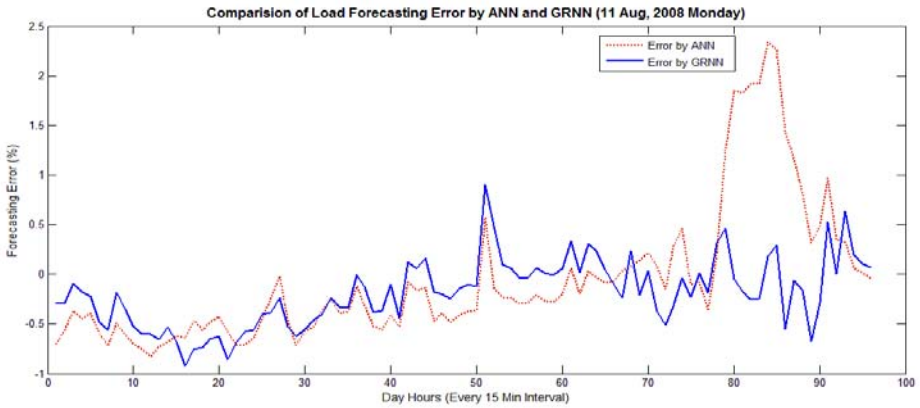

Fig. 8: Comparison of Forecasting Error by ANN and GRNN

c) Results of Winter Season

In this category load curve of week day (16 December 2008, Tuesday) in winter season is selected for forecasting. Fig.7. shows load curve of actual load, load forecasted by ANN and load forecasted by GRNN against day hours (every 15 minute interval). Comparison of forecasting error by ANN and GRNN is also shown in Fig.8.

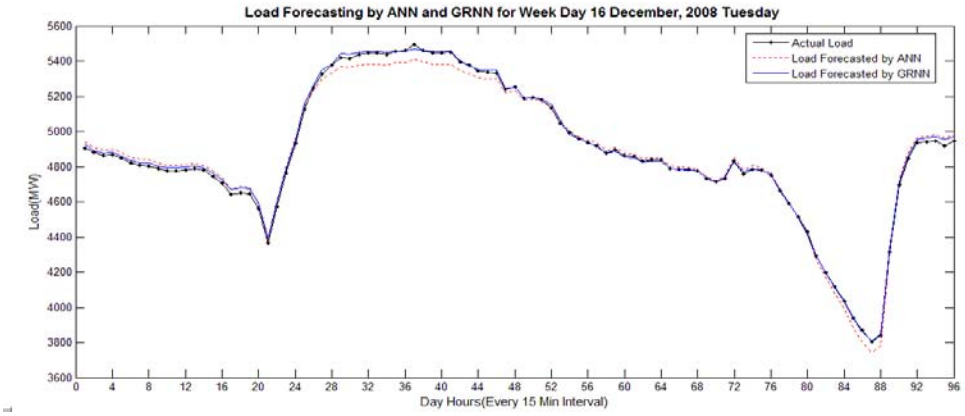

Fig. 9: Comparison of Load Forecasting by ANN and GRNN in winter

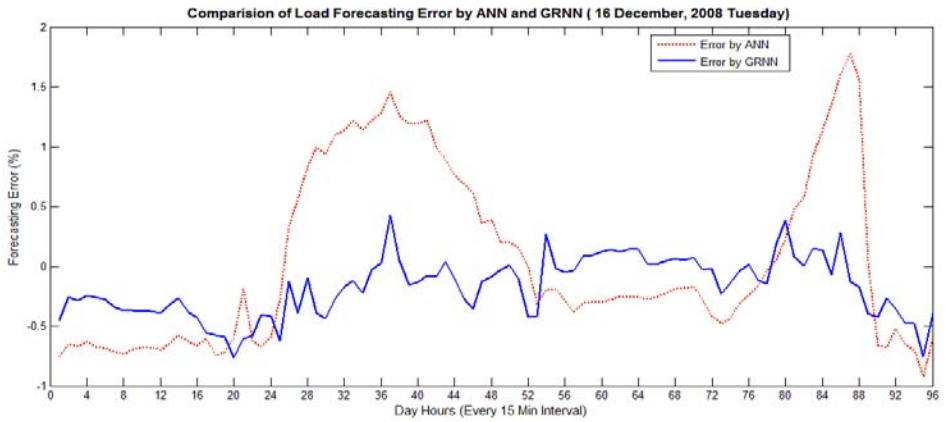

Fig. 10: Comparison of Forecasting Error by ANN and GRNN

The different performance matrices are summarized in tabular form in table no.1

Table 1: Error Comparison

Season	Model	Max. % Error	MAE	MAPE
Summer	ANN	0.0035	2.3852	23.003
	GRNN	**0.0021**	**1.0237**	**8.8046**
Monsoon	ANN	0.0073	2.3468	12.137
	GRNN	**0.0047**	**0.9272**	**10.712**
Winter	ANN	0.0009	1.7770	31.306
	GRNN	**0.0029**	**0.7645**	**11.316**

During result evaluation phase following points were noticed:

- Results demonstrate that optimal structure of both methods ANN and GRNN with minimum forecasting error achieved. The parameters of models were finalized after several trials and error efforts to give the optimum performance.
- In Rajasthan state load is mostly depending upon agriculture and crop cycle.
- GRNN model has less MAE and MAPE as compared to ANN model. This represents a high degree of accuracy in the ability of neural networks to forecast electric load.
- It is observed during case study that GRNN is very fast in comparison of ANN. GRNN does not require the optimization of numbers of neurons and layers in the network. GRNN based model is easy to design and implement.

VII. Conclusion

This work is an effort to examine the neural network based models for STLF. ANN based load forecasting models are very attractive alternative in energy management systems due to simplicity and accuracy. From the forecasting results it is found that GRNN based model produces better performance matrices. GRNN model is faster and easy to design and implementation in comparison of ANN based model.

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Synthesizing Uniform Sum and Difference Patterns by Controlling Steer Angle and using Sub-Arrays

By Jafar Ramadhan Mohammed
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Abstract- Synthesizing sum and difference patterns are usually achieved by controlling two separate sets of the amplitude and phase excitations of the radar antenna elements. In this paper, an alternative and effective approach is proposed. First, by equally partitioning the uniform array elements into two subarrays and then by suitably controlling the steered angle of the beam pattern of each sub-array individually, it is possible to generate the required sum and difference patterns. Since the steering angle parameter is the most important in the proposed method, a general strategy is shown for the selection process of its value. Unlike the existing techniques, the feeding network in the proposed approach is much simpler in practical implementation.

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GJRE-F Classification: FOR Code: 290901

Strictly as per the compliance and regulations of:

Synthesizing Uniform Sum and Difference Patterns by Controlling Steer Angle and using Sub-Arrays

Jafar Ramadhan Mohammed

Abstract- **Synthesizing sum and difference patterns are usually achieved by controlling two separate sets of the amplitude and phase excitations of the radar antenna elements. In this paper, an alternative and effective approach is proposed. First, by equally partitioning the uniform array elements into two sub-arrays and then by suitably controlling the steered angle of the beam pattern of each sub-array individually, it is possible to generate the required sum and difference patterns. Since the steering angle parameter is the most important in the proposed method, a general strategy is shown for the selection process of its value. Unlike the existing techniques, the feeding network in the proposed approach is much simpler in practical implementation.**

Keywords: monopulse antenna, phased arrays, beam pattern synthesis, uniform amplitude distribution.

I. Introduction

Effective design, in terms of cost and simplicity of the feeding network, of a monopulse radar antenna that able to generate the required sum and difference patterns is very desirable. In order to get a feed network as simple as possible, and thus reduce the costs while still generating both patterns, several techniques have been proposed. These include sub-array architectures [1-2], or arrays having common excitations when reconfiguring the pattern from a sum to a difference pattern [3-5], or even the exploitation of using two extra side elements [6-7].More recently, global optimization techniques such as genetic algorithm or particle swarm optimization, with capability of incorporating some constraints in the design process, have been also used [8-9].

In most of the aforementioned techniques, the sum and difference patterns are usually synthesized by using non uniform amplitude distribution se.g., Dolph or Taylor distributions for sum pattern formation and Bayliss distribution for difference pattern formation. Implementation of these distributions require dedicated attenuators/amplifiers and phase shifters (i.e., a variable attenuator and a variable phase shifter for each array element). Accordingly, such implementation requires fairly complex, and expensive feeding network. In addition, these aforementioned non uniform amplitude distribution arrays suffer from directivity saturation for large number of array elements [10].

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In contrast, the practical implementation of the uniform amplitude distribution arrays does not actually require any additional hardware (i.e., attenuators/amplifiers and phase shifters) since the phase shifters are already there for scanning. Thus, the implementation of such a uniform distribution array requires a very less expensive feeding network. Besides the simplicity in the feeding network, the other advantage of the uniform amplitude distribution arrays is their capabilities to provide desired directivity. One of the main drawback of such an array is its high sidelobe level (-13.4 dB) which is not adequate for radar applications that requiring low sidelobe levels.

In this paper, a simple and a new technique for synthesizing sum and difference patterns with uniform amplitude distribution in the linear arrays is presented. In particular, by dividing the array elements into two equally sub-arrays and controlling the steered angles of these two sub-array patterns individually. Then the required sum and difference patterns can be generated by adding or subtracting the steered radiation patterns of these two sub-arrays. Furthermore, by suitably choosing the steer angle of each sub-array pattern, it is also possible to significantly reduce the sidelobe level of the resulting sum pattern while still maintaining uniform amplitude distribution in the feeding network. The sidelobe reduction and the half power beam width (HPBW) in the resulting sum pattern are directly proportional to the selecting values of the steered angles of both sub-arrays.

II. The Method

The structure of the proposed array is shown in Fig.1. In this structure, the total N=2M elements of the uniformly excited equally spaced linear array is divided into two sub-arrays, i.e., left and right subarrays. The index of each element on the left and right sides are ranged from –M to -1 and from 1 to M, respectively.

In each sub-array, the M elements array has uniform amplitude excitations a_n = 1and equally spaced elements with the peak of the main beam steering at desired direction.

Assuming the phase center is at the center of the array and between the two sub-arrays, then the array factors of both sub-arrays are given by

$$AF_{Sum}(\theta) = \underbrace{\sum_{m=-N}^{-1} e^{-j\left(\frac{2m-1}{2}\right)[\,kdsin(\theta)+\beta_l\,]}}_{Left\ side\ sub\ array} + \underbrace{\sum_{m=1}^{N} e^{+j\left(\frac{2m-1}{2}\right)[\,kdsin(\theta)+\beta_r\,]}}_{Right\ side\ sub\ array} \quad (1)$$

where k is the wave number, d is the element spacing, β_l and β_r are the specified scan angles of the main beams for the left and right sub-arrays, respectively, and θ is the observation angle from the normal to array axis and varies from-90° to 90.° It should be mentioned that the array factor expressions which are available in the literature are always real quantity. In contrast, the array factors in (1) for the left and right sides sub-arraysare complex quantities. If the values of steered angles β_l and β_r are not equal it is not possible to get a real array factor expression. Furthermore, it must be noted that the reference axis is at the centre of the array which invariably must generate a real valued array factor.

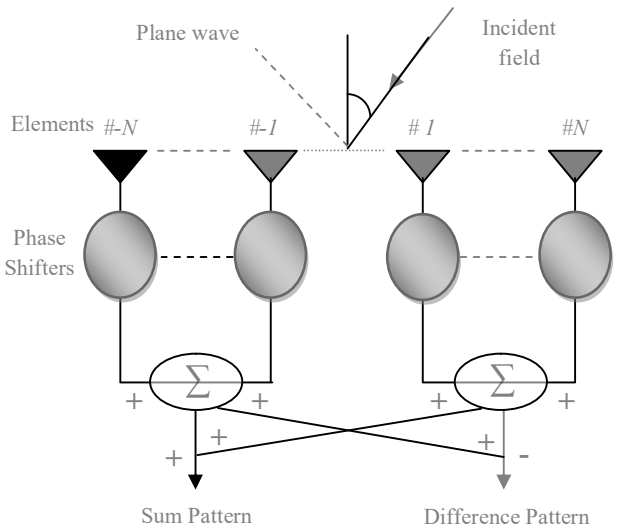

Fig. 1: Sub-array configuration for the proposed technique

Fig.2 shows the radiation patterns of the left and right sub-arrays computed separately according to the first and second terms of (1) for used parameters; $d = \lambda/2$, N=20, β_l and β_r are equal to-8^o and$+8^o$ respectively. It can be seen that the sum pattern can be easily generated by simply adding these two patterns according to (1). Moreover, the sidelobe structures of both patterns are out of phase (anti-phase). This means that the resulting sum pattern will have some reduction in its sidelobe level with compare to the main uniform array where its peak sidelobe value is at -13.4dB.

On the other hand, by just subtracting the pattern of left side sub-array from that of right side sub-array the difference pattern can be easily generated using the same values of β_l and β_r (see Fig.3).

Note that the parameters, β_l and β_r should be carefully chosen as they are responsible for the shape formation of the resulting sum and difference patterns. This issue is investigated in Section IV.

III. Feeding Network

As mentioned earlier, the antenna array under investigation has uniform amplitude distribution. Thus it is not requires any attenuators or amplifiers. On the other hand, the antenna arrays based on electronic steering already contains a variable phase shifter in each element of the array for main beam steering, thus the practical implementation of the proposed method does not actually require any additional hardware.

In comparison with existing techniques which are usually use two separate hardware sets of attenuators and phase shifters to reconfigure between sum and difference patterns, the proposed method uses one hardware set that consists only phase shifters.

Moreover, these phase shifters are fully shared in the proposed method to generate the required sum and difference patterns. Although there are a various techniques for synthesizing sum and difference patterns, the proposed configuration with fully common element excitations has not been previously tried to the best of my knowledge and is able to provide a significant reduction in the complexity and cost of feeding network. Table I shows the complexity of the feeding network for different techniques. From this table, it can be seen that for 20 elements radar antenna, the total number of the required attenuators and phase shifters for synthesizing sum and difference patterns under the case of no common (or separate) excitation are 40 attenuators and 20 phase shifters, while these numbers are reduced to 30attenuators and 20 phase shifters using the method presented in [4] and it is further reduced to only 20phase shifters with the proposed method.

IV. Simulation Results

To illustrate the effectiveness of the proposed approach, a number of numerical experiments have been performed. In the following examples, we assume a uniform linear array with N=20 elements and half-wavelength element spacing. The two sub arrays are then formed by dividing the main array elements into two equally sub arrays, each with M=10 elements. Figures from Fig.4 to Fig.7, shows the resulting sum and difference patterns under various values of steering angles. In all these figures, the values of steering angles are chosen such that $\beta_l = -\beta_r$ (i.e., symmetric).

From all these figures, it can be seen that the required sum and difference beam patterns can be achieved when setting the steered angles at small values and near to the broadside direction. Also note that for Figs 4 to 6, the intersection area between main beams of the two sub-arrays is large and the half power beam width (HPBW) of the resulting sum pattern is exactly equal to that of the standard uniform array. On the other hand, and for large values of steering angles, the HPBW of the resulting sum patterns are significantly increased with respect to that of the standard uniform array and the main beams become nearly flat top with some ripples at the top of the main beam (see Fig.7). Note that this case can be considered as a multiple-pattern antenna arrays that capable to radiate more than one pattern by only varying the steered angle.

This pattern reconfiguration issue is desirable in many applications such as radar, remote sensing, and telecommunications. The resulting difference patterns are adequately locating a null at desired direction since there are still some intersection area between the main beams of both sub-array patterns. Fig.8 shows the variations of the HPBW versus the steering angle values. From this figure, it can be seen that, for small steer angle values which are ranging from $\beta_l = -\beta_r = 1^o$ to 17^o, the HPBW of the resulting sum pattern is at 5^o which is nearly equal to that of the standard uniform array. For other values of $\beta_l = -\beta_r = 18^o$ to 24^o, the HPBW of the resulting sum pattern is at 17^o and its main beam top become flat with some ripples between 0 dB and -2 dB . For $\beta_l = -\beta_r = 30^o$or any other larger values, the resulting sum pattern fails in its operation where it is starting to locate a null instead of peak main beam at the broadside direction. This effect is clearly shown in Fig. 9.

Finally, the sidelobe level in the resulting sum pattern can be significantly reduced if we chose asymmetric values for the steering angles (i.e., $\beta_l \neq \beta_r$) such that the sidelobe structures of both sub-array patterns are approximately equal in magnitude and out of phase. Fig. 10 shows such contradiction in the sidelobe structures of both patterns for choosing values $\beta_l = 0^o$ and $\beta_r = 5.74$.As a result, the sum pattern have a low sidelobe level (an improvement of 6 dB with respect to the standard uniform array). This improvement is come at the cost of little shifting in the main beam of the resulting array.

V. Conclusions

An alternative method for synthesizing sum and difference beam patterns with uniformly excited equally spaced linear arrays has been presented. By suitably choosing the steering angle of the beam patterns of the left and right sub-arrays, it is possible to generate the required sum and difference patterns. It is evident from the present investigation that there is a general strategy to assist the selection process of the steering angle adjustment. First, the generated sum pattern may be exactly same as that of the standard uniform array with narrow HPBW if the steering angles chosen at small values and near to the broadside direction. This imply that the steered main beams of both sub-arrays are intersected at a large area. Next, for small intersection area, the choosing value of the steering angle may lead to reconfiguration the overall array pattern from pencil beam to a pattern like a flat-top beam with wide HPBW.

Finally, for the case of no intersection area between main beams of both sub-array patterns, the steering angle values are not recommended as the resulting sum patterns fails in its operation. Besides the diversity of use, other advantage of the proposed technique is that it is suitable for practical implementation.

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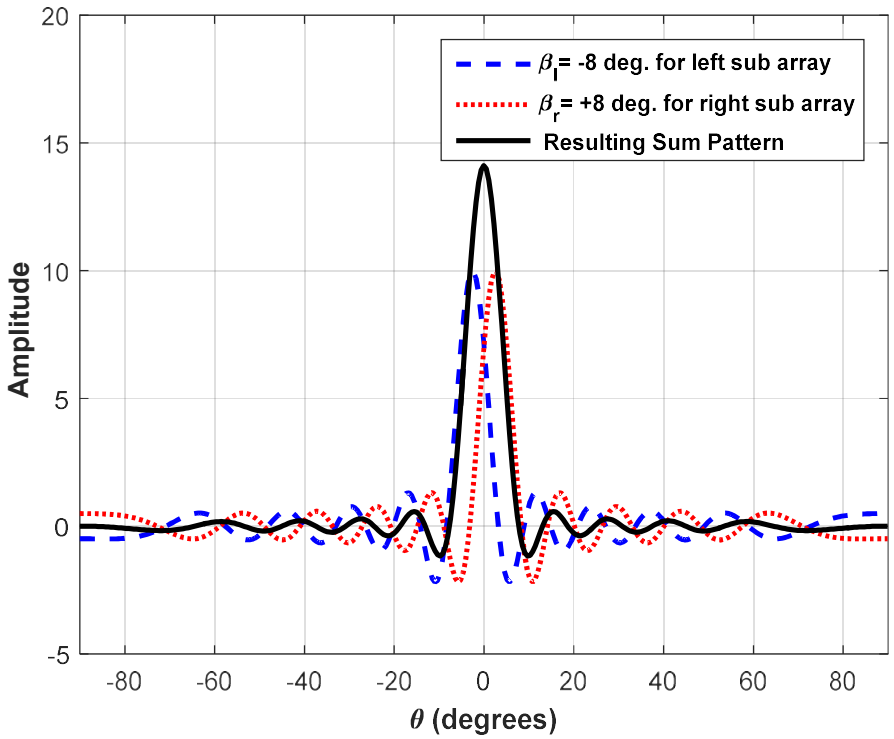

Fig. 2: The beam patterns due to left and right sides sub-arrays and the resulting sum pattern.

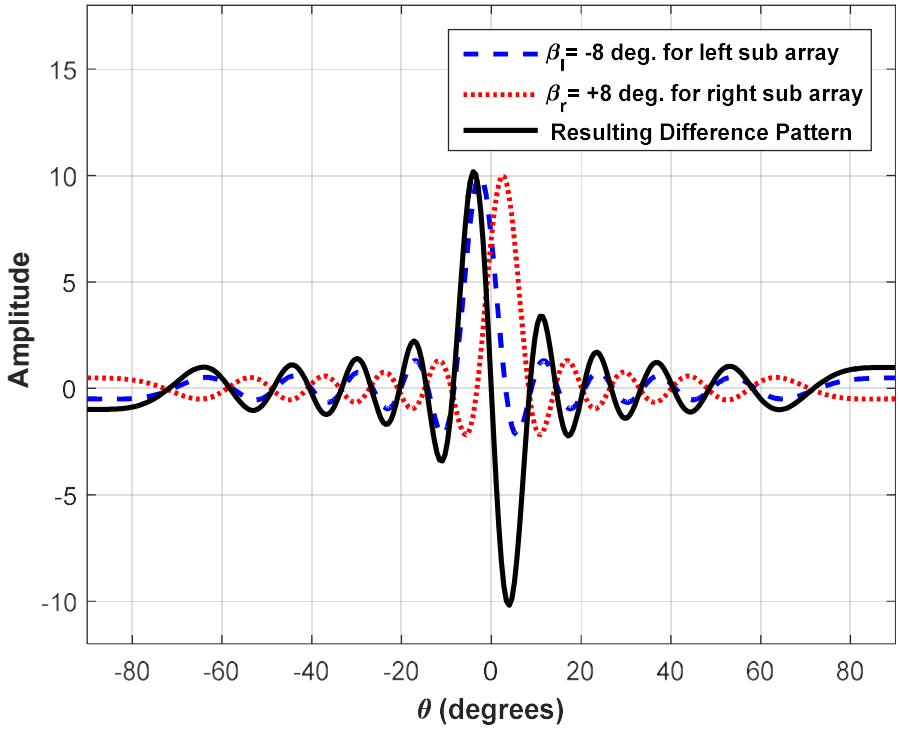

Fig. 3: The beam patterns due to left and right sides sub-arrays and the resulting difference pattern.

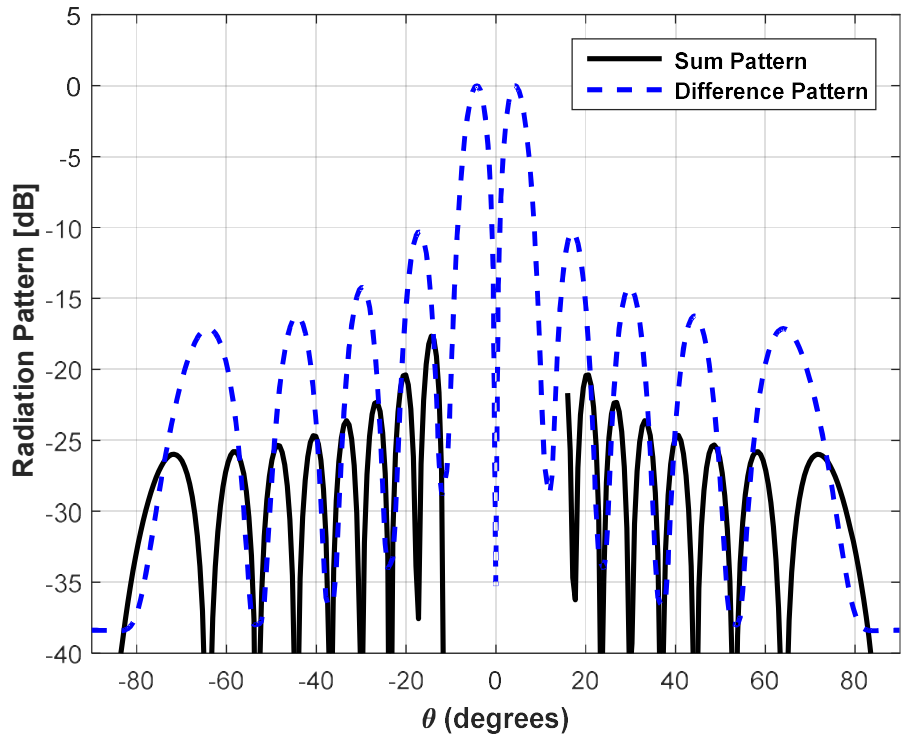

Fig. 4: The resulting sum and difference beam patterns for $2N = 20$, $d = \lambda/2$, $\beta_l = -\beta_r = 1^o$.

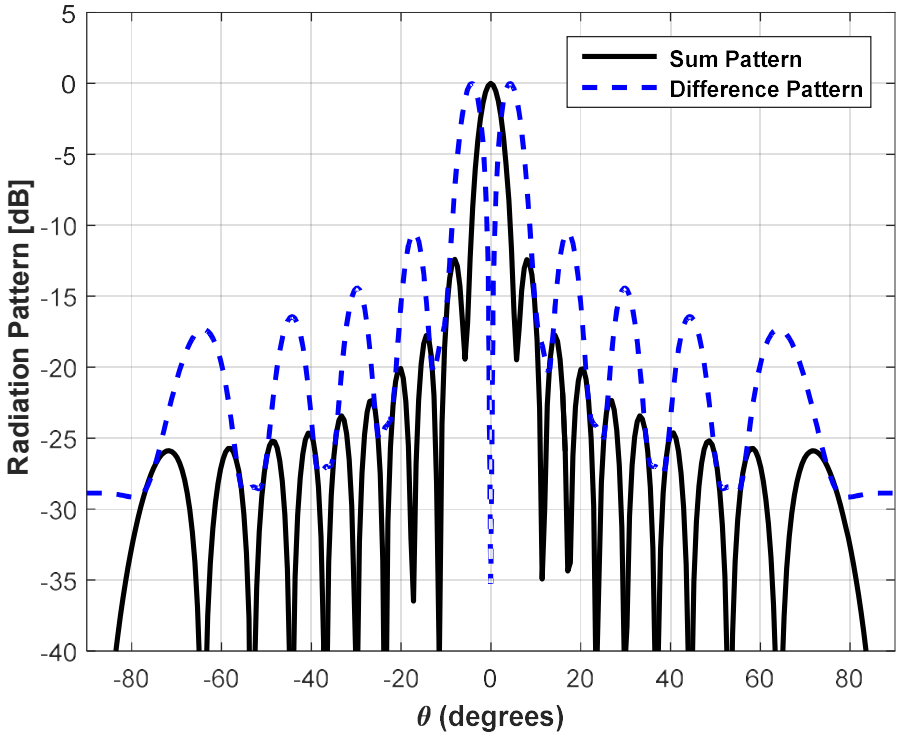

Fig. 5: The resulting sum and difference beam patterns for $2N = 20$, $d = \lambda/2$, $\beta_l = -\beta_r = 3^o$.

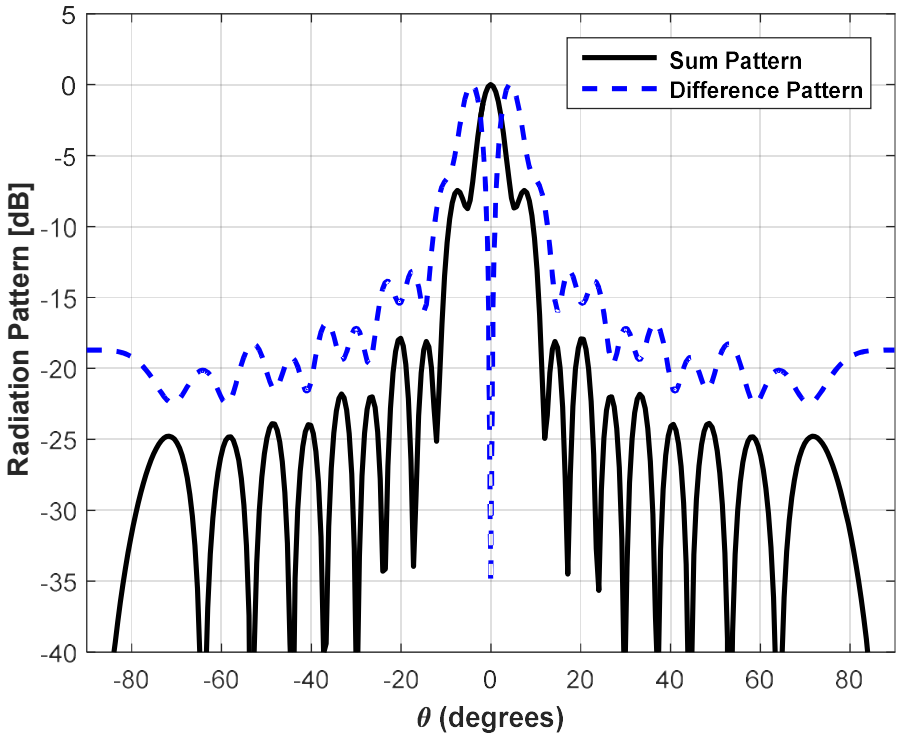

Fig. 6: The resulting sum and difference beam patterns for $2N = 20$, $d = \lambda/2$, $\beta_l = -\beta_r = 10^o$.

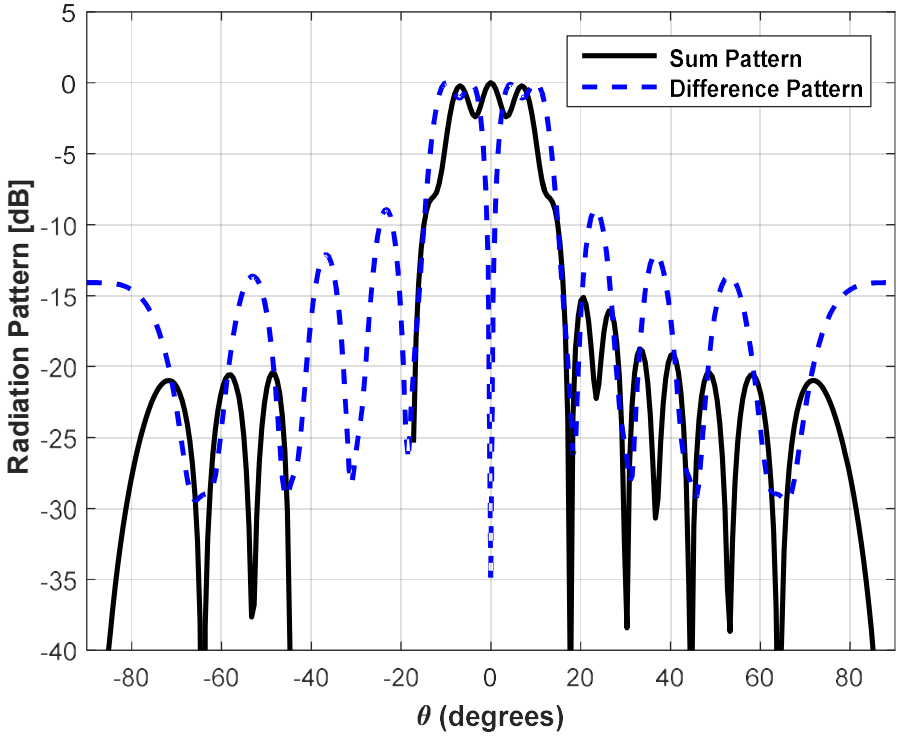

Fig. 7: The resulting sum and difference beam patterns for $2N = 20$, $d = \lambda/2$, $\beta_l = -\beta_r = 20^o$.

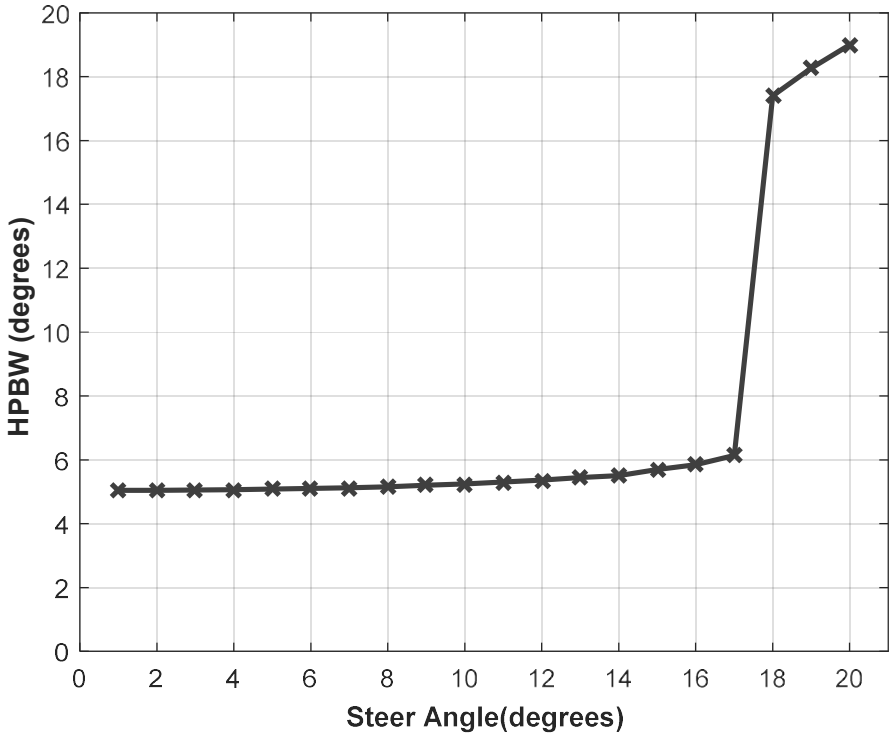

Fig. 8: The HPBW versus Steering Angles$\beta_l = -\beta_r$.

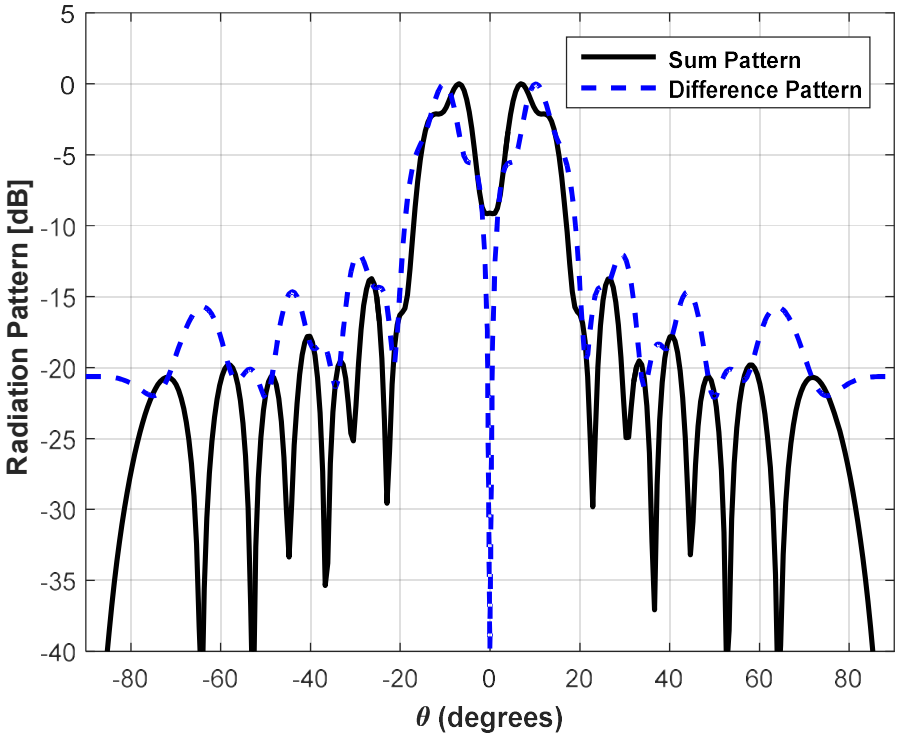

Fig. 9: The resulting sum and difference beam patterns for $2N = 20$, $d = \lambda/2$, $\beta_l = -\beta_r = 30^o$.

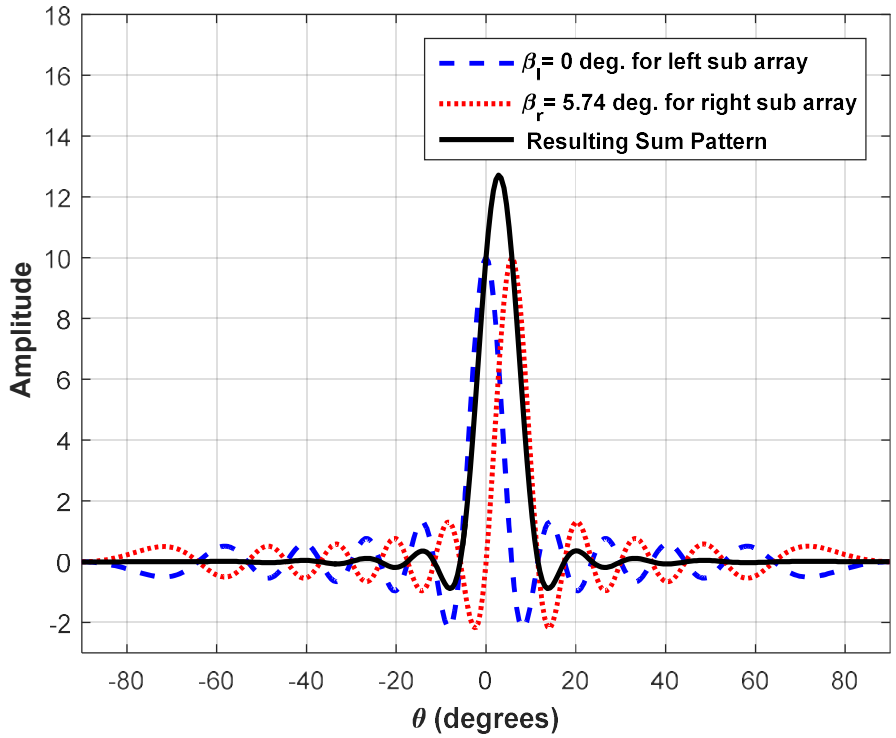

Fig. 10: The resulting sum and difference beam patterns for $2N = 20$, $d = \lambda/2$, $\beta_l = 0^o and\ \beta_r = 5.74^o$.

Table I: Complexity of the Feeding Network for Different Techniques

Technique	Feeding Network Complexity	
	Total No. of Attenuators for both Sum & Difference Patterns	Total No. of Phase Shifters for scanning both Sum & Difference Patterns
Separate excitations (No common excitations)	2N	N
Common excitations [4] (Sharing percentage 50%)	2N-N/2	N
Proposed Array	0	N

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Planar and Angular Modified Substrate Integrated Waveguide (SIW) Filter with Electromagnetic Bandgap(EBG) Structures

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Abstract- Designing of 180o linear full mode substrate integrated waveguide(FMSIW) filter and a new type of FMSIW filter bent with 90o angle have been proposed in this paper with a new type of Electromagnetic bandgap structure, etched on the PEC surface (upper layer) of the main structures to obtain the bandpass characteristics. Insertion loss is effectively low for both (180o FMSIW and 90o bent FMSIW) filters due to this distinct type of EBG structures. Outcomes of Parametric analysis of the EBG structures have also been studied and presented in graphical form. Entire experiments have been done with Neltec (NH-9320), the dielectric constant of 3.2 and thickness of 0.8 mm. Proposed filters in this paper are used for microwave Ku band applications. Both bandpass filters are compact in size, low in cost and easy to fabricate. Moreover, 90o bent filters are more convenient in use where the linear filters are restricted.

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Planar and Angular Modified Substrate Integrated Waveguide (SIW) Filter with Electromagnetic Band-Gap (EBG) Structures

S. Moitra [α], R. Dey [σ] & H. Kumar [ρ]

Abstract- Designing of 180° linear full mode substrate integrated waveguide(FMSIW) filter and a new type of FMSIW filter bent with 90° angle have been proposed in this paper with a new type of Electromagnetic bandgap structure, etched on the PEC surface (upper layer) of the main structures to obtain the bandpass characteristics. Insertion loss is effectively low for both (180° FMSIW and 90° bent FMSIW) filters due to this distinct type of EBG structures. Outcomes of Parametric analysis of the EBG structures have also been studied and presented in graphical form. Entire experiments have been done with Neltec (NH-9320), the dielectric constant of 3.2 and thickness of 0.8 mm. Proposed filters in this paper are used for microwave Ku band applications. Both bandpass filters are compact in size, low in cost and easy to fabricate. Moreover, 90° bent filters are more convenient in use where the linear filters are restricted.

Keywords: 180° linear FMSIW filter, 90° bent FMSIW filter, Ku-band, insertion loss (IL), EBG structure.

I. Introduction

Rapid development in planer components is a result of growing interest in the field of wireless component design. An effective approach in designing passive microwave component is the substrate integrated waveguide (SIW) technology. In SIW dielectric material is sandwiched between two metal conducting plates and series of vias are inserted in the other two sides thus forming a rectangular waveguide-like structure modified in planer form [1]. SIW inherits almost all of the advantages of conventional rectangular waveguide like low insertion loss, high power handling capability in the microwave band and high-quality factor. Most of the properties of SIW like dispersion characteristics, propagation constant and field pattern are similar to that of waveguide counterparts. Several passive components like antennas, filters, power dividers and couplers are designed in the recent past using the manifold benefits of SIW. Several filters [2], couplers [3], oscillators [4], slot array antennas [5], six-port circuits [6], and circulators [7] are proposed since then.

In this paper, a conventional(linear) and a 90° bent full mode SIW (FMSIW) bandpass filter embedded with new type of Electromagnetic Bandgap Structures are proposed, which exhibits the bandpass property of the microwave Ku-band.

For designing high Q-factor and low loss filters, SIW which is realized by metallic vias on low loss substrates through printed circuit board is proved to be a useful technology [8]-[10]. In SIW fabrication process takes place with using two rows of conducting cylindrical vias embedded in a dielectric substrate that connects two parallel metal plates, and permit the implementation of a classical rectangular waveguide components in planar form, along with several printed passive circuitry, active devices and antennas as shown in Fig. 1.

II. Design Equations

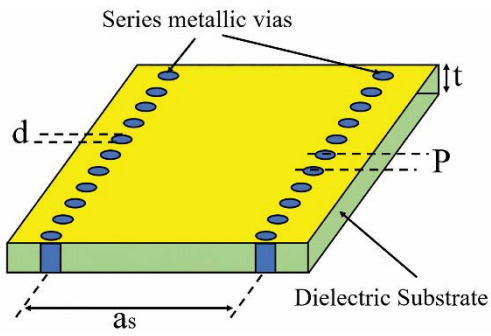

Fig. 1: Layout of Basic SIW structure realized on a dielectric substrate **(**a_s=effective width of SIW section, p=center to center gap between vias **'**pitch**'**, d=diameter of metallic vias and t=thickness of dielectric material**)**.

The basic design formulations for designing an SIW filter are as follows:

$$a_s = a_d - \frac{d^2}{0.95p} \qquad \ldots\ldots\ldots\ldots (1)$$

where, a_s is the separation between via rows (center to center), a_d is the width of the structure, d is the diameter, p is the pitch (as shown in Figure 1). The cut-off frequency of the SIW can be obtained by the following relation.

$$f_c = \frac{c}{2\varepsilon_r . a_s} \qquad \ldots\ldots\ldots\ldots (2)$$

Where c is the velocity of light in vacuum.

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III. Designing of 180° Bent FMSIW Bandpass Filter

a) 180° FMSIW Filter Design Without EBG Structures

Fig 2. and Fig 3. shows the basic 180° FMSIW structure used in designing the bandpass filter and the high pass characteristic of the basic structure respectively.

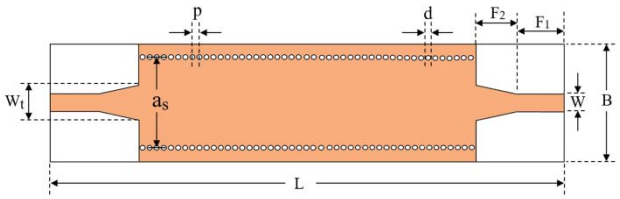

Fig. 2: Basic structures of 180° FMSIW filter **(**All dimensions are in mm**)**.

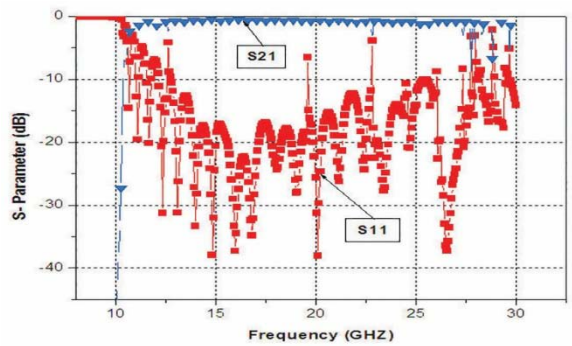

Fig. 3: Scattering Parameters of basic 180° FMSIW filter as designed on a substrate dielectric constant of 3.2 and 0.8mm thickness.

b) 180° FMSIW Filter Design With EBG Structures

The basic 180° FMSIW structure which is shown in Fig 2. acts as a high pass transmission line section. Tapered section between micro strip feed line and SIW section [14] avoids the impedance mismatch and designed as for 50Ω impedance matching. In this paper, implementation of introduced new type of EBG structures on the linear (180°) FMSIW filter creates additional resonance within the structure. Thus a considerable stop band attenuation arises in the range of Ku band with a transmission band of minimum insertion loss. The parametric analysis of EBG elements on the 180° FMSIW structure shows that the magnitude and frequency of the stop band attenuation is highly dependent on the dimension of the EBG elements. Fig 4. and Fig 5. shows the EBG loaded 180° FMSIW filter and its transmission characteristics respectively. Basic dimensional calculations can be obtained from [8].

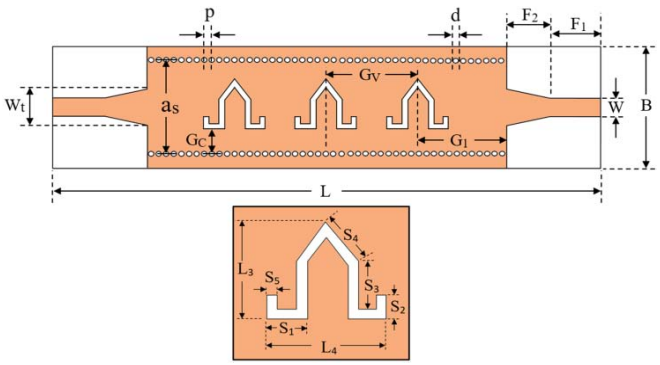

Fig. 4: 180° FMSIW bandpass filter with EBG realized on a dielectric substrate

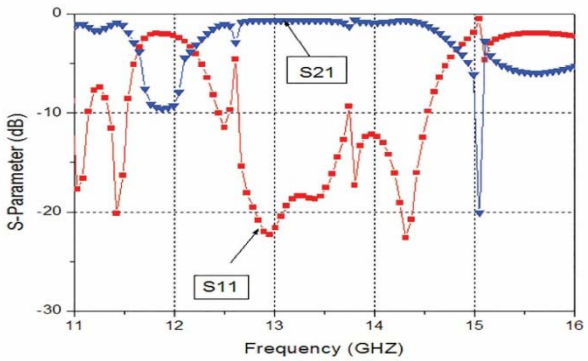

Fig. 5: Scattering Parameters of 180° FMSIW filter with EBG slots as designed on a substrate dielectric constant of 3.2 and 0.8mm thickness.

Introduction of EBG in 180° FMSIW results in production of transmission zero at around 15.04GHz, which complies the range of microwave Ku-band. The range of obtained passband is from 12.44 GHz to 14.53GHz with a minimum insertion loss of 0.71 dB. The E-field of the 180 FMSIW bandpass filter is shown in Fig 6

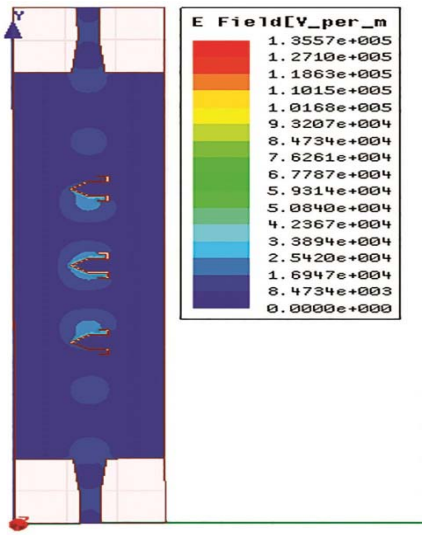

Fig. 6: E-Field distribution of EBG loaded 180° FMSIW bandpass Filter at 13.5 GHz.

Table 1: Dimensions of the 180° FMSIW filter.

Sl No.	Parameters	Without EBG Structure (mm)	With EBG Structure (mm)
1.	L	80 mm	80 mm
2.	t	0.8 mm	0.8 mm
3.	W	2.1 mm	2.1 mm
4.	B	14.6 mm	14.6 mm
5.	Wt	3.22 mm	3.2 mm
6.	F1	5 mm	5 mm
7.	F2	5 mm	5 mm
8.	d	0.6 mm	0.6 mm
9.	P	1 mm	1 mm
10.	as	8.6 mm	8.6 mm
11.	H	3 mm	3 mm
12.	S1	–	1 mm
13.	S2	–	1 mm
14.	S3	–	1.8 mm
15.	S4	–	1.2 mm
16.	S5	–	0.2 mm
17.	L3	–	4.29 mm
18.	L4	–	4 mm
19.	Gv		13.86 mm

Table 2: Performance of FMSIW Filter.

Parameters	180° FMSIW with EBG
Insertion Loss	0.66
Transmission Bandwidth	2.59 GHz
S11 (dB)	>10
S21 (dB)	<1.3
Lower Cut-off frequency 'f_L'	12.12 GHz
Higher Cut -off frequency 'f_L'	14.71 GHz

IV. Designing of 90° Bent FMSIW Bandpass Filter

a) 90° FMSIW Filter Design Without EBG Structures

In this paper, transformation of 180° FMSIW into 90° FMSIW structure was provided. For better transmission, greater bandwidth and low insertion loss the outer via series have been additionally bent in two points P_1 and P_2 by 45°. These 90° FMSIW structures exhibit similar properties with TE_{10} mode of propagation as in SIW. Fig 7. and Fig 8. shows the basic 90° FMSIW structure used in designing the bandpass filter and the high pass characteristic of the proposed structure respectively.

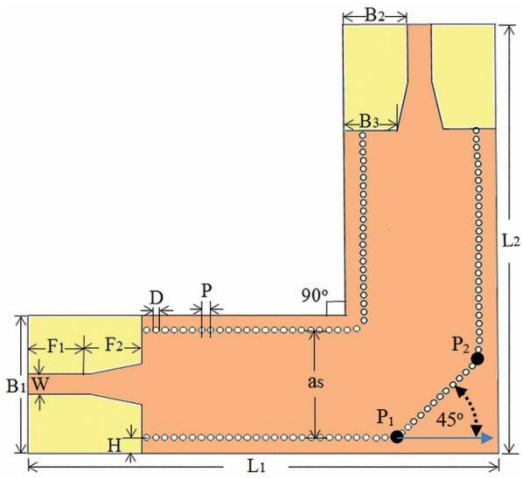

Fig. 7: Basic structures of 90° FMSIW filter (All dimensions are in mm).

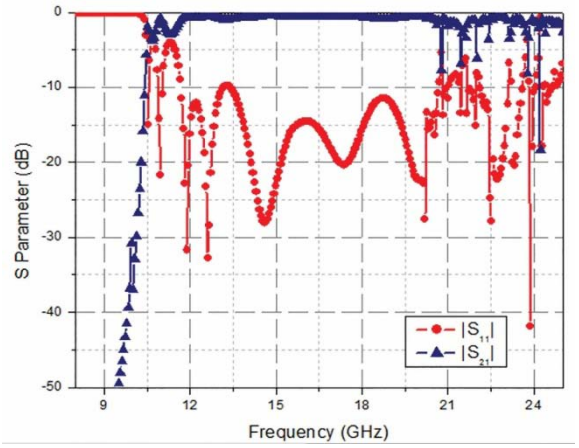

Fig. 8: Scattering Parameter of 90° FMSIW filter as designed on substrate dielectric 3.2 and thickness of 0.8mm.

a) 90° FMSIW Filter Design with EBG Structures

In this section, we have induced the EBG structures in the basic 90° FMSIW structure. In the middle section of the basic structure extra resonance will produce for bending of via rows. Thus, for etching the EBG structure denoted with 'M' in the middle region effective result will produce in terms of band width and isolation in microwave Ku band region as shown in Fig 10. Fig 9. and Fig 10. defines the EBG loaded 90° FMSIW BPF and its transmission characteristics respectively. E-field of FMSIW bandpass filter is shown in Fig.11.

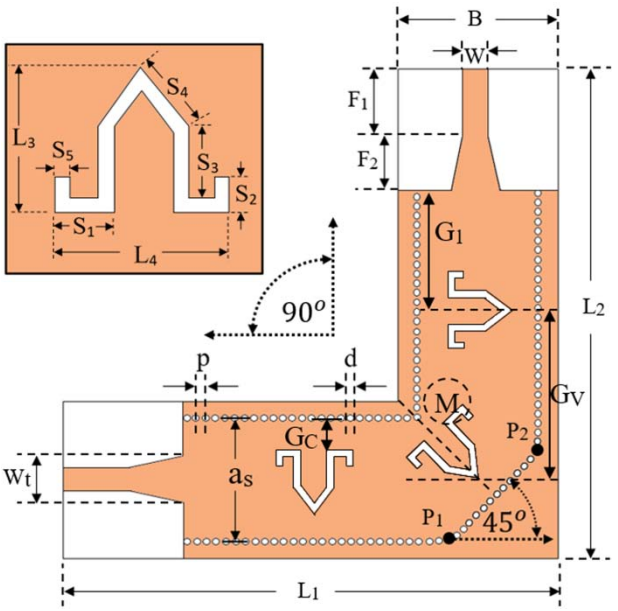

Fig. 9: 90° FMSIW bandpass filter with EBG realized on a dielectric substrate.

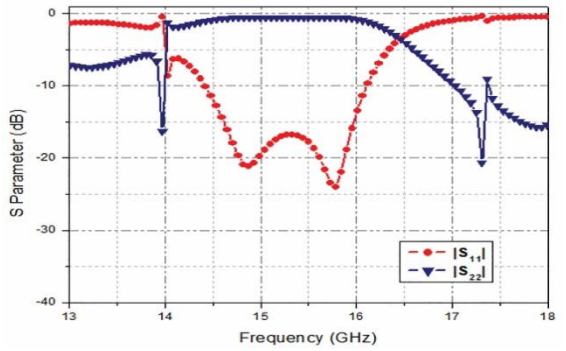

Fig. 10: S-Parameter of 90° FMSIW bandpass Filter with EBG.

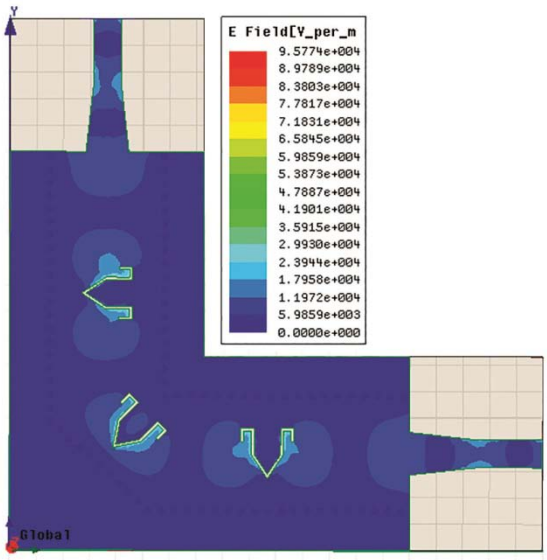

Fig. 11: E-Field of 90° FMSIW bandpass filter(15.5 GHz) with EBG realized on a dielectric substrate.

Table 3: Dimensions of the 90° bent FMSIW filter.

Sl No.	Parameters	Without EBG Structures (mm)	With EBG Structures (mm)
1.	L1	40 mm	40mm
2.	L2	40 mm	40 mm
3.	t	0.8 mm	0.8 mm
4.	W	2.1 mm	2.1 mm
5.	B	14.6 mm	14.6 mm
6.	Wt	3.22 mm	3.2 mm
7.	F1	5 mm	5 mm
8.	F2	5 mm	5 mm
9.	D	0.6 mm	0.6 mm
10.	P	1 mm	1 mm
11.	as	8.6 mm	8.6 mm
12.	H	3 mm	3 mm
13.	S1		1 mm
14.	S2		1 mm
15.	S3		1.8 mm
16.	S4		1.2 mm
17.	S5		0.2 mm
18.	L3		4.29 mm
19.	L4		4 mm
20.	Gv		7.9 mm

Bending of 180° FMSIW bandpass filter to 90° FMSIW filter results in the production of transmission zero at around 17.31GHz with a transmission bandwidth lies in the range of microwave Ku-band. The range of obtained passband is from 14.61GHz to 15.97GHz with a minimum insertion loss of 0.58 dB.

Table 4: Performance of 90° bent FMSIW Filter.

Parameters	90° FMSIW with EBG
Insertion Loss	0.58
Transmission Bandwidth	1.36 GHz
S11 (dB)	>15
S21 (dB)	<1.3
Lower Cut-off frequency 'f_L'	13.97 GHz
Higher Cut-off frequency 'f_U'	17.31 GHz

V. Parametric Analysis of EBG Structures

Microwave bandpass filter requires productive analysis of the technique to make the design effective. Several useful parameters of EBG elements are varied and the output is studied in details in this paper. Effective size of the EBG elements 'S_5' and the distance between successive EBG elements 'G_v' are studied. These parameters are found to have significant effect over the insertion loss, transmission band and isolation of the filter configurations.

a) *Parametric Analysis of EBG Structures Induced In 180° FMSIW Band Pass filter*

The effect of varying the distance of the EBG section 'G_v' with the transmission bandwidth is shown in Fig 10. It has been observed that the transmission bandwidth increases when the variation of distance takes place from 13.65mm to 13.75mm but the bandwidth decreases as we increase the distance between the EBG structures up to 13.95mm.

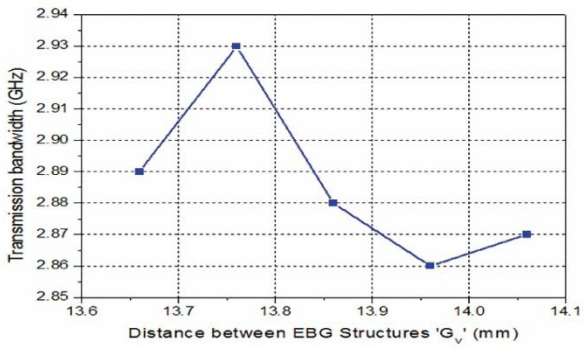

Fig. 12: Distance between EBG structures vs. Transmission Bandwidth of 180° FMSIW filter.

The distance vs. Stop band attenuation of the EBG structures is also studied to achieve greater control over the passband and loss characteristics. Fig 11. represents the variation which conveys that the stop band decreases from 16.59dB to 9.3dB as the distance increases from 13.66mm to 13.76mm but after 11.76mm the stop band attenuation increases with varying the distance by 0.1mm.

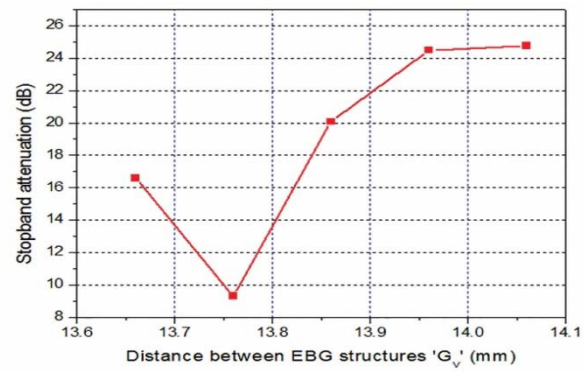

Fig. 13: Distance between EBG structures vs. Stop Band Attenuation of EBG structure of 180° FMSIW Filter.

The size of the EBG structures 'S_5' is also varied to achieve the size of EBG structure vs. transmission bandwidth and size of EBG structure vs. stop band attenuation graph to obtain greater control over passband and loss characteristics. Fig 12. shows the Size of EBG structure vs. Transmission bandwidth of EBG element. A clear observation is there that the transmission bandwidth slightly decreases when the size of the EBG element increases from 0.1mm to 0.2mm and again increases by small value when the size is increased to 0.3mm and gradually decreases as the size increases by 0.4mm.

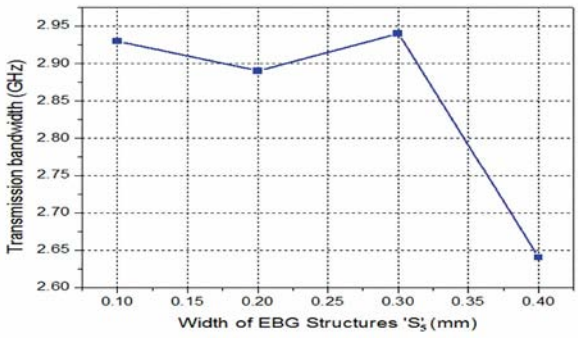

Fig. 14: Size of EBG structures vs. Transmission Bandwidth of 90° FMSIW Filter.

Fig 13. defines the size of EBG structures vs. Stop band attenuation. A clear observation is there that the stop band attenuation increases as the size increases from 0.1mm to 0.2mm but decreases as the size of EBG structure increased further.

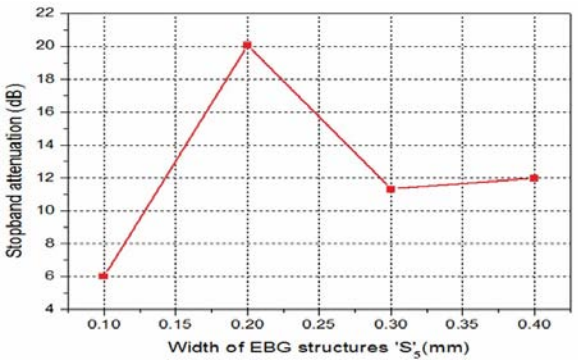

Fig. 15: Size of EBG structures vs. Stop Band Attenuation of 90° FMSIW Filter.

a) *Parametric Analysis of EBG Structures Induced In 90° bent FMSIW Band Pass filter*

The effect of varying the distance of the EBG section 'G_v' with the transmission bandwidth is shown in Fig 14. It has been observed that the transmission bandwidth is constant in a distance from 11.58mm to 11.61mm but the bandwidth decreases by 0.05 GHz as the distance increases to 11.62mm.

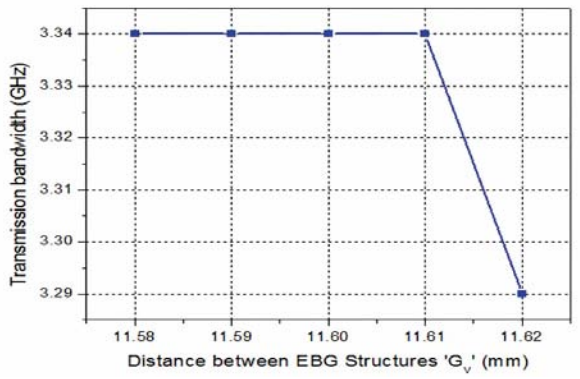

Fig. 16: Distance between EBG structures vs. Transmission Bandwidth of 90° FMSIW filter.

The distance vs. Stop band attenuation of the EBG structures is also studied to achieve greater control over the passband and loss characteristics. This variation is there in Fig 15. which shows that the stop band decreases from 28.63dB to 20.64dB as the distance increases from 11.58mm to 11.59mm but after 11.60mm the stop band attenuation increases with distance varying with 0.01mm.

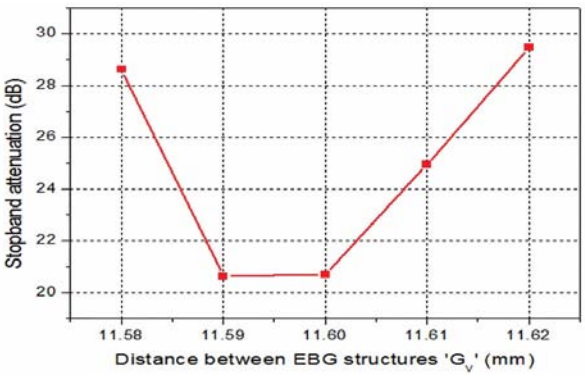

Fig. 17: Distance between EBG structures vs. Stop Band Attenuation of EBG structure of 90° FMSIW Filter.

The size of the EBG structures 'S_5' is also varied to achieve the Size of EBG structure vs. Transmission bandwidth and size of EBG structure vs. Stop band attenuation graph to achieve greater control over pass band and loss characteristics. Fig 16. shows the size of EBG structure vs. transmission bandwidth of EBG element. It can be reveals that the transmission bandwidth increases when the size of the EBG elements raises from 0.2mm to 0.3mm.

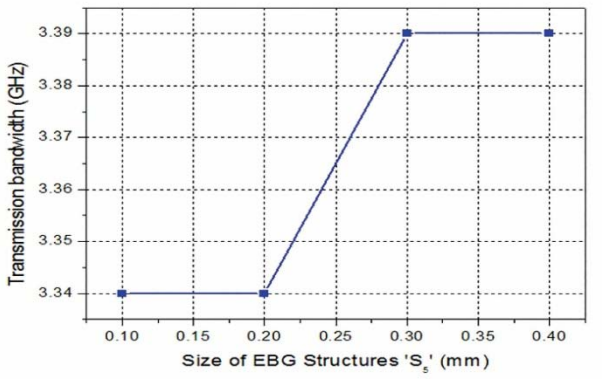

Fig. 18: Size of EBG structures vs. Transmission Bandwidth of 90° FMSIW Filter.

Fig 17. represents the variation graph of the Size of EBG structures and Stop band attenuation. It can be observe that the stop band attenuation decreases from 0.1mm to 0.2mm but increases as the size of EBG structure increases from 0.2mm to 0.4 mm.

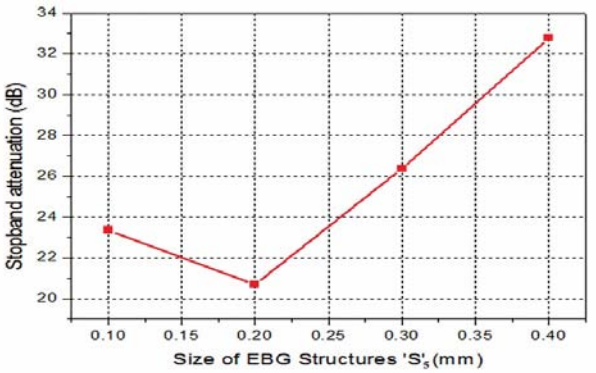

Fig. 19: Size of EBG structures vs. top Band Attenuation of 90° FMSIW Filter.

Table 2. and Table 4. represents simulated outcomes of the linear (180°) and 90° bent FMSIW filters respectively. Based on the parametric analysis presented in this paper, successfully achieves good filter performance like minimum loss and high isolation property.

VI. Conclusion

In this article, a brief discussion is there for obtaining the bandpass characteristics of 180° FMSIW filter and 90° FMSIW filter. 180° FMSIW filter loaded with EBG structures bent down to 90° and analyzed the bandpass characteristics for obtaining the desired passband. Bending of 180° FMSIW filter to 90° FMSIW filter and implementation of EBG structures on both designs are found to serve the purpose quite effectively. For better understanding, a detailed presentation for the analyses of several useful parameters of the EBG elements is there. Additionally, with bending the linear filter, length has been decreased. Thus, 90° bent filters are more flexible than linear 180° filters regarding the use and bandpass characteristics. Distance and size of

EBG elements can be chosen to achieve a better result. In future, both filters can be used for such applications (radar and remote sensing operations) which complies the range of Ku band. Moreover, 90° bent filters have the advantage to minimize the space complexity using its bending strategy and novel passband characteristics. Both designs are simple and easy to fabricate in the presence of advanced fabrication technology.

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Technopreneurship: A View of Technology, Innovations and Entrepreneurship

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Technopreneurship: A View of Technology, Innovations and Entrepreneurship

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Abstract- There is a strong connection between Technological development, Innovations and entrepreneurship. It is noteworthy that, entrepreneurship forms the sub structure upon which science and technology are built. As we understand it, technopreneurship is, by a large part, still entrepreneurship. The difference is that technopreneurship is either involved in delivering an innovative hi-tech product (e.g. Microsoft) or makes use of hi-tech in an innovative way to deliver its product to the consumer (e.g. eBay), or both (e.g. most pharmaceutical companies). Technopreneurship is not a product but a process of synthesis in engineering the future of a person, an organization, a nation and the world. Strategic directions or decision-making processes are becoming more demanding and complex. This requires universities, and in site professional development programs and training to produce strategic thinkers who will have skills to succeed in a rapidly changing global environment.This paper has brought to the fore the need for countries to put forward , realize and promote technopreneurship as a way of technological advancementin the modern age, as it asserts that entrepreneurship must be the sole baseof innovation in the world of science and technology; only then can technological innovations be valuable to the pursuit of economic development. While the strength and growth of any economy is facilitated by the civil entrepreneurial culture and the versatility of its technical know-how, this paper focus on the relevance of adopting technopreneurship as a way of societal development, thus establishing the inter-relationship between the scientist, engineers and the business sector with aim of enhancing proficiency in research and development.

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I. Introduction

In this world of accelerating economic globalization, advances in science and technology continue in the blink of an eye, and knowledge is recognized as a core competence in accumulating wealth (Lalkaka, 2002). he latter half of the 20th century has seen science and technology compliment land, labor, and capital as sources of wealth (Etzkowitz, 2003a). Correspondingly, knowledge and innovation have come to be recognized as factors of production (O'Shea, Allen, Morse, O'Gorman, & Roche, 2007). The art of entrepreneurship has the potential to ignite knowledge and innovation within the IT industry. In this environment, then, the question becomes how best to harness and capitalize on knowledge and innovation. With the advent of the internet, the information age has become an opportunistic environment for entrepreneurs. The rapid evolution of technology in the last fifty years plays a significant role in our day to day lives. Information Technology (IT) builds and supports the processes of organizations on a competitive global platform. The shift from the physical world to the virtual world is also a noticeable trend as an increasing number of everyday functions and processes are shifting to an electronic realm. Traditionally, IT entrepreneurship has been most successful and lucrative in most parts of the world. Around the world, we can see that nations have embraced information and communication technology (ICT) as a means to enrich public and private sector processes, while providing citizens with easier access to these services (Fang, 2002).The emergence of technological innovations has opened up to new opportunities and challenges to a nation's economic development (Yunos, 2002). It is worth to mention that information technology has becoming an important fact to the business community as it helps improve the business processes.

The term "technopreneurs" means technology entrepreneurs, which are basically the big, small and medium enterprise ICT and multimedia companies. Focusing on these various enterprises, advancements in ICT and technological adoption will provide channel to accelerate and expand businesses as well as its people, which bears vital importance to the growth and development of entrepreneurs in the knowledge-based economy. Besides daily advancements to better structures and strategies are being explored and developed to help technology-based enterprise grow especially the small and medium ones offering a promising future within the global marketplace, thereby being able to expand themselves to compete in this borderless world, at the same time create, and add value to their business in order to achieve sustainability.

a) Nigeria's Experience

The history and development of technopreneurship in Nigeria is linked to the entre preneurship development process. Prior to 1970 the role of government was not significant till 1986 after the introduction of Structural Adjustment Program (SAP) which was subsequently followed by the establishment

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of the Small Scale Industries Credit Guarantee Scheme (SSICS), National Directorate of Employment (NDE), National Open Apprenticeship Scheme (NOAS), Small and Medium Enterprise Development Agency of Nigeria (SMEDAN),as well as Centre for Entrepreneurship Development (CED), National Centre for Technology Incubation(NCTI). The process received a major boost with the introduction of privatization and commercialization decrees in 1988 - 1995 resulting in the emergence of business enterprises in the fields of agriculture, manufacturing, banking, mining, education, publishing, and information & communication technology. This development provided the fertile ground needed for the emergence of micro, small and medium enterprises that are engaged in the production and provision of auxiliary products and services. The role of Government became much more apparent through the activities of SMEDAN by supporting and supervising entrepreneurship units while the Central bank of Nigeria provides financial assistance to entrepreneurs through the 10% fund contribution by commercial banks to the Small and Medium Enterprise Equity Investment Scheme (SMEEIS).As noted by Babajide, "the scheme aimed at assisting the establishment of new, viable small and medium industries; thereby stimulating economic growth, and development of local technology, promoting indigenous entrepreneurship and generating employment".

II. Literature Review

The emergence of technology and the innovations it brought has opened up new opportunities and challenges into businesses in this regard, technological adoption and advancement act as channel to expand and accelerate the businesses as well as the people. Lalkaka (2002) defined technological innovation as the process that drives a concept towards a marketable product or service. This holds true as it contributes towards raising productivity and competitiveness (Lalkaka, 2002).

Technopreneurship is innovative application of technical science and knowledge individually or by a group of persons, who create and manage a business and take it financial risk in order to achieve their goals and perspectives. The engineers possess high technical skills in this regard but they often enjoy few skills in business and in terms of entrepreneurial thinking (Prodan ,2007). Technopreneurship is one of the basic foundation areas of the ICT age in entrepreneurship that plays important role in creation of competitive advantage in various enterprises and organizations, reconstruction and economic growth being basic reasons for this, businesses will be able to expand themselves to compete in this ever expanding world, at the same time create and add value to them(businesses) in order to achieve sustainability. Today, it is completely clear that according to a report from OECD, development of technology play an essential role in economic growth and development and technology oriented industries may play ever-increasing and major role in international trade. While emerging technopreneurship may cause ever-growing appearance of knowledge based SMEs (Dahlstrand, 2007). Technopreneurship as a leadership style of business including identifying extremely technological economic opportunities with high capacity for growth, collection of resources like expert manpower and capital, rapid growth and remarkable risk management by means of decision making skills (Dorf, R.C., & Byers 2005). The rapid advancement of technology has encouraged small and medium-sized businesses (SMEs) to utilize the opportunity to establish, expand, as well as prosper their businesses capable of generating employment opportunities, mobilizing the local resources, creating a balanced and affluent society and playing a significant complementary role to large firms and eventually strengthening the economic development of the nation as a whole (APEC, 2001)

III. Definition of Technopreneurship

Technopreneurship is a latent concept that is placed in the core of many fundamental subjects. Various literatures use the term "technology-based entrepreneurs", "technical entrepreneurs", "high technology entrepreneurs" or even "high tech new ventures" to describe new business that combine entrepreneurial skills and technology (Florida and Kenney, 1988; Dahlstr and and Lindholm, 1999; Renko, Autio and Tontti, 2002 ; Oakey, 2003; Kakati, 2003) Technopreneurship comprises of identifying modern technologies and even creation of technological opportunities by presentation of commercial products and services (Blanco,2007). Technology -based entrepreneur is a process and formation of a new business that involves technology and these "technopreneurs" use technological innovations and translate such technology into successful products or services. Technopreneurship is the process of investing in a project which gathers and activate expert members with different assets, which relates to advancement in scientific and technological knowledge, in order to create and acquire value for a specific enterprise, the social context in which the entrepreneur operates also plays an important role in nurturing this concept, one of such ways is through embeddedness, where entrepreneurs are being embedded within the confined structure in the area in which they operate. Objective of technopreneurship is commercialization of innovations developed by academic scientists via patenting, licensing, start-up creation, and university–industry partnerships

(Grimaldi et al., 2011). Entrepreneurs who are into the core businesses involving technology - based industries and make use of technology to come out with new or innovative products through a process of commercialization are technopreneurs. Their businesses are generally marked with high growth potential and high leverage of knowledge and intellectual property. Potential Technopreneurs must be equipped with both technical and business skills. Generally, technopreneurs possess high technological knowledge deprived from relevant skills of business (i.e. financial experiences and data), and achievement in technological enterprises. Techniques and technology are deemed as some part of innovation. Technopreneurship process is mainly related to technological innovations, where technology may be utilized as a system of theoretical and operational knowledge and skills by enterprises for development, production, and delivery of their products and services so that it could be defined and embodied in personnel, materials, facilities, equipment, and physical procedures and processes. In general from their viewpoint, technopreneurs possess a lot of technical knowledge but they lack of entrepreneurial necessary skills for management, duration, and success in organizations and this has led to reduced efficiency in technology base organizations and enterprises (Antonici & Prodan, 2007). Techno-preneurship will be placed in the development path when the relationship among micro and macro factors is being addressed between technological opportunities and entrepreneurial performance. In a study conducted by Petti and Zhang (2011), corporate technopreneurship is included in a system of internal entrepreneurial processes and the related strategic capabilities respectively including identifying, discovering, and creation of technological opportunities and development of values that enable innovative business models to exploit from these opportunities. More clearly, it is to search for opportunities and budgeting for investment and covers entrepreneurial tendency. Knowledge management covers capacity for attraction and manages the relevant change to innovation of business model and incorporates dynamic capability that is aimed at creation of competitive advantage in organizational environment.

The suggestion that there is a strong and positive correlation between technopreneurship and the growth of enterprises has certainly been discussed in literature since the early works on entrepreneurship and economic development by Schumpeter. It is widely accepted that an increase in the number of technopreneurs leads to an increase in enterprise growth which is also a direct result of their skills, and their tendency to innovate. Their ability to generate enterprise growth in a particular economy is normally manifested in their innovative capability, as described by introducing new goods and services which are not familiar to consumers, new quality, new method of production, opening of a new market, and capture of a new source of supply of raw materials or other inputs. The obvious ability and willingness of entrepreneurs (who anchor their business thrust on technology) to practically perceive and create new business opportunities and decide to venture in to such opportunities in spite of the challenges of market uncertainties and other impediments, affect and ultimately renew the business activities, not only within their business units and industries, but also within the economy they are situated. The culmination of various technopreneural initiatives with the occurrence of a variable with a differing role in an aggregated form could result in general enterprises growth which, to a greater extent, can be measured in terms increase in competiveness, market share, quality, profitability, and innovation gained by the business units. The influence of this is normally driven by their activities in provision of a wide range of services. Investment-generated innovative services are associated with lower transaction costs and, therefore, greater efficiency, competiveness, market growth as well as increased earnings. Consequently, absences of funds yield little room for opportunities in terms of increased innovative activities. Expectedly, given the abundant natural resource and cheap labour in Nigeria, the technopreneurs will be able to help build a significant cluster of viable ideas and business schemes in order to develop a number of excellent enterprises in Nigeria. The technopreneurs will be able to manifest characteristics such as product and process innovativeness, high growth rate, technology adoption, and high market growth rate. This could contribute significantly to the business as well as economic growth through value addition, wealth creation and job opportunities. Therefore there is strong positive relationship between innovative services, technopreneurship and enterprise, also the growth of technoprenuership drive and SMEs significantly depend on the availability and accessibility innovative services. Innovative entrepreneurship is becoming the corners tone of economic growth in the developed and developing world. Government and the industry can create the plat forms that tap in to people's creativity in what ever way it is expressed, rather than regarding innovation as the domain of asm allh and ful of people. Industries in the developed world spend huge sumannually on research and development, with the eye to fostering innovation and aculture of risk and reward (Cukier, 2006).

a) Competition and Progress in the Technopreneurs' world

Competition is the process of trying to dobetter than others. In the world today, people and organizations face a common global problem which is

the need to improve in performance so as to adapt to the fast paced global changes. People and organization who deliberately innovate, or make continuous changes in their products and processes, has a hugegap in the world of information and communication technology. The basic key to maintaining competitiveness lies in the ability to change and improve what we do and how we do it. According to Paul Mott-University of Pennsylvania, in the world of competition, an effective organization, institutions etc. displays three characteristic simultaneously(Molt, 1972). The seare:

*Efficiency:*This is the optimal use of services to create a well structural, stable, routine in product in high quantities, quality and at low cost. In this world of advance technology, efficiency alone is not enough to meet the global market(Molt, 1972).

Adaptability: A daptability means mastering; Innovation is the key to Adaptability. Itrequires looking for new technologies, ideas and methods that may improveor completely change a process routine to match the demands of the technological world. Adaptability also involves processes based on knowledge acquired from an earlier work done. Adaptability helps you not just to reproduce but to improve on an existing model so as to meetthedem and of clients. This means that as techno-preneurs, we must not just study the technology of product and services but we must study the market so as to adapt the innovation to meet the market demand. In other words we must main stream innovation (Molt, 1972).

Flexibility: This is the ability of an organization to react to unexpected emergencies quickly while still maintaining it' sroutine. It'snolongerenough to relysolely on flexibility in order to cope with change, anticipating a change by "leapfrogging" bringing to the market goods and services that meet the needs of the consumer to them even before the consumer envisage the change.

SME shave unique characteristics and due to these characteristics, it is conclusive to say they have inherent capabilities to undertake technological innovations successfully across specialized field and economy. As there is adequate empirical evidence to shed light on SME innovation and its contributions in the context of developed countries, in light of this, there is hardly any proof of evidence showing innovative SMEs are rapidly industrializing economies like Nigeria. This paper takes into consideration deep rooted findings of two empirical "Innovation Projects" implemented in Lagos based on the last few years, specifically the Ikeja and Victoria-island regions. In today's economy, SMEs are largely incremental innovators, due to the effects of their customers and their involvement in the said products and/or process innovations. Majority of these SME's carried out their innovations with internal efforts only, only a few/minority obtained external support to carry out its innovations, the latter had better technical strength and frequent analysis on outcomes for both product &process innovations. Such SMEs achieved better innovation performance as well as better economic performance.

The Economy grows better innovation performance as well as better economic performance rapidly if entrepreneurs make remarkable progress in various industries like Manufacturing, Precision Engineering Design, Food Processing, Pharmaceutical, Textile &Garments, Retail, IT and ITES, Agro and Service sector and can be achieved with the following:

(i) Innovations: How creative is the product
(ii) Quality of innovations: How valuable standard is the product
(iii) Patenting culture: How to protect and secure that Standard.

The elements of creativity are sometimes generalized as cognitive, affective, personal and motivational, and social or environmental. Among these, cognitive and affective elements are arguably most important. The cognitive aspects of creativity include basic knowledge (both general and field-specific), perceptiveness, originality, attraction to complexity (e.g., combining, analyzing, and applying different, disparate ideas or concepts), open-mindedness (e.g., resistance to closure, and awareness of creativity. Affective elements includecuriosity, humor, independence, and risk-taking.

IV. Challenges to Technopreneur

In the new age of IT, great exploits in innovations research and development hasn't been without its negatives and disadvantage. These hindering factors include: government policy, human capacity development, lack of facilities, and lack of standard for confirmation, capital, market and energy. Research innovation is generally not appreciated, so less investment would lead to less develop ment breakthrough in products. Instead of being trend setters, they choose the easier option which is to follow trends.

V. Role of Government

Government roles in supporting technopreneur-ship comes in various forms directly and indirectly, indirectly by enacting favorable regulation and public policies for creating conducive economic system for technopreneurship to grow and directly by providing risk capital. Venkataram an(2004) clearly believed that some kind of intervention was necessary for encouraging technopreneurship. However, if government attempted to provide the intangible infrastructure, an entitlement mentality would emerge. On the other hand, markets or private institutions have not always solved problems effectively and efficiently. Both independent on each other would crash.

The governments basically promote technopreneurship by injecting risk capital; this alone does not provide encouraging results. It should be noted that massive interventions may increase dependency of technopreneurship to government aids, which cannot be sustainable in the long term. Government intervention should be comprehensively analyzed and carefully designed to focus on developing technologies that are relevant to the needs of potential users, technically reliable, and economically competitive. Availability of desirable technologies is a pre-requisite for technopreneurship to be viable. It will be extremely challenging to encourage technopreneurship if business enterprises are not interested in indigenous technology developed domestically. Growth and transformation spinoff firms will also be very difficult, no matter what or how much incentives provided by government.

With all these factors coupled with the fact that technology is research based and developmental and so as to sustain its existence as well as the global business practice, solution in the positive direction is imperative, a fulcrum for development is needed. Creativity training and entrepreneurial skills is needed combined with experiences. The intellect is within us, technology is here to stay. Promoting innovative entrepreneurship should thus be central concern for policymakers. Itrequires that government officials themselves act as technopreneur in implementing policies, and promoting new partnerships with the stakeholders. The success of future innovators as well as the future sole depends on whether the government is ready to do this bidding and accept the task ahead. Technologi calinnovationsem power us and grow the economy.

VI. Conclusion

Technopreneurship is the process organizational creativity it is also aprocess of main streaming innovation to continually find solution to important corporate problems and implementing the solutions to, in turn satisfying the economy or target. It also laysemphasis on integrating technology with entrepreneurship. Technopreneurs are entrepreneurs who are into the intimate business of technology based industries. They make use of technology to come up with innovative eproducts through commercialization.

Aspiring technopreneurs mustbe adequately equipped with both technical and business skills. Technopreneurs continually go through the process of constant improvement and always try to redefine our dynamic digital economy. We need to encourage entrepreneurial views and skills at all levels of the society.

VII. Concluding Remarks

There is no denying it that technopreneurship must be encouraged, nurtured and facilitated. But however, all aspects of technopreneurship should be extensively examined and vetted so as to fully understand the challenges it brings in every phase of the technopreneurship development. Enacted policies in developing technologies should be properly directed and their Research and development capacity should be continuously improved such that they will be able to create relevant technologies to always suit user's needs, technically reliable, and economically competitive. Relevant, reliable, and competitive technologies are pre-requisite for a successful technology transfer. Also the absorbing capacity of existing business enterprises needs to be improved. All the above said submission will not only just increase technological demand but the economy as a whole, technopreneurship will be viable and be a major contributing factor to the realization of indigenous technologies to social and economic developments.

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Note :

"

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1. General,

2. Ethical Guidelines,

3. Submission of Manuscripts,

4. Manuscript's Category,

5. Structure and Format of Manuscript,

6. After Acceptance.

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· Use present tense to report well accepted

· Use past tense to describe specific results

· Shun familiar wording, don't address the reviewer directly, and don't use slang, slang language, or superlatives

· Shun use of extra pictures - include only those figures essential to presenting results

Title Page:

Choose a revealing title. It should be short. It should not have non-standard acronyms or abbreviations. It should not exceed two printed lines. It should include the name(s) and address (es) of all authors.

Abstract:

The summary should be two hundred words or less. It should briefly and clearly explain the key findings reported in the manuscript--must have precise statistics. It should not have abnormal acronyms or abbreviations. It should be logical in itself. Shun citing references at this point.

An abstract is a brief distinct paragraph summary of finished work or work in development. In a minute or less a reviewer can be taught the foundation behind the study, common approach to the problem, relevant results, and significant conclusions or new questions.

Write your summary when your paper is completed because how can you write the summary of anything which is not yet written? Wealth of terminology is very essential in abstract. Yet, use comprehensive sentences and do not let go readability for briefness. You can maintain it succinct by phrasing sentences so that they provide more than lone rationale. The author can at this moment go straight to shortening the outcome. Sum up the study, with the subsequent elements in any summary. Try to maintain the initial two items to no more than one ruling each.

- Reason of the study - theory, overall issue, purpose
- Fundamental goal
- To the point depiction of the research
- Consequences, including definite statistics - if the consequences are quantitative in nature, account quantitative data; results of any numerical analysis should be reported
- Significant conclusions or questions that track from the research(es)

Approach:

- Single section, and succinct
- As a outline of job done, it is always written in past tense
- A conceptual should situate on its own, and not submit to any other part of the paper such as a form or table
- Center on shortening results - bound background information to a verdict or two, if completely necessary
- What you account in an conceptual must be regular with what you reported in the manuscript
- Exact spelling, clearness of sentences and phrases, and appropriate reporting of quantities (proper units, important statistics) are just as significant in an abstract as they are anywhere else

Introduction:

The **Introduction** should "introduce" the manuscript. The reviewer should be presented with sufficient background information to be capable to comprehend and calculate the purpose of your study without having to submit to other works. The basis for the study should be offered. Give most important references but shun difficult to make a comprehensive appraisal of the topic. In the introduction, describe the problem visibly. If the problem is not acknowledged in a logical, reasonable way, the reviewer will have no attention in your result. Speak in common terms about techniques used to explain the problem, if needed, but do not present any particulars about the protocols here. Following approach can create a valuable beginning:

- Explain the value (significance) of the study
- Shield the model - why did you employ this particular system or method? What is its compensation? You strength remark on its appropriateness from a abstract point of vision as well as point out sensible reasons for using it.
- Present a justification. Status your particular theory (es) or aim(s), and describe the logic that led you to choose them.
- Very for a short time explain the tentative propose and how it skilled the declared objectives.

Approach:

- Use past tense except for when referring to recognized facts. After all, the manuscript will be submitted after the entire job is done.
- Sort out your thoughts; manufacture one key point with every section. If you make the four points listed above, you will need a least of four paragraphs.

- Present surroundings information only as desirable in order hold up a situation. The reviewer does not desire to read the whole thing you know about a topic.
- Shape the theory/purpose specifically - do not take a broad view.
- As always, give awareness to spelling, simplicity and correctness of sentences and phrases.

Procedures (Methods and Materials):

This part is supposed to be the easiest to carve if you have good skills. A sound written Procedures segment allows a capable scientist to replacement your results. Present precise information about your supplies. The suppliers and clarity of reagents can be helpful bits of information. Present methods in sequential order but linked methodologies can be grouped as a segment. Be concise when relating the protocols. Attempt for the least amount of information that would permit another capable scientist to spare your outcome but be cautious that vital information is integrated. The use of subheadings is suggested and ought to be synchronized with the results section. When a technique is used that has been well described in another object, mention the specific item describing a way but draw the basic principle while stating the situation. The purpose is to text all particular resources and broad procedures, so that another person may use some or all of the methods in one more study or referee the scientific value of your work. It is not to be a step by step report of the whole thing you did, nor is a methods section a set of orders.

Materials:

- Explain materials individually only if the study is so complex that it saves liberty this way.
- Embrace particular materials, and any tools or provisions that are not frequently found in laboratories.
- Do not take in frequently found.
- If use of a definite type of tools.
- Materials may be reported in a part section or else they may be recognized along with your measures.

Methods:

- Report the method (not particulars of each process that engaged the same methodology)
- Describe the method entirely
- To be succinct, present methods under headings dedicated to specific dealings or groups of measures
- Simplify - details how procedures were completed not how they were exclusively performed on a particular day.
- If well known procedures were used, account the procedure by name, possibly with reference, and that's all.

Approach:

- It is embarrassed or not possible to use vigorous voice when documenting methods with no using first person, which would focus the reviewer's interest on the researcher rather than the job. As a result when script up the methods most authors use third person passive voice.
- Use standard style in this and in every other part of the paper - avoid familiar lists, and use full sentences.

What to keep away from

- Resources and methods are not a set of information.
- Skip all descriptive information and surroundings - save it for the argument.
- Leave out information that is immaterial to a third party.

Results:

The principle of a results segment is to present and demonstrate your conclusion. Create this part a entirely objective details of the outcome, and save all understanding for the discussion.

The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

Content

- Sum up your conclusion in text and demonstrate them, if suitable, with figures and tables.
- In manuscript, explain each of your consequences, point the reader to remarks that are most appropriate.
- Present a background, such as by describing the question that was addressed by creation an exacting study.
- Explain results of control experiments and comprise remarks that are not accessible in a prescribed figure or table, if appropriate.
- Examine your data, then prepare the analyzed (transformed) data in the form of a figure (graph), table, or in manuscript form.

What to stay away from

- Do not discuss or infer your outcome, report surroundings information, or try to explain anything.
- Not at all, take in raw data or intermediate calculations in a research manuscript.
- Do not present the similar data more than once.
- Manuscript should complement any figures or tables, not duplicate the identical information.
- Never confuse figures with tables - there is a difference.

Approach

- As forever, use past tense when you submit to your results, and put the whole thing in a reasonable order.
- Put figures and tables, appropriately numbered, in order at the end of the report
- If you desire, you may place your figures and tables properly within the text of your results part.

Figures and tables

- If you put figures and tables at the end of the details, make certain that they are visibly distinguished from any attach appendix materials, such as raw facts
- Despite of position, each figure must be numbered one after the other and complete with subtitle
- In spite of position, each table must be titled, numbered one after the other and complete with heading
- All figure and table must be adequately complete that it could situate on its own, divide from text

Discussion:

The Discussion is expected the trickiest segment to write and describe. A lot of papers submitted for journal are discarded based on problems with the Discussion. There is no head of state for how long a argument should be. Position your understanding of the outcome visibly to lead the reviewer through your conclusions, and then finish the paper with a summing up of the implication of the study. The purpose here is to offer an understanding of your results and hold up for all of your conclusions, using facts from your research and generally accepted information, if suitable. The implication of result should be visibly described. Infer your data in the conversation in suitable depth. This means that when you clarify an observable fact you must explain mechanisms that may account for the observation. If your results vary from your prospect, make clear why that may have happened. If your results agree, then explain the theory that the proof supported. It is never suitable to just state that the data approved with prospect, and let it drop at that.

- Make a decision if each premise is supported, discarded, or if you cannot make a conclusion with assurance. Do not just dismiss a study or part of a study as "uncertain."
- Research papers are not acknowledged if the work is imperfect. Draw what conclusions you can based upon the results that you have, and take care of the study as a finished work
- You may propose future guidelines, such as how the experiment might be personalized to accomplish a new idea.
- Give details all of your remarks as much as possible, focus on mechanisms.
- Make a decision if the tentative design sufficiently addressed the theory, and whether or not it was correctly restricted.
- Try to present substitute explanations if sensible alternatives be present.
- One research will not counter an overall question, so maintain the large picture in mind, where do you go next? The best studies unlock new avenues of study. What questions remain?
- Recommendations for detailed papers will offer supplementary suggestions.

Approach:

- When you refer to information, differentiate data generated by your own studies from available information
- Submit to work done by specific persons (including you) in past tense.
- Submit to generally acknowledged facts and main beliefs in present tense.

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Abstract	Clear and concise with appropriate content, Correct format. 200 words or below	Unclear summary and no specific data, Incorrect form Above 200 words	No specific data with ambiguous information Above 250 words
Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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