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# Electronically Tunable Third-Order Switched-Capacitor Filter with Feedforward Signal to Minimize Overshoot

By Adnan Abdullah Qasem & G. N. Shinde

*SRTM University, India*

**Abstract-** The study proposes an Electronically Tunable Third-Order Switched-Capacitor Filter with Feedforward Signal to minimize Overshoot Configuration. This circuit is designed for center frequency  $f_0=15$  KHz. The proposed circuit discusses a new configuration to realize third-order with three filter functions low-pass, band-pass, and high-pass simultaneously in single circuit. The circuit uses OP-AMP and MOSFET with Capacitor as Switched-Capacitor. The response of circuit is studied for different circuit merit factor Q and center frequency  $f_0=15$  KHz. The filter circuit can be used for both narrow as well as for wide bandwidth, Also, this circuit works for electronically tunable bandwidth. The gain roll-off for this circuit is close to the ideal value of 18 dB / octave (40dB/ decade) as for third order filters. This filter configuration shows better response for  $Q \geq 0.4$ . Also, stabilization of gain for High-pass filter function can be achieved at 0dB for  $Q \geq 0.4$ . In the proposed circuit configuration, the peak gain for overshoot is minimizing from 44dB to 5dB due to the feedforward input signal. The Low-pass filter function works practically only for higher merit factor Q. The circuit shows better response for  $Q \geq 0.4$  and  $f_0 = 15$  kHz.

**Keywords:** *electronically tunable, third-order switched-capacitor, pass band, merit factor q, cut-off frequency.*

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# Electronically Tunable Third-Order Switched-Capacitor Filter with Feedforward Signal to Minimize Overshoot

Adnan Abdullah Qasem<sup>a</sup> & G. N. Shinde<sup>σ</sup>

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**Keywords:** electronically tunable, third-order switched-capacitor, pass band, merit factor q, cut-off frequency.

## I. INTRODUCTION

Conventional analog circuits use the ratio of resistances to set the transfer function of filter circuits. The values of RC product determine the frequency responses of these circuits [1-2]. A switched-capacitor can replace a resistor [2]. MOSFET technology can be used for designing switched-capacitor circuits [3]. The filter circuits using Switched-Capacitor allow very sophisticated, accurate and tunable analog circuits to be manufactured. Many of the circuits proposed the working of only one type of operation [5- 10]. The Switched-Capacitor concept can be used to realize wide variety of universal filter that have the advantage of compactness and tenability [5]. Switched capacitor techniques have been developed so that both digital and analog functions can be integrated on a single silicon chip. Switched-Capacitor filters have the advantage of better accuracy in most cases. Typical center frequency accuracies are normally on the order of about 0.2% for most Switched-Capacitor ICs, and

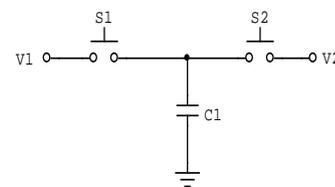
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worst-case numbers range from 0.4% to 1.5% (assuming, of Course, that an accurate clock is provided) [6]. This Paper of Electronically Tunable Third-Order Switched-Capacitor Filter with Feedforward Signal to minimize Overshoot has been studied for different values of circuit merit factor Q and  $f_0=15$  KHz .

## II. BASIC SWITCHING OPERATION

The essence of the Switched-Capacitor is the use of Capacitors and analog Switches to perform the same function as resistors. This replacement of resistor, analog with op. amp based integrator, and then forms an active filter. Furthermore, the use of the Switched-Capacitor will be seen to give frequency tenability to active filters. Filter using Switched-Capacitor technique overcome a major obstacle of filter on a chip fabrication—the implementation of resistors by simulating resistors with high speed Switched-Capacitors using MOSFETs. The switching function of the MOSFET produces a discrete response rather than a continuous response from the filter [14]. The operation of switched-capacitor can be explained with the help of following circuit diagram.



*Figure 1 :* Circuit diagram for operation of the switched-capacitor

Since the charge  $q$  on a capacitor  $C_1$  is given by

$$q = C_1 V$$

Where  $V$  is the voltage across the capacitor  $C_1$ .

Therefore, when  $S_2$  closes with  $S_1$  open, then  $S_1$  closes with  $S_2$  open a charge  $q$  is transferred from  $V_2$  to  $V_1$  with

$$\Delta q = C_1 (V_2 - V_1)$$

If this switching process is repeated  $N$  times in time ( $t$ ), then the amount of charge transferred per unit time is given by

$$\frac{\Delta q}{\Delta t} = C_1(V_2 - V_1) \frac{N}{\Delta t}$$

L.H.S. is current and number of cycles per unit time is switching frequency.

$$\therefore i = C_1(V_2 - V_1) f_{clk}$$

$$\therefore \frac{(V_2 - V_1)}{i} = \frac{1}{C_1 f_{clk}} = R$$

Thus the switched-capacitor is equivalent a resistor.

### III. PROPOSED CIRCUIT CONFIGURATION

The proposed circuit configuration for Electronically Tunable Third-Order Switched-Capacitor Filter with Feedforward Signal to minimize Overshoot is shown in Figure 2. The circuit consists of three op-amps ( $\mu A$  741) with wide identical gain bandwidth product (GB) and four Capacitors with MOSFET, which form Switched-Capacitor. Switched-Capacitor can replace resistors, which was proposed earlier [2]. The input sinusoidal voltage is applied to the inverting terminal of the first op-amp through switched capacitor (SC). The non-inverting terminal is grounded. SC is used in the feedback circuit. The output of the first op-amp is supplied as non-inverting input of the second op-amp. The feedforward input signal is given to the inverting terminal of the second op-amp. SC is used as feedback. The output of the second op-amp is supplied as non-inverting input of the third op-amp. The inverting terminal is grounded. SC is used as feedback. Low-pass function is observed at the output of the third op-amp. The output of the second op-amp gives Band-pass function. The High-pass function is seen at the inverting input of the first op-amp.

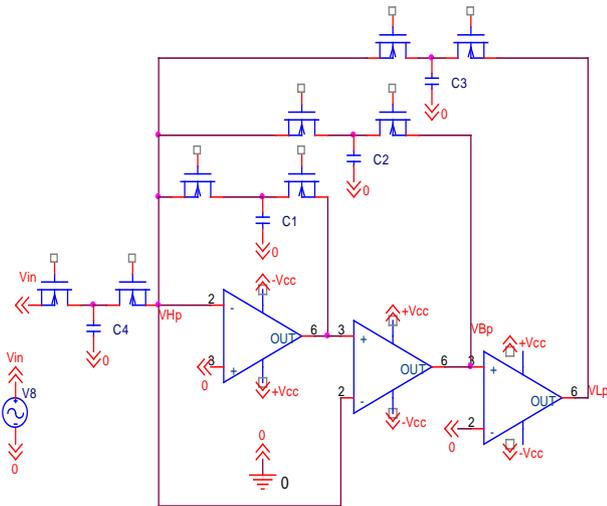


Figure 2. Proposed Circuit diagram for Electronically Tunable Third Order Switched-Capacitor filter

### IV. CIRCUIT ANALYSIS AND DESIGN EQUATIONS

Op-amp ( $\mu A$  741) is an internally compensated op-amp, which represented by "Single pole model",

$$A(s) = A_0 \omega_0 / (S + \omega_0) \quad (1)$$

Where,

$A_0$  = open loop d.c. gain,  $\omega_0$  = open loop -3dB bandwidth,  $GB = A_0 \omega_0$  = gain bandwidth product of op-amplifier.

$$A(s) = A_0 \omega_0 / S = GB / S, \quad (2)$$

Where,  $S \gg \omega_0$

This shows that the op-amplifier is an "integrator", Thus Electronically Tunable Third-Order Switched-Capacitor Filter transfer function at three different terminals are given below. The voltage transfer function for low-pass filter:

$$T_{Lp} = \frac{-GB_1 GB_2 GB_3 C_4}{X_1 S^3 + X_2 S^2 + X_3 S + X_4} \quad (3)$$

The voltage transfer function for band-pass filter:

$$T_{Bp} = \frac{-SGB_1 GB_2 C_4}{X_1 S^3 + X_2 S^2 + X_3 S + X_4} \quad (4)$$

The voltage transfer function for high-pass filter:

$$T_{Hp} = \frac{S^3 C_4}{X_1 S^3 + X_2 S^2 + X_3 S + X_4} \quad (5)$$

Where

$$X_1 = C_1 + C_2 + C_3 + C_4$$

$$X_2 = GB_1 C_1 + GB_2 C_2$$

$$X_3 = GB_1 GB_2 C_2 + GB_2 GB_3 C_3$$

$$X_4 = GB_1 GB_2 GB_3 C_3$$

The circuit was designed using coefficient matching technique i.e. by comparing these transfer functions with General Third-order transfer functions [10]. The general Third-order transfer function is given by

$$T(S) = \frac{\alpha_3 S^3 + \alpha_2 S^2 + \alpha_1 S + \alpha_0}{S^3 + \omega_0 \left(1 + \frac{1}{Q}\right) S^2 + \omega_0^2 \left(1 + \frac{1}{Q}\right) S + \omega_0^3} \quad (6)$$

By comparing (3), (4), and (5) with (6), we get the design equation as

$$C_1 + C_2 + C_3 + C_4 = 1 \quad (7)$$

$$GB_1 C_1 + GB_2 C_2 = \omega_0 \{1 + 1/Q\} \quad (8)$$

$$GB_1 GB_2 C_2 + GB_2 GB_3 C_3 = \omega_0^2 \{1 + 1/Q\} \quad (9)$$

$$GB_1GB_2GB_3C_3 = W_0^3 \quad (10)$$

So that Values of  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$  can be calculated using these equations for different values of Q and  $f_0 = 15$  KHz (table1).

Table 1 : Capacitance values for different values of Q

Q	$C_1$ ( $\mu$ f)	$C_2$ ( $\mu$ f)	$C_3$ (nf)	$C_4$ ( $\mu$ f)
0.1	286.8	7.9	19.2	705.3
0.4	91.3	2.5	19.2	906.2
0.8	58.7	1.6	19.2	939.7
1	52.2	1.4	19.2	946.4
4	32.6	0.9	19.2	966.5
8	29.3	0.8	19.2	909.8
10	28.7	0.77	19.2	970.5

### V. SENSITIVITY

The sensitivities of  $\omega_0$  and Q in this Electronically Tunable third-order Switched-capacitor Filter are as follows.

$$S_{C_1}^{W_0} = -\frac{1}{3} C_1$$

$$S_{C_2}^{W_0} = -\frac{1}{3} C_2$$

$$S_{C_3}^{W_0} = -\frac{1}{3} \{C_3 - 1\}$$

$$S_{C_4}^{W_0} = -\frac{1}{3} C_4$$

$$S_{GB_1}^{W_0} = S_{GB_2}^{W_0} = S_{GB_3}^{W_0} = \frac{1}{3}$$

$$S_{C_1}^Q = -\frac{1}{3} (1 + Q) C_1$$

$$S_{C_2}^Q = -(1 + Q) C_2 \left\{ \frac{1}{(C_2 + C_3)} - \frac{1}{3} \right\}$$

$$S_{C_3}^Q = -(1 + Q) \left\{ \frac{1}{(C_2 + C_3)} - \frac{1}{3} - \frac{2}{3C_3} \right\}$$

$$S_{C_4}^Q = -\frac{1}{3} (1 + Q) C_4$$

$$S_{GB_1}^Q = -(1 + Q) \left\{ \frac{C_2}{C_2 + C_3} - \frac{2}{3} \right\}$$

$$S_{GB_2}^Q = -\frac{1}{3} (1 + Q)$$

$$S_{GB_3}^Q = -(1 + Q) \left\{ \frac{C_3}{C_2 + C_3} - \frac{2}{3} \right\}$$

### VI. EXPERIMENTAL SET UP

The circuit consists of three op-amps ( $\mu$ A 741) with wide identical gain bandwidth product (GB) and four Capacitors with MOSFET, which form Switched-Capacitor. The circuit performance is studied for

different Values of circuit merit factor Q with center frequency  $f_0 = 15$  KHz. The general operating range of this filter is 10 Hz to 1.2 MHz. The value of GB ( $GB_1 = GB_2 = GB_3$ ) is  $(2\pi \times (5.6) \times 10^5 \text{ rad/sec})$ . The table1 shows the capacitor values for different circuit merit factor Q. MOSFETs are driven by two non-overlapping clocks. The input voltage of 0.5mV is applied. The table1 shows the capacitor values for different circuit merit factor Q.

### VII. RESULT AND DISCUSSION

Following observations are noticed for Low-pass, Band-pass and High-pass at corresponding terminals.

#### a) Low-Pass Response

The figure 3 shows the low pass response for different values of circuit merit factor Q.

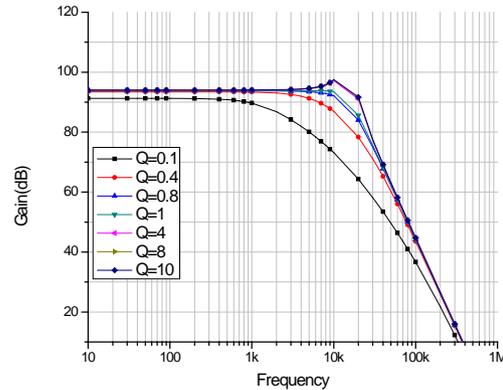


Figure 3 : Low-pass (LP) responses for different values of Q

Table 2 : Analysis of Low Pass Response for Graph (Fig. 3)

Q	Max. Passband Gain (dB)	$f_{\omega}$ (kHz)	$f_0 \sim f_{\omega}$ (kHz)	Gain Roll-off in stop band	
				dB/Octave (kHz)	Octave starting at (kHz)
0.1	91.3	20	5	17	215
0.4	93.4	38	23	17.7	90
0.8	93.6	43	28	18	60
1	93.8	43	28	18	60
4	94	44	29	18	60
8	94	44	29	18	60
10	94	44	29	18	60

The maximum pass-band gain varies between 91.3dB to 94dB and the gain roll-off per octave varies between 17 to 18dB/octave. But in previous reported configuration maximum pass-band gain varies between 82dB to 87dB. Also, the gain roll-off per octave in stop-band varies between 14 to 19dB/octave [14]. The maximum pass-band gain increase with increase in

values of circuit merit factor Q but after  $Q \geq 4$  this value gets stabilized at the maximum pass-band gain. The Gain roll-off values are close to ideal value of 18dB/octave for third order switched-capacitor filter. The response shows no overshoot for all the values of circuit merit factor Q where as the previous reported configuration shows overshoot with increase in Q (for  $Q=10$ , the overshoot is 14 dB) [14].

b) High-pass response

The figure 4 shows the High pass response for different values of circuit merit factor Q.

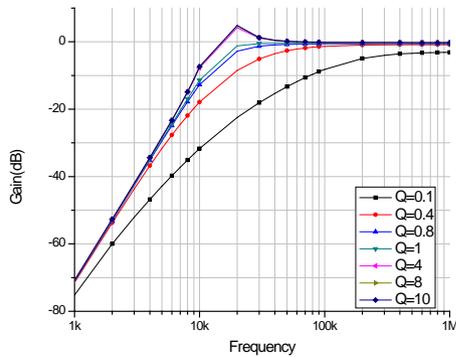


Figure 4 : High-pass (HP) responses for different values of Q

Table 3 : Analysis of High Pass Response for Graph (Fig. 4)

Q	$f_{0H}$ (kHz)	$f_0 \sim f_{0H}$ (kHz)	Gain Roll-off in stop band		Gain Stabilization		Peak Gain of overshoot (dB)
			dB/Octave	Octave Starting at (kHz)	(dB)	$f_s$ (kHz)	
0.1	158	143	17.4	2	-3	460	0
0.4	37	22	18	3.5	0	170	0
0.8	19	4	18	5	0	46	0
1	13	2	18	5	0	46	0
4	13	2	18	5	0	40	3
8	13	2	18	5	0	40	5
10	13	2	18	5	0	40	5

Table 5 : Analysis of Band Pass Response for Graph (Fig. 5)

Q	Max. Passband gain (dB)	$f_1$ (kHz)	$f_2$ (kHz)	BW (kHz)	Gain Roll-off / octave in stop band			
					Leading Part		Trailing Part	
					dB/ octave	Octave starting at (kHz)	dB/ octave	Octave starting at (kHz)
0.1	39	0.4	55	54.6	5.8	0.6	12	206
0.4	52	0.8	60	59.2	6	3	12	61
0.8	57	1.2	52	51.8	6	3	12	40
1	58	1.3	51	50.7	6	3	12	41

The Gain roll-off in stop-band varies between 17.4dB to 18dB/octave which is close to the ideal value of 18 dB /octave for third order Switched-Capacitor filter. Also, the gain is stabilized for all values of circuit merit factor  $Q \geq 0.4$ . But in previous reported Configuration, the Gain roll-off in stop-band varies between 11 to 12dB/octave. Also, the gain can't be stabilized at 0dB for all values of circuit merit factor Q [14]. The peak gain for overshoot is minimizing from 44dB to 5dB due to the feedforward input signal that's given to the second Op-amp in the proposed circuit configuration. The gain gets stabilized almost at 0 dB for all values of  $Q \geq 0.4$ . The response shows overshoot for all the values of  $Q \geq 4$ . The analysis for the responses are summarizes in the table 3.

Table 4 : Comparison of Overshoot

Q	Overshoot observed in dB	
	Previous Reported circuit	Proposed circuit
0.1	0	0
1	0	0
5	38	3
10	44	5

c) Band-pass response

The figure 5 shows the Band-pass response for different values of circuit merit factor Q.

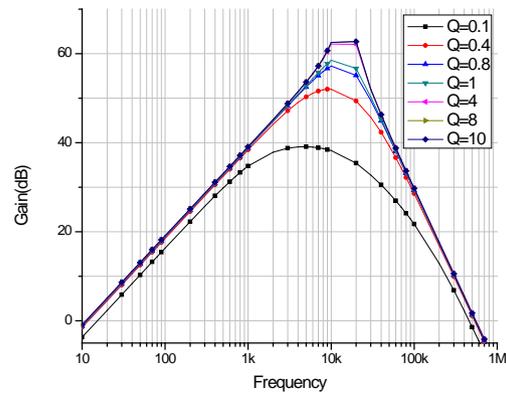


Figure 5 : Band-pass (BP) response for different values of Q

4	62	1.7	44	43.2	6	3	12	41
8	62.5	1.8	44	43.2	6	3	12	41
10	62.5	1.8	44	43.2	6	3	12	41

The maximum pass-band gain varies between 39dB to 62.5dB. Also, the bandwidth varies between 43.2 KHz to 59.2 KHz and Gain roll-off in trailing part varies between 11.6 to 12dB/octave. But in previous reported configuration the maximum pass-band gain varies between 33dB to 73dB. Also, the bandwidth varies between 59.4 KHz to 22 KHz and Gain roll-off in trailing part varies between 8dB/octave to 13dB/octave [14]. The maximum pass-band gain increases with increase in circuit merit factor Q. The bandwidth decreases with increasing in values of circuit merit factor Q but after  $Q \geq 4$  this value gets stabilized at 43.2 KHz. For lower values of circuit merit factor Q, this filter can be used for wide bandwidth and for higher values of circuit merit factor Q it can be used for narrow bandwidth. There is no shift in the central frequency. It is also observed that the pass band distribution of frequency is symmetric for both sides. The gain roll-off/octave in leading and trailing part of the response is same. The circuit works better band pass response for  $Q \geq 0.4$ .

### VIII. CONCLUSIONS

A realization of Electronically Tunable Third-Order Switched-Capacitor Filter with Feedforward Signal to minimize Overshoot has been proposed. The filter circuit can be used for both narrow as well as for wide bandwidth, so this circuit works for electronically tunable bandwidth. The gain roll-off for this circuit is close to the ideal value. The gain gets stabilized almost at 0 dB for all values of  $Q \geq 0.4$ . The Low pass filter function works practically only for higher merit factor Q. The circuit shows better response for  $Q \geq 0.4$  and  $f_0 = 15$  kHz. In the proposed circuit configuration, the peak gain for overshoot is minimizing from 44dB to 5dB due to the feedforward input signal.

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## Adaptive Filters

By Dr. Ziad Sobih & Prof. Martin

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*Abstract-* We know the optimum and suboptimum receiver for ISI in the transmission through band-limited non ideal channels. The optimum employ maximum likelihood detection. The sub optimum employ linear equalizer.

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# Adaptive Filters

Dr. Ziad Sobih<sup>α</sup> & Prof. Martin<sup>σ</sup>

**Abstract-** We know the optimum and suboptimum receiver for ISI in the transmission through band-limited non ideal channels. The optimum employ maximum likelihood detection. The sub optimum employ linear equalizer.

In our design of the equalizer we assume that we know at the receiver the impulse response of the channel or the frequency response. In most communication channels this response is varying as a function of time. In this case we use an equalizer to adapt for this change.

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## I. ADAPTIVE LINEAR EQUALIZER

In the case of linear equalizer we will consider two methods to adjust the coefficient values  $c_k$ . One method is to minimize the peak distortion at the

$$\begin{aligned} E(\varepsilon_k I_{k-j}^*) &= E[(I_k - I_k) I_{k-j}^*] \\ &= E(I_k I_{k-j}^*) - E(\hat{I}_k I_{k-j}^*), \quad j = -K, \dots, K \end{aligned} \quad (1)$$

We assume that information symbols are uncorrelated. And that it is uncorrelated with the estimate

$$E(\varepsilon_k I_{k-j}^*) = \delta_{j0} - q_j, \quad j = -K, \dots, K \quad (2)$$

$$E(\varepsilon_k I_{k-j}^*) = 0, \quad j = -K, \dots, K \quad (3)$$

This mean that  $q_0=1$  and  $q_n=0$  for  $n$  not equal to zero.

When the channel response is not known the cross correlation in equation 1 can not be found. To circumvent this problem we send a known training sequence  $I_k$  to the receiver. This way we can estimate the cross correlation by using time averages. After we send this training sequence for samples length equal or more than equalizer length we can find the equalizer coefficient that satisfy equation 3.

A simple recursive algorithm

$$\hat{c}_j^{(k+1)} = \hat{c}_j^{(k)} + \Delta \varepsilon_k I_{k-j}^*, \quad j = -K, \dots, -1, 0, 1, \dots, K \quad (4)$$

Where  $\hat{c}_j^{(k)}$  is the  $j$ th coefficient at time  $k$  T,  $\varepsilon_k$  is the error at time  $k$  T, and  $\Delta$  is a scaling factor for rate adjustment. This is the zero forcing algorithm. The term  $\varepsilon_k I_{k-j}^*$  is the cross correlation estimate of  $E(\varepsilon_k I_{k-j}^*)$ .

output. The second method is to minimize the mean square error at the output. Now we will talk about each method.

## II. THE ZERO-FORCING ALGORITHM

The peak distortion  $D(c)$  is minimized by selecting the appropriate  $c_k$ . In general it is not easy computation. Except for the case  $D_0 < 1$ . In this case  $D(c)$  is minimized by forcing  $q_n = 0$  and  $q_0 = 1$ . We will use the zero forcing algorithm to achieve this condition.

The zero forcing algorithm is achieved by equating the cross correlation between the error and the desired sequence to zero. We have

$I_{(j-k)}$ . This is accomplished by recursive first order difference equation which is a simple discrete time integrator. This is due to second fundamental theory of calculus.

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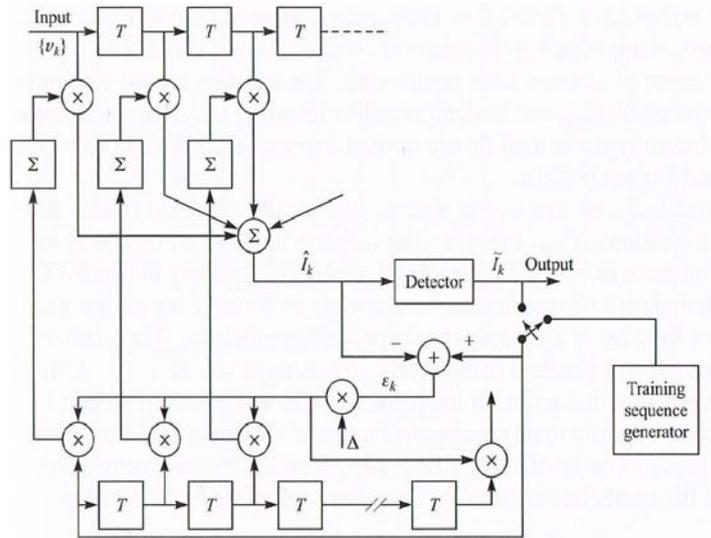


Figure 1

When we use a training sequence we are in the training mode. We do this until the coefficient of the equalizer converge to the optimal. At this point the decision of the output is sufficiently reliable. Now we go to the adaptive mode where we use the estimated output to continue adjusting the coefficients. In this case the cross correlation equation to update c is

$$c_i^{(k+1)} = c_i^{(k)} + \Delta \tilde{\epsilon}_k \tilde{I}_{k-i}^* \tag{5}$$

This is similar to least mean square LMS algorithm. We will talk about MSE in detail next.

### III. THE LMS ALGORITHM

First we calculate the error. We find that to minimize the error C has to satisfy the set of linear equations.

$$\Gamma C = \xi \tag{6}$$

Where T is the covariance metric of the input v k. C is the quantizer coefficients and E is the input times d the desired response.

An iterative algorithm can be used that avoid metric inversion to calculate C opt. the simplest is the method of steepest decent. In which we choose any C to start and it will converge by time to C opt. our start C will correspond to some point on the MSE surface curve. The gradient G is computed at this point. Using this gradient we move to the next estimate closer to the minimum.

$$C_{k+1} = C_k - \Delta G_k, \quad k = 0, 1, 2, \dots \tag{7}$$

The gradient is

$$G_k = \frac{1}{2} \frac{dJ}{dC_k} = \Gamma C_k - \xi = -E(\epsilon_k V_k^*) \tag{8}$$

Where C<sub>k</sub> is the coefficients at the k iteration. E k is the error at k iteration. V is the vector of the input. Delta is a small positive number that will ensure convergence of the iterative process. If the minimum MSE is reached at some k then G<sub>k</sub>=0 so that C<sub>k</sub> stay constant. This method is slow but it is good to explain things.

The basic difficulty of this method is the lack of knowledge of the gradient vector G. G depend on the covariance metric T and the vector E of cross correlation. These depend on the coefficient of the equivalent discrete channel model in which the receiver do not know. To overcome this difficulty an estimate of G is used. The coefficient can be found using this estimate as

$$\hat{C}_{k+1} = \hat{C}_k - \Delta \hat{G}_k \tag{9}$$

Where we have an estimate of the gradient and an estimate of the coefficients

We find that

$$\hat{G}_k = -\epsilon_k V_k^* \tag{10}$$

The equation is

$$\hat{C}_{k+1} = \hat{C}_k + \Delta \epsilon_k V_k^* \tag{11}$$

This is the basic LMS algorithm for recursively adjusting the weight coefficients described by Widrow (1966). It is figure 2

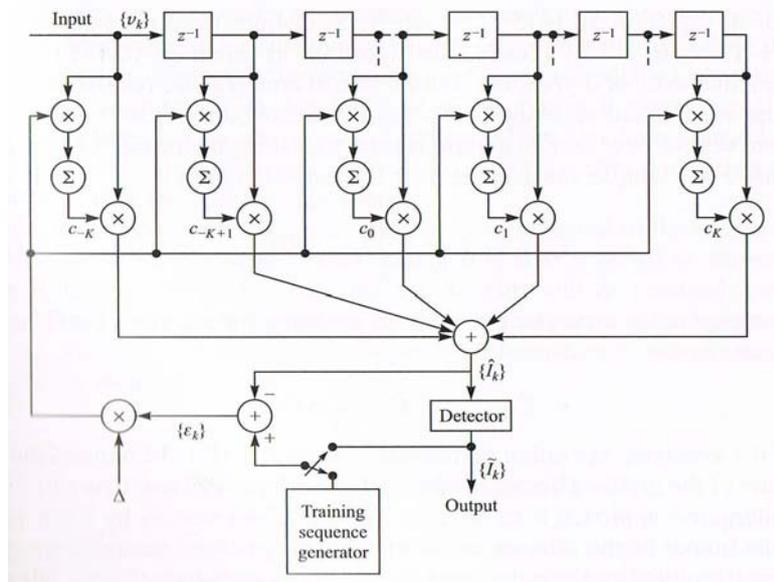


Figure 2

Equation 11 has been used in commercial modems. Three versions are used using only the sign adaptive equalizers that are used in high speed information.

$$\begin{aligned}
 c_{(k+1)j} &= c_{kj} + \Delta \text{csgn}(\varepsilon_k) v_{k-j}^*, & j &= -K, \dots, -1, 0, 1, \dots, K \\
 c_{(k+1)j} &= c_{kj} + \Delta \varepsilon_k \text{csgn}(v_{k-j}^*), & j &= -K, \dots, -1, 0, 1, \dots, K \\
 c_{(k+1)j} &= c_{kj} + \Delta \text{csgn}(\varepsilon_k) \text{csgn}(v_{k-j}^*), & j &= -K, \dots, -1, 0, 1, \dots, K
 \end{aligned}$$

where  $\text{csgn}(x)$  is defined as

(12-13-14-15)

$$\text{csgn}(x) = \begin{cases} 1 + j & [\text{Re}(x) > 0, \text{Im}(x) > 0] \\ 1 - j & [\text{Re}(x) > 0, \text{Im}(x) < 0] \\ -1 + j & [\text{Re}(x) < 0, \text{Im}(x) > 0] \\ -1 - j & [\text{Re}(x) < 0, \text{Im}(x) < 0] \end{cases}$$

Equation 14 is the most easy to implement. It has the slowest convergence relative to the others.

Several other LMS algorithms are obtained by averaging the gradient vector over several iteration points before we adjust c.

$$\tilde{\mathbf{G}}_{mN} = -\frac{1}{N} \sum_{n=0}^{N-1} \varepsilon_{mN+n} \mathbf{V}_{mN+n}^* \quad (16)$$

now the equation is

$$\hat{\mathbf{C}}_{(k+1)N} = \hat{\mathbf{C}}_{kN} - \Delta \tilde{\mathbf{G}}_{kN} \quad (17)$$

this reduce the noise

A good approach is to low pass filter the noisy gradient vector to have a good estimate. A simple way to do that is

$$\tilde{\mathbf{G}}_k = w \tilde{\mathbf{G}}_{k-1} + (1-w) \hat{\mathbf{G}}_k, \quad \tilde{\mathbf{G}}(0) = \hat{\mathbf{G}}(0) \quad (18)$$

Where  $0 < w < 1$  determine the band width of the low pass filter. If  $w$  is close to unity the filter

bandwidth is small. On the other hand if  $w$  is small the filter has a large band width. With this filtered quantity the LMS equation is

$$\hat{\mathbf{C}}_{k+1} = \hat{\mathbf{C}}_k - \Delta \tilde{\mathbf{G}}_k \quad (19)$$

In the training mode we have the detected sequence and the transmitted sequence at the receiver to adjust the weight of the coefficients of the equalizer. After training we can start the adaptive mode. The length of the training sequence has to be equal or more to the number of coefficients.

The training sequence is usually used to be periodic. The period is  $N=2k+1$ . In this case the gradient is averaged over the period length as in equation 17. The weights adjustment can be by making a decision on the received data and use this decision to calculate the error. As long as the receiver operate at low error rate the convergence algorithm will be ok. The second algorithm is to compare the received data with the transmitted data assuming it is provided by a probe initially for training.

If the channel response changes, the error will change. This mean that the weights will change according to equation 11. We will also have a change if the information sequence or the noise statistics change. Thus, the equalizer is adaptive.

a) *Convergence Properties of the LMS Algorithm*

The convergence properties given in equation 11 is governed by the step size parameter. We will choice the step size parameter to ensure convergence of the steepest descent algorithm equation 7 using the exact value of the gradient.

We have

$$\begin{aligned} \mathbf{C}_{k+1} &= \mathbf{C}_k - \Delta \mathbf{G}_k \\ &= (\mathbf{I} - \Delta \mathbf{\Gamma}) \mathbf{C}_k + \Delta \xi \end{aligned} \quad (20)$$

This can be modeled by the closed loop control system in figure 3. The autocorrelation matrix in 20 is coupled. In order to solve the equations in 20 we have to decouple this matrix. This is also done to find the convergence property. The appropriate linear transformation to decouple this matrix is

$$\mathbf{\Gamma} = \mathbf{U} \mathbf{\Lambda} \mathbf{U}^H \quad (21)$$

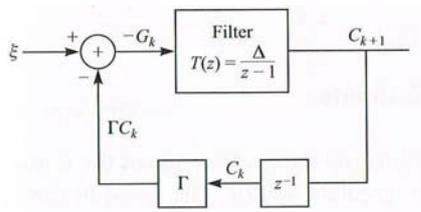


Figure 3

This form has a matrix with diagonal equal to the Eigen values of the system.

We put 21 into 20 and we have

$$\mathbf{C}_{k+1}^o = (\mathbf{I} - \Delta \mathbf{\Lambda}) \mathbf{C}_k^o + \Delta \xi^o \quad (22)$$

Now the system is decupled and the solution is

$$\mathbf{C}_{k+1}^o = (\mathbf{I} - \Delta \mathbf{\Lambda}) \mathbf{C}_k^o \quad (23)$$

This mean that the system will converge if

$$|1 - \Delta \lambda_k| < 1, \quad k = -K, \dots, -1, 0, 1, \dots, K \quad (24)$$

The inequalty that insure convergence is

$$0 < \Delta < \frac{2}{\lambda_{\max}} \quad (25)$$

We have an upper bound on the max Eigen value

$$\begin{aligned} \lambda_{\max} &< \sum_{k=-K}^K \lambda_k = \text{tr } \mathbf{\Gamma} = (2K + 1) \Gamma_{kk} \\ &= (2K + 1)(x_0 + N_0) \end{aligned} \quad (26)$$

The convergence is fast if (1-delta\*Lambda) is small. This mean that the pole is far from the unit circle. As we can see from the equations lambda\_max/lambda\_min determine the convergence rate.

IV. EXCESS MSE DUE TO NOISY GRADIENT ESTIMATES

The receiver when adjusting the coefficients use a noisy estimate of the gradient vector. the noise result in random fluctuation from the optimal value. So we have j = j\_min + j\_delta were j\_delta is the variance of noise.

The total MSE at the output is

$$J = J_{\min} + (\mathbf{C} - \mathbf{C}_{\text{opt}})^H \mathbf{\Gamma} (\mathbf{C} - \mathbf{C}_{\text{opt}}) \quad (27)$$

Were C\_opt is the optimum value of C. simplifying we get

$$J = J_{\min} + \sum_{k=-K}^K \lambda_k E |c_k^o - c_{k \text{opt}}^o|^2 \quad (28)$$

We find j\_delta as

$$J_{\Delta} = \sum_{k=-K}^K \lambda_k E |c_k^o - c_{k \text{opt}}^o|^2 \quad (29)$$

It has been shown that

$$J_{\Delta} = \Delta^2 J_{\min} \sum_{k=-K}^K \frac{\lambda_k^2}{1 - (1 - \Delta \lambda_k)^2} \quad (30)$$

Simplifying

$$\begin{aligned} J_{\Delta} &\approx \frac{1}{2} \Delta J_{\min} \sum_{k=-K}^K \lambda_k \\ &\approx \frac{1}{2} \Delta J_{\min} \text{tr } \mathbf{\Gamma} \\ &\approx \frac{1}{2} \Delta (2K + 1) J_{\min} (x_0 + N_0) \end{aligned} \quad (31)$$

Were x0+N0 is the received signal plus noise

Delta should be

$$\Delta < \frac{2}{(2K + 1)(x_0 + N_0)} \quad (32)$$

For example

$$\Delta = \frac{0.2}{(2K + 1)(x_0 + N_0)} \quad (33)$$

The degradation in the output SNR of the equalizer due to excess MSE is less than 1 dB.

The analysis of the excess error is for assuming that C have converged to optimum.

The convergence has been studied by many researchers.

This is an example were we have 11 coefficients. We start with all of them are zero. We see that all of them will converge to the right value of the channel. We use MS algorithm. The Matlab code is given. As we can see the error converge to zero as the number of iteration increase. We also add noise to the input to the equalizer.

```
echo on
N=500;
K=5;
isi=[.05 -.063 .088 -.126 -.25 .9047 .25 0 .126 .038
.088];
sigma=.01;
delta=.09;
num_of_realizations=1000;
mse_av=zeros(1,N-2*K);
```

```
for j=1:num_of_realizations,
for i=1:N,
if (rand<.5),
info(i)=-1;
else
info(i)=1;
end;
echo off;
end;
if (j==1);echo on ; end

end
noise =awgn(info,10);

d_c=[0 0 0 0 0 0 0 0 0 0 0];

for k=1:(N-10),
y_kk=[noise(k:k+10)];
out=y_kk*isi;
z_k=d_c*y_kk.';
e_k= out-z_k
d_c = d_c + e_k * .115 * [ noise(k:k+10) ]
mse(k) =e_k ^2;
echo off;
end;
if (j==1);echo on ;end
mse_av=mse_av+mse;
echo off
echo on
mse_av=mse_av/num_of_realizations
```

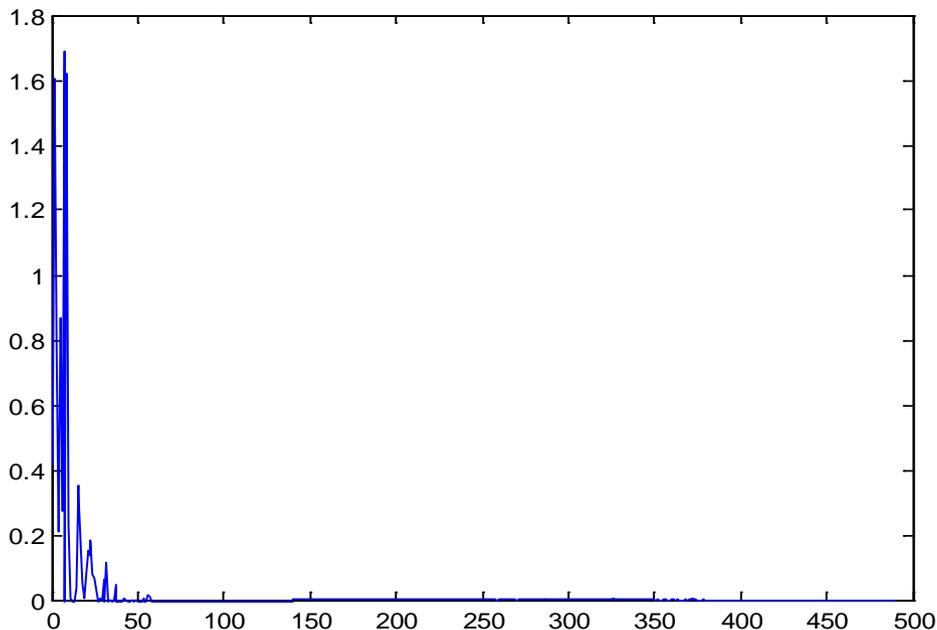


Figure 4

The choice of delta is very critical in the LMS algorithm. To be practical we design the most significant bits for an estimate of the coefficient and the least significant bits for delta so that the LMS algorithm find its way exactly to C opt.

It is important to mention that the LMS algorithm is able to track slowly time varying system. In other words  $j_{\min}$  is a function of time and the MSE surface is moving with time index  $n$ . The LMS method try to track  $j_{\min}$  but always behind it. This mean that we have another error which is the lag error. The total error is

$$J_{\text{total}} = J_{\min}(n) + J_{\Delta} + J_l \quad (34)$$

Where  $j_l$  is the lag error.

Now we try to plot  $j_{\Delta}$  and  $j_l$  as a function of delta. They will behave as in the figure below.  $J_{\Delta}$  decrease and  $j_l$  increase as a function of delta. The total will have a minimum which is the optimum choice for delta.

If the time varying system is fast the  $j_l$  will dominate the error. In this case the LMS will not be appropriate and we must use recursive least squares algorithms.

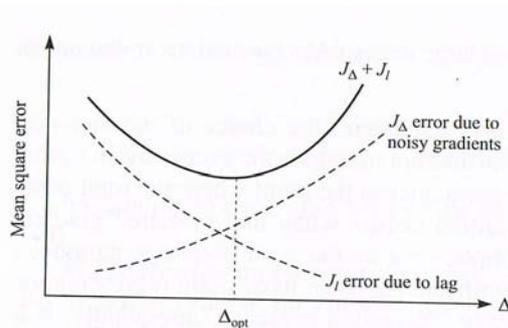


Figure 5

## V. ACCELERATING THE INITIAL CONVERGENCE RATE IN THE LMS ALGORITHM

As we see the convergence rate is controlled by delta. It is also strongly related to the spectral characteristics of the channel. By that I mean the ratio of lambda max to lambda min. if this ratio is close to one the convergence will be fast. If not the convergence will be slow. In this case we say that the channel has poor spectral characteristics.

Researchers investigated this topic from all angels. One simple way is to start with large delta and reduce it to the optimum as time pass by.

To accelerate initial convergence methods have been studied in 1971 and 1977. One method is to replace delta by the weighting matrix  $W$ . the form is

$$\begin{aligned} \hat{C}_{k+1} &= \hat{C}_k - W \hat{G}_k \\ &= \hat{C}_k + W(\mathbf{r} \hat{C} - \xi) \\ &= \hat{C}_k + W e_k \mathbf{V}_k^* \end{aligned} \quad (35)$$

Where  $W$  ideally is the inverse of the autocorrelation matrix of the input data. The autocorrelation can be estimated and the inverse can be found.

If the training sequence is periodic,  $W$  can be seen as a single row and the block diagram of the system will be as in figure 6.

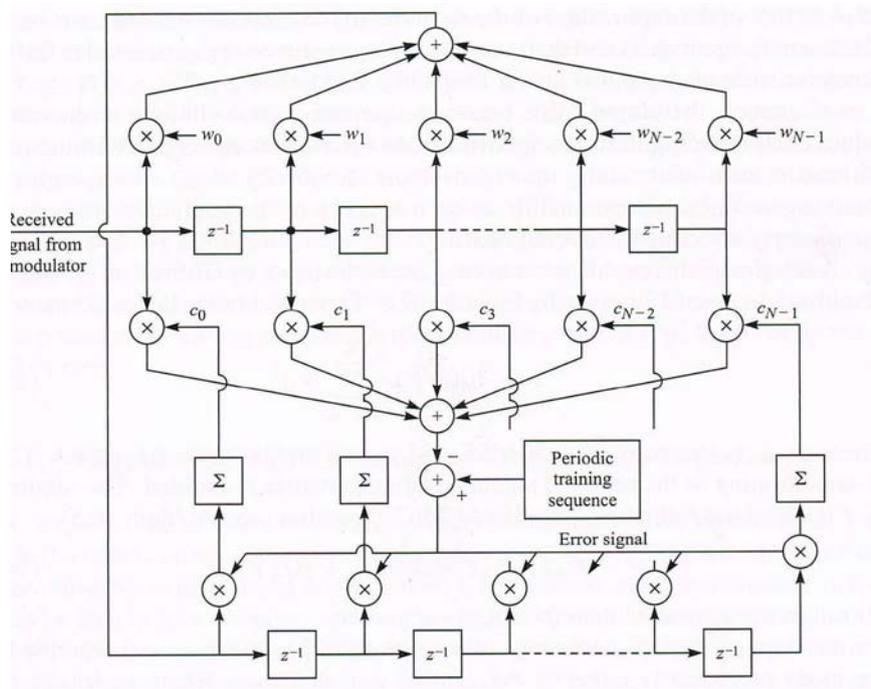


Figure 6

We can estimate the weights from the received signal. The basic steps are:

First we collect one period of N samples in the equalizer delay line. Then we compute N-point DFT (Rn). Then we compute the power spectrum (Rn ^2) and we add to it N times the estimate of the noise variance. Then we compute the inverse DFT. This yields wn in figure 6. To adjust the taps we have

$$c_j^{(k+1)} = c_j^{(k)} - e_j \sum_{m=0}^{N-1} w_k v_{k-j-m}^* \quad j = 0, 1, \dots, N - 1 \quad (36)$$

## VI. CONCLUSION

As in the case of linear adaptive equalizer the coefficient of decision feedback equalizer can be adjusted recursively. This is based on minimization of MSE.

(37)

We should note that this will converge and for the expected value we can use (epsilon V).

(38)

This is the LMS algorithm. First we use a training sequence then we switch to dissection mode.

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# Digital Frequency Synthesis using Multi-Phase NCO for Dielectric Characterization of Materials on Xilinx Zynq FPGA

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**Abstract-** Precise measurement of dielectric characteristics of materials is becoming necessity in several engineering applications. The dielectric constant measurement over wide frequency range for emerging applications such as PCB manufacturing, agriculture, environmental and food processing industries has several challenges. With the advancement in digital VLSI and Field Programmable Gate Array (FPGA) based processing the digital techniques for estimating the dielectric constant are feasible. In this context the digital based frequency generation techniques over wide frequency are discussed in this paper. The multi phase Numerically Controlled Oscillator (NCO) based technique for generating high frequency signals are experimented in this paper. The efficient implementation of NCO for Xilinx Zynq family FPGA, XC7Z020 device is simulated here. The realized multi phase NCO is observed to be occupying only 15% of resources and operating at 250MHz to result efficient synthesis of sine wave with sampling frequency of 1GHz. The design issues related to digital carrier generation on FPGAs, while driving high frequency Digital to Analog Converters (DACs) are discussed and simulation results are presented here.

**Keywords:** *dielectric measurement, digital phase, FPGA, multi phase NCO, Zynq SOC FPGA.*

**GJRE-F Classification :** *FOR Code: 290901p, 090609*



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## I. INTRODUCTION

The dielectric properties measurement is necessary because it can provide the electrical or magnetic characteristics of the materials, which proved useful in many research and development fields [1][10]. The present work is aimed to evolve digital multi phase technique for generating high frequency sinusoid signal using FPGAs, which becomes useful in precise dielectric characterization of materials.

The work presented in this paper is part of ongoing research [1] [9] aimed for precise characterization of printed circuit board (PCB) at high frequencies (order of Hundreds of MHz). This paper discusses the multi phase NCO based technique for

generating high frequency sine wave, which is required in this context.

Measurement of dielectric properties requires measurements of the complex relative permittivity ( $\epsilon_r$ ) and complex relative permeability ( $\mu_r$ ) of the materials [1]. The complex dielectric permittivity consists of real and imaginary parts. The real part of the complex permittivity is referred as dielectric constant and it is a measure of the amount of energy from an external electrical field stored in the material. The imaginary part is indicative of the amount of energy that gets dissipated in material when it is subjected to electric field [1]. The imaginary part is zero for lossless materials. The term loss tangent is defined as given in (1) which indicates the dissipative nature of material with respect to the energy storage nature [11].

$$\tan \alpha = \frac{\epsilon_r''}{\epsilon_r'} = \frac{1}{Q} \quad (1)$$

The vector diagram for loss tangent is shown in Fig.1. Loss tangent is also referred as quality factor (Q). The circuit equivalent of real and imaginary parts of permittivity can be well derived from capacitor action [1].

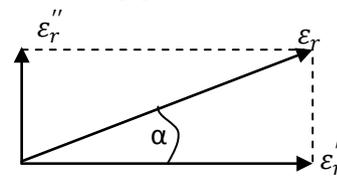


Fig 1 : Capacitor action with dielectric

The equation (2) gives capacitance value of parallel plate capacitor as function of area of the plate, distance between plates and permittivity of the medium.

$$C = \frac{\epsilon A}{d} \quad (2)$$

Where  $\epsilon$  is the total permittivity, which can be represented as  $\epsilon = \epsilon_0 \epsilon_r$

The  $C_0$  can be used to represent the capacitance when only vacuum is present between the capacitor parallel plates. The equation (2) can be rewritten as given in equation (3) in terms of  $C_0$ .

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$$C = \epsilon_r C_0 \tag{3}$$

The Fig. 2. shows simple RC circuit for measuring the dielectric constant.

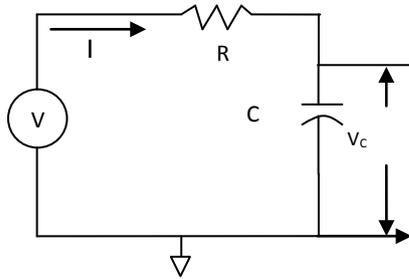


Fig. 2 : Schematic of RC circuit

The voltage across capacitor can be given as equation (4) whose phase term can be computed as in equation (5).

$$V_C = \frac{V}{1+j\omega C_0 \epsilon_r R} \tag{4}$$

$$\theta = - \tan^{-1} \left( \frac{1}{\omega C_0 \epsilon_r R} \right) \tag{5}$$

The phase shift between  $V$  and  $V_C$  is a function of dielectric constant for all remaining being constant values. The dielectric constant measurement through digital techniques is possible, if the signal with angular frequency  $\omega$  can be generated digitally and the phase shift between  $V$  and  $V_C$  is measured accurately [2]. The FPGA based techniques for sinusoid generation using NCO is an established area and being widely used in communication applications. However the maximum synthesizable signal with NCO is limited to  $F_{clk}/2$ , where  $F_{clk}$  is the clock at which the NCO runs.

To enable dielectric Constant measurement up to high frequencies it is required that the FPGA based circuit should be able to generate the signal up to the desired frequency. Above in equation (4)  $\omega = 2\pi f$  and  $f$ =frequency at which dielectric constants are measured. In conventional implementation of NCO the realizable

frequency by NCO is given in equation (6). Fig.3. describes the basic NCO architecture.

$$\text{Output sine wave frequency} = \frac{\Delta p \cdot F_{clk}}{2^N} \tag{6}$$

Where  $F_{clk}$  = clock frequency at which NCO is running

$N$  = size of bit width phase registered

$\Delta p$  = input phase increment word

Since  $F_{clk}$  and  $N$  are fixed for a particular implementation, the input phase increment word ( $\Delta p$ ) describes the frequency of the output sine wave. The first register in the Fig.3. latches the frequency controlled word on the clock edge and the accumulator realized by added and register continuously accumulates input frequency word and generates the phase. This phase accumulator generates the digital phase, which is input to sine lookup table. The sine lookup table generates the digital amplitude samples of sine waves [3]. The digital samples of sine wave need to be supplied to DAC chip which generates corresponding analog sine wave. The analog sine wave after passing through low pass filter will be suitable for dielectric constant measurement. The low pass filter removes the spurious harmonic signals which are present in DAC output.

The present day available RF DAC [6][13] enables high frequency sine wave up to 1 GHz provided the digital part is capable of generating suitable samples. With the present day available FPGA technology the max achievable frequency  $F_{clock}$  is up to 300 MHz only which means the maximum  $F_o$  that can be generated is 150MHz only, Whereas the necessity of dielectric constant measurement of PCB materials is up to few Mega Hertz to Giga Hertz frequencies.

This becomes limitation of digital based carrier generation for high frequency dielectric constant characterization of materials. The present paper implementation of multi phase NCO based architecture enables digital generation of sine wave samples [3], which can be used while interfacing with RF DACs[6][13] by which the concept of digital dielectric constant can be extended up to Hundreds of Mega Hertz to Giga Hertz frequency level.

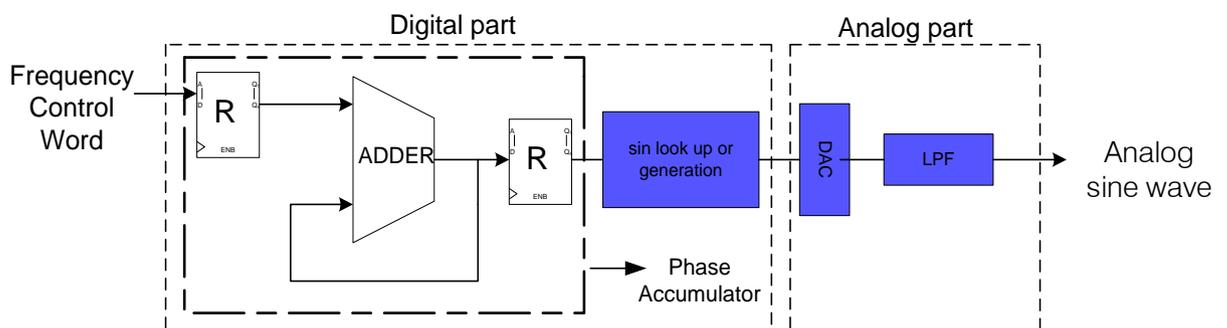


Fig. 3 : High level block diagram of NCO based SIN wave generation

The remaining part of the paper is organized into three sections. Section 2 explains the high level architecture of multiphase digital NCO. Section 3 explains the simulation and synthesis results including the resource utilization summary for ZED board. The last section provides conclusion and future scope of the work.

## II. HIGH LEVEL ARCHITECTURE

This section presents high level architecture of proposed multiphase NCO based sine wave generation [4]. Multiphase NCO technique in principal uses the inverse concept of distributed arithmetic. The distributed arithmetic (DA) principle is an area optimization technique usually implemented in FPGAs and Application Specific Integrated Circuits (ASICs), where certain hardware is made to run at high frequency than the actual throughput required. Utilizing same resource for multiple operations in different clock cycles allows achieving area optimization. For e.g. in a digital logic the requirement is to multiply numbers at 10MHz rate. The FPGA logic employing DA technique runs at 100MHz. The multiplier input is multiplexed and output is demultiplexed to perform 10 multiplications by using single unit.

In multiphase NCO the concept is reverse implementation of resource sharing. In the present Implementation on the ZED board [12] it is aimed to generate sine wave 400 MHz by achieving sampling frequency of 1GHz.

In this implementation 4 NCO modules are made to run as parallel blocks which shall maintain phase offsets corresponding to their sample position. The sine wave generation [4] is illustrated in fig. 4. Scheme of multiphase NCO for high frequency digital The effective sampling rate achieved is denoted as  $F_s$  and is given at (7).

$$F_s = 4 \times F_{clk} \quad (7)$$

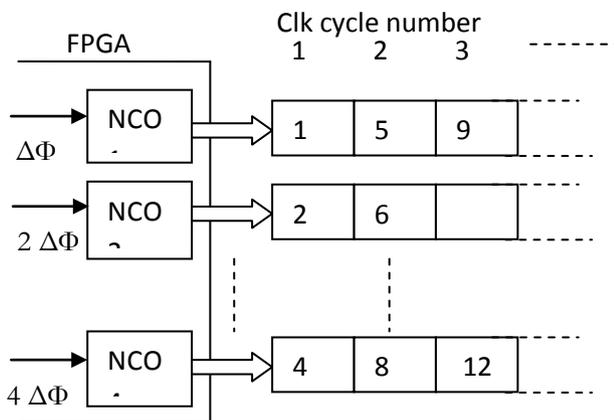


Fig. 5: Set of 4 NCOs generating samples at  $F_s$

The effective sampling rate achieved is denoted as  $F_s$  and is given at (7). The NCOs are fed with phase shifts such that the samples generated by all NCOs form successive samples in sine wave at higher sampling rate  $F_s$ . The figure 5 has the illustration of the same.

The initial phase shifts can be computed by a series of adders, where at each stage  $\Delta\Phi$  is added [6].

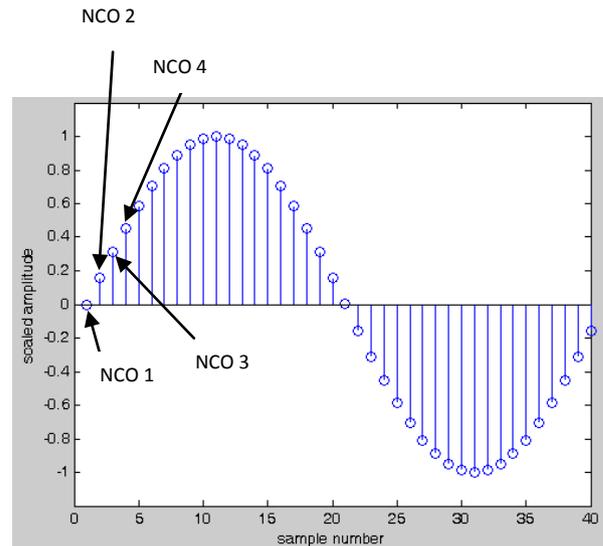


Fig. 5: Samples generated by each NCO in the sin wave at  $F_s$

As the uniformly sampled phase results in spurious values at the multiples of sampling frequency, the phase dithering is implemented. In the phase dithering a pseudo noise binary signal (PN) is used to produce a random number. This random numbers are added to phase accumulator output, before applying to the address inputs of SIN and COS look up tables.

## III. SIMULATION AND SYNTHESIS RESULTS

The simulation results for the implemented logic are given in this section. The figure (6), shows the phase outputs of each NCO. The phase shifts in each channel can be observed due to the different initial values assignment [3].

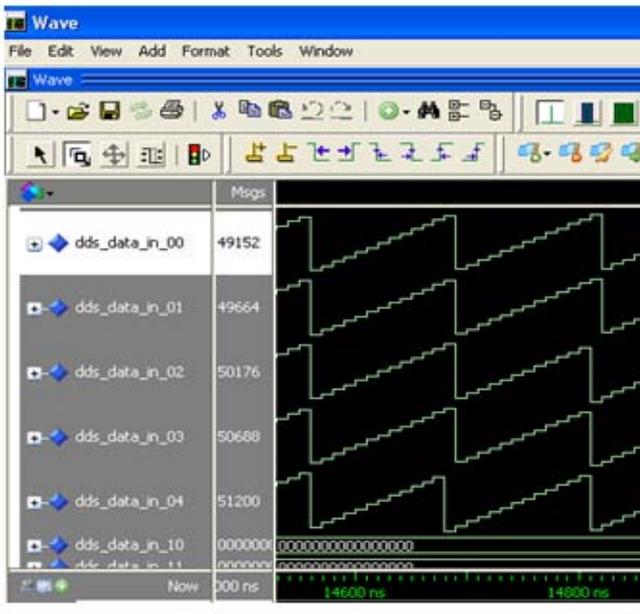


Fig. 6 : Simulation results showing phases of 4 NCOs

The simulation results showing the generated sine waves on all four channels are shown in figure 7. The resultant signal when applied to multi channel DAC is simulated by a mod 4 counter based interleaving logic, placing samples from each channel as illustrated in fig. 5. The last waveform in Fig. 7, RF\_DAC\_SIG shows the generated sine wave with  $F_s$  sampling rate.

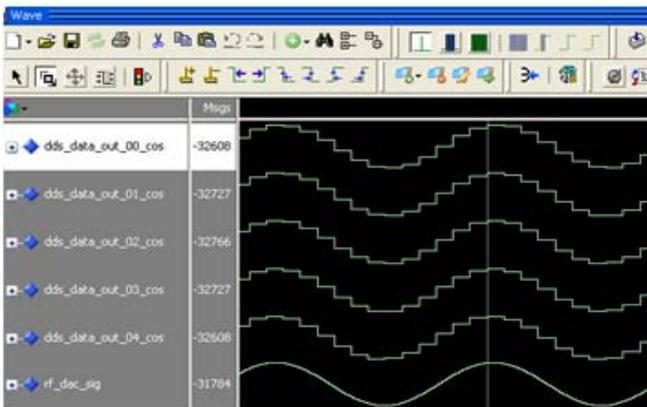


Fig. 7 : Simulation results showing sin wave samples of 4 NCOs and muxed resulting sin wave

The logic is synthesized using Xilinx's ISE 14.6 tool and the area and speed analysis are carried out. The area utilization summary and maximum clock estimate of the implemented digital logic [7] For ZED board (XC7Z020) FPGA [5], are given at fig. 8.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	333	18224	1%
Number of Slice LUTs	459	9112	5%
Number of fully used LUT-FF pairs	270	522	51%
Number of bonded IOBs	35	186	18%
Number of BUFPG/BUFPGCTRLs	2	16	12%

Fig. 8 : Area utilization summary

Timing Summary:

Speed Grade: -3

Minimum period: 2.945ns (Maximum Frequency: 339.587MHz)  
 Minimum input arrival time before clock: 3.021ns  
 Maximum output required time after clock: 3.819ns  
 Maximum combinational path delay: No path found

Fig. 9 : Maximum clock utilization summary

The maximum speed reports 333 MHz, which is higher than the considered 250 MHz operation for the aimed specifications.

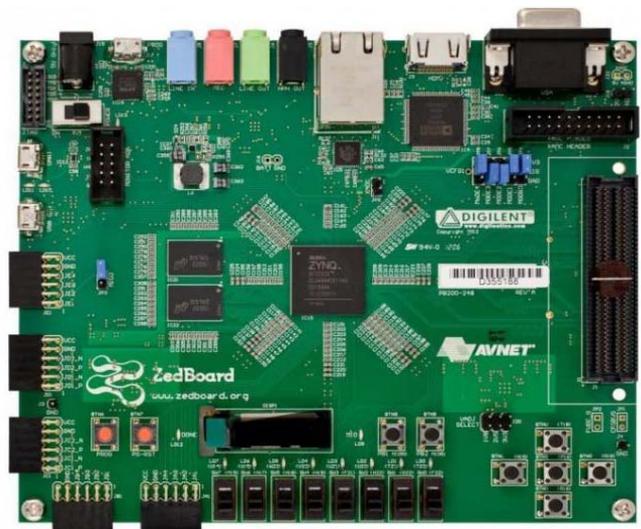


Fig.10 : Zynq Evaluation and development board

It is aimed to continue this work with hard ware integration of Digital to analog converter from Analog devices AD9122 Tx-DAC IC [13]. Hence the data and control signal generation are ensured to meet the specification of this IC and the same are verified with Xilinx Chipscope Integrated Logic Analyzer (ILA) tool.

The figure 11, has chipscope ILA obtained results for 4 channel with the multiphase technique. Since the the AD9122 is complex DAC, similar logic is implemented for generating the quadrature tones with 90 degree phase shifts.

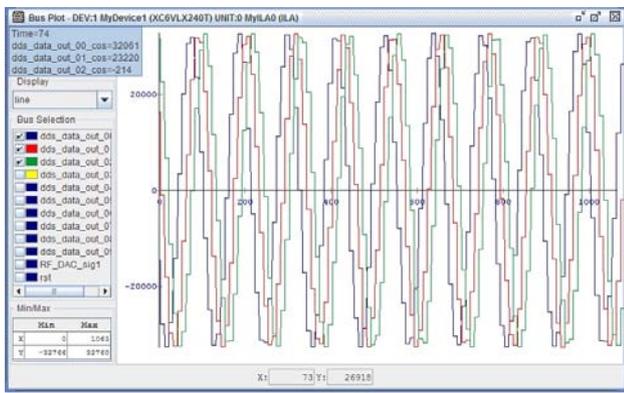


Fig. 11 : On-chip verification results with Chipscope

#### IV. CONCLUSION

The dielectric constant measurement technique with capacitance based measurement is discussed. The basic circuit and dielectric constant measurement using RC circuit principle is discussed. The need of high frequency digital signals synthesis for high frequency sine wave generation is elaborated. FPGA based techniques with multi DDS for driving RF DACs presented considering clock frequency of 250 MHz on FPGA. By employing 4 NCOs, sine wave with 1 Giga samples per second is simulated. Using Xilinx ISE tools synthesis is carried out and area utilization summary is observed. The work is aimed to continue in establishing this technique on With Xilinx Zynq FPGA and RF DAC cards for dielectric constant measurement applications.

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# Reducing the Vulnerability of Digital Protective Relays to Intentional Remote Destructive Impacts: Continuation of the Theme

By Vladimir Gurevich

*Abstract-* A problem of protecting digital protective relays from intentional destructive electromagnetic impacts described in the article. The article is continuation of previous author's publications on this theme.

*Keywords:* digital protective relays, intentional destructive electromagnetic impacts, high power electromagnetic threats, high-altitude electromagnetic pulse, intentional electromagnetic interference.

*GJRE-F Classification : FOR Code: 090699*



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## I. INTRODUCTION

As mentioned in [1], due to the way in which digital protection relays (DPR) of electric power system facilities perform their functions they constitute dangerous entry channels for intentional remote destructive impact (IRDI) into the power systems. IRDI can be qualified as:

- a) Cyber attacks;
- b) High Power Electromagnetic (HPEM) Threats, including High-Altitude Electromagnetic Pulse (HEMP) and Intentional Electromagnetic Interference (IEMI);
- c) Function-technological (use of normal technological functions of protection relays, which were pre-set in such a way that in case of actuation without a cyber attack, for example, by activate the discrete input, the DPR will send corresponding commands to high-voltage circuit breakers, which will interfere with the normal functioning of the electric network or even the whole power system).

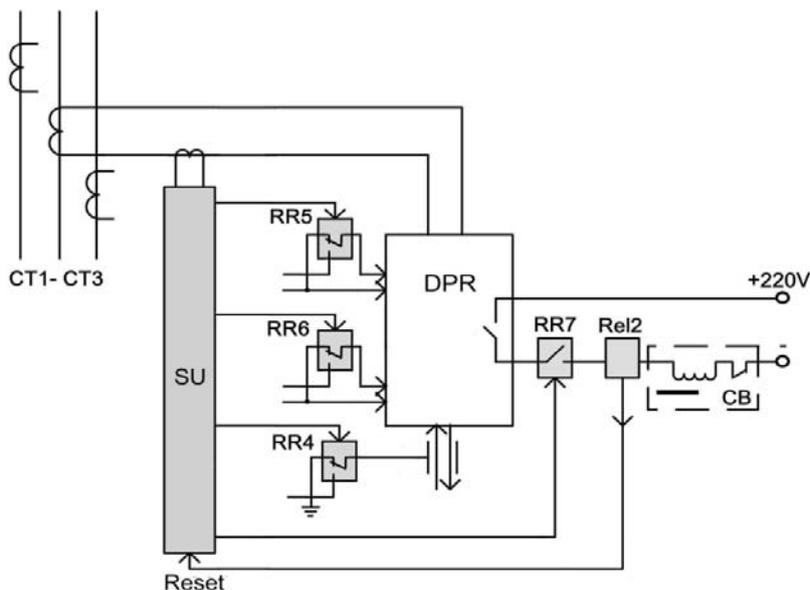
The IRDI can affect the DPR in the following ways:

- Create internal damage of microelectronic components accompanied by simultaneous malfunctioning of relay protection;
- Result in latent destruction of microelectronic components, which cannot be diagnosed under standard workability checks of a DPR, but which can emerge in the course of a DPR's operation as faulty performance of a specific aggregate of logical and computation operations;
- Result in the malfunctioning of DPR by interfering with its algorithm of operation (cyber attacks);

- Result in the malfunctioning of relay protection under full physical and software-based functionality of DPR (function-technological IRDI).

According to [1] there are passive and active methods of protection of DPRs from IRDI. The passive methods of protection include special broadband filters; special metal control cabinets; double and triple shielded and twisted cables; special protective paints, lacquers, films that reflect electromagnetic waves; curtains, carpets and hangings made of metallic fiber, special construction materials, which weaken electromagnetic radiation. The active methods of protection are based on a joint use of DPR and electro-mechanic protection relays (EMPR), which are more resistant to IRDI. At the same time there are two options of connecting DPR and EMPR: parallel connection and series connection [2]. The parallel connection of DPR and EMPR requires a full set of electro-mechanical protection relays designed to perform a total complex of protective functions. Moreover, this connection does not guarantee the absence of faulty and unnecessary actuations of DPR affected by IRDI. As mentioned in [1], faulty, unnecessary and abnormal actuations of DPR (the concepts offered in [3]) can result in larger damage than failures. The series connection of DPR and EMPR does not require using a full set of EMPR; however, a simple starting unit (SU) should be available. Besides, this type of connection prevents faulty and abnormal actuations of DPR affected by IRDI. This is why this type of connection is preferable. The specific example of this type of protection based on a specially designed unit with responsive electro-mechanic elements (reed switches) is described in [4, 5], Fig. 1.

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*Fig. 1 :* Electrical diagram of the active type unit presented in [4, 5] to protect the DPR from IRDI (SU - starting unit on the basis of a reed switch)

This device is designed to protect the DPR from function-technological IRDI – the most complicated IRDI, which cannot be controlled by any other means of protection. Obviously, the device described in [4, 5] is just an example of the concept, the purpose of which is to confirm the possibility of implementing the idea in practice, though it still needs further development, and improvement. Nevertheless, the example substantiates that the problem of DPR protection from function-technological IRDI can be successfully solved. It should be noted that the described device blocks the discrete inputs, communication and outputs of DPR in between the emergency modes, to which DPR should respond; efficiently protects it not only from function-technological IRDI, but also from internal damages, induced by powerful electro-magnetic impacts and cyber attacks affecting its sensitive inputs.

## II. PROTECTION CURRENT AND VOLTAGE CIRCUITS

In order to protect the DPR from internal damage related to effects of high-voltage impulses, which can get into its analogue inputs from current and voltage circuits and in order to protect the supply circuits the well known methods of improving the stability of electronic equipment to electro-magnetic impacts can be used. It should be noted that modern DPRs are already equipped with a built-in protection from these impacts, which corresponds to the requirements of the standards of electro-magnetic compatibility (EMC). However, IRDI are significantly different from electro-magnetic noises in terms of intensity and frequency range, stipulated by these standards. This is why the protection built into DPR

should be significantly strengthened. This is one of the ways to improve DPR's resistance to IRDI. The other way is the use of additional external means of protection, such as passive means of protection (see above).

The elements that connect the analogue inputs of DPR with the external current and voltage circuits are the input current transformer (CT) and the voltage transformer (VT). And for this reason these elements will be affected by the powerful overloads of IRDI in the first turn. The input CT in DPR is simpler in terms of design. As a rule, this is a multi-loop secondary winding, wound on a ferromagnetic core and a primary winding, which consists of several coils of thick insulated wire, wound above insulated secondary winding, see Fig. 2.



*Fig. 2 :* Example of a module of analogue inputs of DPR with installed CT. You can clearly see the primary winding, which consists of 4 coils of flexible insulated black wire

The methods of improvement of the structure's resistance to impacts of powerful impulse voltage are rather simple and include the following:

- Use of grounded shield (either foil or additional single-layer winding) located between the primary and the secondary windings;
- Encapsulation of the secondary winding by pouring it with epoxy resin, which will be hardened in vacuum, see Fig. 3;
- Increasing insulation level between primary and secondary windings by use of a wire with high-voltage insulation as the primary winding;
- Use of additional screens and semi-conducting covers, which equalize the electric field in the CT's design;
- Use of the insulated coating of CT magnetic core

There are many types of flexible wires in high-voltage insulation made of silicone, polyethylene, PTFE and rated for 10-25 kV voltage that are produced by several companies, such as: Teledyne Reynolds, Multi-contact; Allied Wire & Cable; Wiremax; Dielectric Sciences Inc., Axon' Cable, Daburn Electronics & Cable, Sumitomo Electric, Belden, Experimental design bureau of Cabel Industry, "Redkiy Cabel" LLC amongst others.

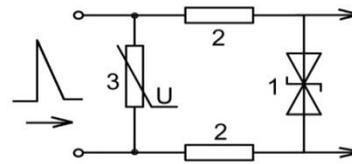
The recommendations for the improvement of resistance of VT are similar except for the fact that instead of a flexible wire with a high-voltage insulation as the primary winding, they use a winding wire with improved insulation of Class III according to IEC 60317-0-1 "Specification for particular types of winding wires – Part 0-1: General requirements – Enamelled round copper wire made of polyimide", where both coils are encapsulated in vacuum.



**Fig. 3 :** Encapsulated current transformers with epoxy encapsulated secondary winding hardened in vacuum. You can clearly see the primary winding, which consists of a single coil of flexible insulated wire

Since the increase of the cross section of the winding wire automatically results in an increase of insulation thickness and its electric strength, it is recommended to use a larger cross section wire regardless of natural increase of VT's size. Some manufacturers are producing winding wires with

insulation made of polyamide, which withstands voltage 1.5 or even double voltage compared with that rated under IEC 60317-0-1. These manufacturers are, for example, P.A.R. Insulations & Wires Ltd of England, Bemka A. S. of Turkey amongst others. In order to ensure additional protection of VT, a special protective chain can be installed inside DPR on its primary winding, see Fig. 4.



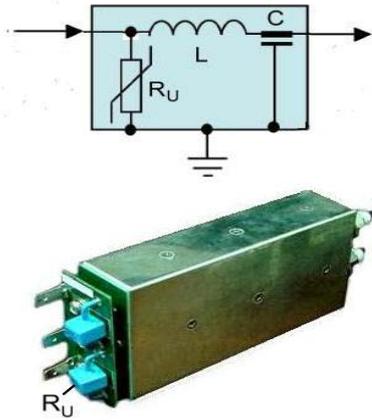
**Fig. 4 :** A diagram of efficient protective chain: 1 – semiconducting suppressor; 2 – current-limiting resistor; 3 – voltage depending resistor (VDR)

This chain, which contains a combination of elements with different specifications, ensures the most efficient protection from electromagnetic IRDI. In addition two low-voltage, opposite connected Zener diodes should be installed on the opposite sides of both internal VT and CT. They will restrict the voltage level of electromagnetic interference, which enters the input of an electronic circuit, if it manages to get to the secondary winding through all layers of insulation and the shield.

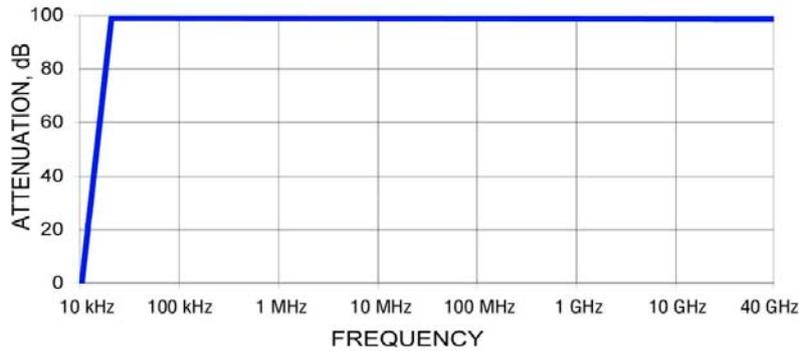
Usually, internal impulse power supplies of DPRs have built-in filters at the input, which include VDR, chocks and capacitors and are efficient in suppression of electromagnetic interferences, including IRDI. It is very important to equip all power supplies of DPR with these high quality filters.

### III. PROTECTION OF AUXILIARY POWER SUPPLY

The measures mentioned above are related to the design of DPR and this is the responsibility of manufacturers. Besides these measures it is necessary to consider the measures of group protection of DPR, which include special relay cabinets [2] and other known measures of passive protection. Among these measures special filters need to be highlighted. They are connected at the entry ports of the voltage and current circuits into the relay room running from the external CT and VT located outside and into the AC supply circuits of the battery chargers. It should be taken into consideration that these are not just simple ordinary filters, which weaken natural electromagnetic interference, but filters that are specially designed to suppress electromagnetic impulse of a HEMP and powerful electromagnetic radiation of IRDI. Technical requirements to these filters are stipulated by military standards and reference books, such as MIL-STD-188-125 and MIL-HDBK-423.

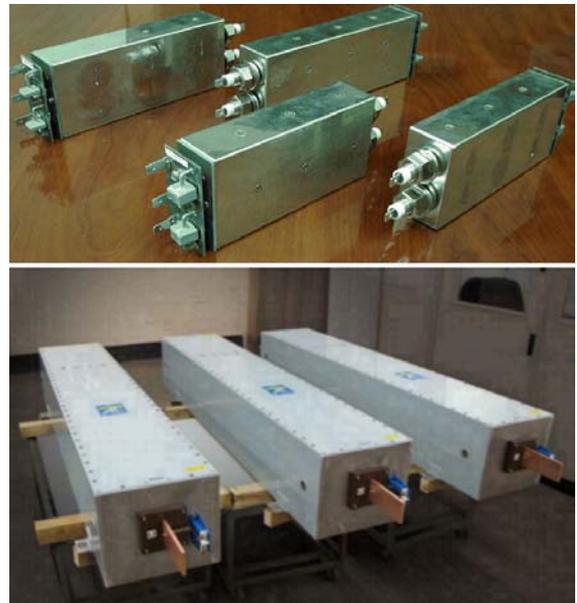


*Fig. 5 :* Layout of the filter and simplified circuit of one section of the filter designed to protect from IRDI. In practice the circuit contains several sections connected in series per each line. There is also a powerful varistor,  $R_U$ , at the input of the device



*Fig. 6 :* Typical frequency specification of filters designed to protect from IRDI

The filters designed for installation in the supply circuits of AC and DC current in single-phase and 3-phase consumers for current ratings from several tens of Amps to several thousands of Amps are available in the market, see Fig. 7.



*Fig. 7 :* Powerful filters for supply circuits: Above - for current rating of several tens of Amps; below - for current rating above 1000 A

There are also less powerful filters for control circuits rated 1-3 A (which can be used to protect the secondary voltage circuits of external VT), see Fig. 8, as well as for communication and data transfer systems, see Fig. 9.



Fig. 8 : Filter for control circuit rated up to 1 A



Fig. 9 : Filter for communication and data transfer systems

Special devices can be used for additional protection of the system of the secondary DC power supply. They include powerful varistors and thermocouples, which disconnect the varistor and generate a signal in case the varistor damaged, see Fig. 10.

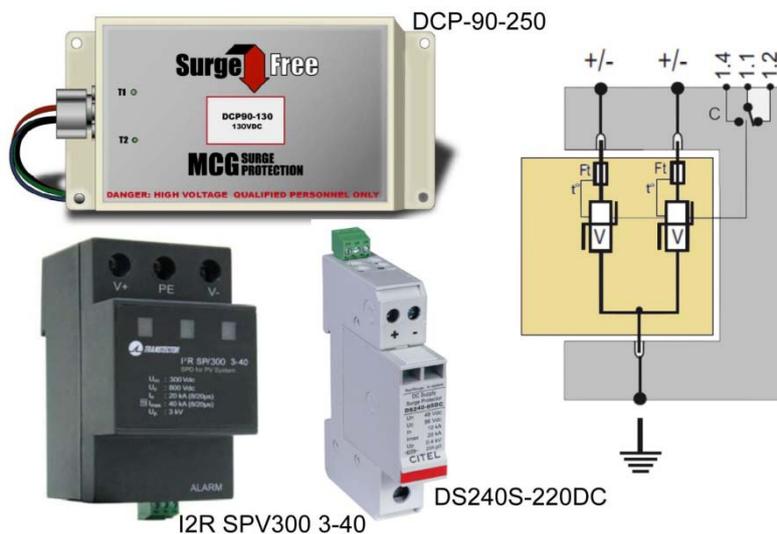


Fig. 10 : Protection devices for the system of secondary DC power supply

These devices are intended to protect the system of secondary DC power supply from impulse overloads.

#### IV. CONCLUSION

Thus, a conclusion can be made that today there are reliable methods of protection of DPR from all types of IRDI. The choice of one or another method of protection fully depends on a specific situation. The most comprehensive and efficient protection from all types of IRDI is provided by a complex protection, which includes both active and passive means of protection. It is clear that use of additional technical means will result in some degree of increase of relay protection system. However, taking into consideration that special

protection from IRDI is not necessary for all the DPRs, the total cost increase of an electric power facility will not be significant. Besides, it should be taken into consideration that the use of protection from IRDI significantly increases DPR resistance to common electromagnetic interference, i.e., improves reliability of its operation not only under possible extreme conditions, but also under normal operation mode conditions.

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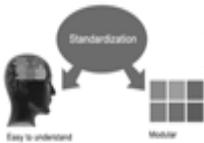
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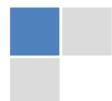


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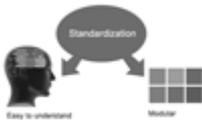
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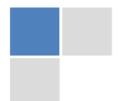
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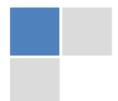
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