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Reducing Hearing Aid Power Consumption using Truncated-Matrix Multipliers

By Thomas L. Hemminger & E. George Walters

The Behrend College, United States

Abstract - The traditional platforms for implementing hearing aid algorithms have been application specific integrated circuits (ASIC) and some general purpose DSP chips. One of the most important issues involved in hearing aid design is power consumption, i.e., battery life. This paper introduces an alternative method for implementing hearing aid algorithms by using truncated-matrix multipliers. These designs can offer a significant reduction in power consumption and chip area. However, the approach can often increase computational error but it can be partially compensated for by introducing a method of coefficient shifting of the filter weights. This latter approach significantly reduces the computational error resulting in improved system performance.

Keywords : *truncated-matrix multipliers, hearing aids, power consumption, coefficient shifting, integer processing.*

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Reducing Hearing Aid Power Consumption using Truncated-Matrix Multipliers

Thomas L. Hemminger ^α & E. George Walters ^σ

Abstract - The traditional platforms for implementing hearing aid algorithms have been application specific integrated circuits (ASIC) and some general purpose DSP chips. One of the most important issues involved in hearing aid design is power consumption, i.e., battery life. This paper introduces an alternative method for implementing hearing aid algorithms by using truncated-matrix multipliers. These designs can offer a significant reduction in power consumption and chip area. However, the approach can often increase computational error but it can be partially compensated for by introducing a method of coefficient shifting of the filter weights. This latter approach significantly reduces the computational error resulting in improved system performance.

Keywords : truncated-matrix multipliers, hearing aids, power consumption, coefficient shifting, integer processing.

I. INTRODUCTION

Most modern hearing aids employ DSP algorithms running on application specific integrated circuits (ASICs) or on modern DSP chips. These algorithms are designed not only to amplify the overall audio signal but to selectively amplify those signals within specific frequency bands. Most all persons suffering from hearing loss lose the upper frequency range of hearing, requiring the audio signal to be separated into specific bands prior to processing [R. Chamberlain et al., 2003], [Y. Wei and Y. Lian, 2006]. For this reason the audio signal is usually separated into a large number distinct bands, or octaves, each amplified with a specific gain, and then the signals are recombined. A compressor stage is often employed to force the final signal to within the hearing range of the user. With the need for extensive signal processing and with the desire to have small unobtrusive devices, one of the main problems with hearing aids is battery life. Many of these devices run on a 1.3V battery drawing less than 2 mA and have a battery lifespan of about 100 hours of normal use [B. Edwards, 1998]. With this in mind we have endeavored to employ truncated-matrix multipliers to reduce the number of components, thus reducing the power consumption. This paradigm also has the added advantage of having less delay than full multipliers which can be beneficial to the user. As stated above, the cost is lower numerical accuracy, but

experiment has shown this not to be a significant issue in this work, the reason being that a small increase in truncation noise is beyond most users hearing range. Many current computational methods are based on weighted overlap-add (WOLA) filter banks, windowed finite impulse response (FIR) filter banks, lattice wave digital filter banks (LWDFB), or DFT methods [R. Vicen-Bueno, et al., 2007], [W. Wei, and D. Liu, 2011]. Here it was decided to simulate a hearing aid by employing the windowed FIR method using a Hamming window on the individual frequency bands. The results from using a full multiplier will be compared with those of the truncated-matrix multiplier. This will enable the development of a rough estimate of the power requirements based on the number of components. This paper is organized as follows. Section II describes the truncated-matrix multiplier, and includes the fundamental design and also a method to provide constant correction, to reduce final numerical error. It also provides the rationale for coefficient shifting thus improving the overall accuracy of the result. Section III introduces the simulations that were employed and section IV presents the results. The conclusions and some thoughts for further work are contained in section V.

II. TRUNCATED-MATRIX MULTIPLIERS

Truncated-matrix multipliers are designed by removing several of the least significant columns of the partial product, i.e., these products are not formed [E. G. Walters III and M. Schulte, 2011], [E. G. Walters III and M. Schulte, 2010], [E. G. Walters III, 2012], [T. Erdogan, et al., 2004], [E. E. Swartzlander, Jr., 1999]. As a result, they consume less power, less area, and can have a lower time delay than conventional multipliers. This does come at a cost of less accuracy which may or may not be an issue in certain applications. For example, audio processing mainly concerns perceived sound quality rather than absolutely precise numerical results. Research has shown that video processing does not often need to be precise as a first step in identifying objects in an image, e.g., facial recognition and video surveillance [T. T. Zin, et al., 2011]. In fact, a multi-level approach can be employed whereas the first level of numerical accuracy is lower, but as subjects are narrowed down, the analysis becomes more precise [J. S. Kim, et al., 2011].

In the numerically intensive domain of digital signal processing employment of the truncated

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multipliers can provide significant power savings over their full-width counterparts [J. M. Jou, et al., 1999]. These can be direct replacements for standard multipliers with little degradation in numerical performance. In general, FIR filters can have a significant number of smaller floating point coefficients. After converting them to signed integers the result is often a set of coefficients with many leading zeros (positive) or ones (negative) for sign extension. For this reason it is necessary to shift these coefficients to the left prior to multiplication to obtain greater accuracy. However, the operation is only performed on the filter coefficients and not on the incoming data since the bits corresponding to the filters can be modified prior to implementation. This leaves only one set of right shifts when the system is in real-time operation. FIR filters require a very simple set of multiply and add operations as shown in (1) for a T tap filter.

$$y[i] = \sum_{k=0}^{T-1} h[k]x[i-k] \quad (1)$$

Where $x[i]$ is the i^{th} value of the input stream and $h[k]$ is the set of filter coefficients. When using an odd number of taps the coefficients are symmetric and they yield a linear phase response, which is an attractive quality in audio signal processing. One way to reduce the number of multiplications is to add the two input data values of x_{i-k} and x_{i+k} prior to multiplication by the appropriate filter coefficient but this only increases the complexity of the basic circuit components. Table 1 shows the coefficients for one of the 63-tap filters used in this work.

The bandwidth of this filter ranges from 500 to 1000Hz and employs a Hamming window. The original rounded integer values of the filter are headed by $h[k]$. The number of left shifts is headed with S , and the new left-shifted values are in the next column to the right. The coefficients were developed using MATLAB and then quantized to 16-bit signed integers ranging from -32768 to +32767. Normally, when converting to 16-bit signed integers the coefficients need to be within the range of $[-1, 1-2^{-15}]$ and the multiplier becomes 2^{15} . This is followed by rounding the results. However, here the original coefficients for all the filters had magnitudes within the range of $[-0.5, 0.5-2^{-16}]$ so a multiplier of 2^{16} yielded results within the proper signed integer range, thus eliminating the need to normalize the data. For example, the value of tap $h[21]$ in Table 1 was originally -0.049036 which was then multiplied by 2^{16} and rounded to be represented as the 16-bit signed integer -3214. This indicates that the decimal point is implied to be to the right of the most significant (sign) bit. In fact, it is not a good idea to normalize the filters because their relative gains become corrupted by the normalization process. This in turn, unnecessarily complicates

computation of the new filter gains so it was decided not to perform that operation. As stated earlier, in order to preserve accuracy it is necessary to shift the bits of each coefficient as far to the left as possible. For example, in the top row the value of $h[0]$ is -12 which is shifted to the left by $S = 11$ bits yielding the rightmost column value of -24576. Note that the results in the right column range from -32768 to +32767 thus preserving the sign bit. After multiplication by the corresponding input data point and truncated by the r least significant columns the result from each tap is right shifted by the value of S to reestablish the proper magnitude. The result is then added to the summation. It is important to keep in mind that in practice the r least significant partial products are not formed in the first place to reduce power consumption. The design is illustrated in Fig. 1 where for simplicity an 8x8 multiplier has been synthesized. Those partial products in the r rightmost columns are never formed and there is no corresponding hardware for them.

Table 1: FIR filter with 63 taps

k	h[k]	S	2 ^S h[k]	k	h[k]	S	2 ^S h[k]
0	-12	11	-24576	32	4708	2	18832
1	-22	10	-22528	33	4042	3	32336
2	-29	10	-29696	34	3023	3	24184
3	-27	10	-27648	35	1773	4	28368
4	-10	11	-20480	36	438	6	28032
5	29	10	29696	37	-834	5	-26688
6	98	8	25088	38	-1911	4	-30576
7	200	7	25600	39	-2694	3	-21552
8	333	6	21312	40	-3131	3	-25048
9	482	6	30848	41	-3214	3	-25712
10	624	5	19968	42	-2981	3	-23848
11	724	5	23168	43	-2504	3	-20032
12	745	5	23840	44	-1876	4	-30016
13	647	5	20704	45	-1194	4	-19104
14	402	6	25728	46	-546	5	-17472
15	0	15	0	47	0	15	0
16	-546	5	-17472	48	402	6	25728
17	-1194	4	-19104	49	647	5	20704
18	-1876	4	-30016	50	745	5	23840
19	-2504	3	-20032	51	724	5	23168
20	-2981	3	-23848	52	624	5	19968
21	-3214	3	-25712	53	482	6	30848
22	-3131	3	-25048	54	333	6	21312
23	-2694	3	-21552	55	200	7	25600
24	-1911	4	-30576	56	98	8	25088
25	-834	5	-26688	57	29	10	29696
26	438	6	28032	58	-10	11	-20480
27	1773	4	28368	59	-27	10	-27648
28	3023	3	24184	60	-29	10	-29696
29	4042	3	32336	61	-22	10	-22528
30	4708	2	18832	62	-12	11	-24576
31	4939	2	19756				

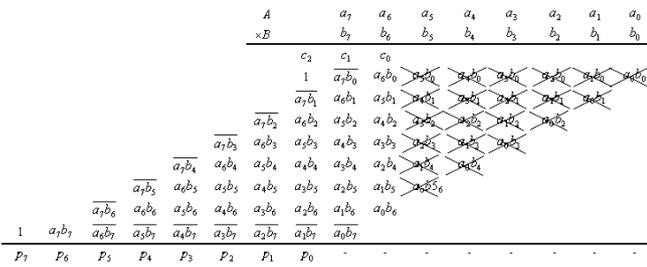


Figure 1 : An 8x8 truncated-matrix multiplier. This employs constant correction with $r = 6$ and $k = 2$

The remaining partial products are added column-wise to produce the desired product. Note that after the addition operation the k least significant bits are also truncated so that an 8 bit result is maintained ($p_0 - p_7$). Of course, the issue here is how to reduce the error from these operations. A number of methods are available in the literature as in [Y. C. Lim, 1992], [L. D. Van and C. C. Yang, 2005] but it was decided to choose a method that has worked well in previous simulations [M. J. Schulte, et al., 1993]. Here, each bit of the multiplier and multiplicand are considered to have equal probability of either being zero or one. In this case their partial product $a_i b_j$ should have an expected value of $1/4$ so the expected values of the unformed partial products are added to the expected round off error of the product. The sum is then rounded to the least significant column that has been formed. This produces the correction constant C which is expressed below in (2).

$$C = \text{round} \left(2^{-r} \left(2^{r+k-1} - 2^{r-1} - E_{r_mean} \right) \right) 2^r \quad (2)$$

This value is added to the partial product matrix (see Fig. 1) as bits $c_2 c_1 c_0$. The leading ones in some of the rows and the nand operations on some of the elements are necessary to produce the proper signed result. Once the truncated product has been formed it is necessary to compensate for the previous shifting operation on the filter coefficients. Without this procedure the accuracy of the result suffers as described in Fig. 2(a). The correction factor was not introduced here to simplify the figure. In this case the number B has several leading zeros and if r has a large value, where r is the number of truncated columns, the error becomes significant. If the number is small and negative then the most significant bit is one and several of the next most significant bits are also equal to one due to sign extension. As shown in Fig. 2(b) the number B has been left-shifted where the shift amount S is the number of consecutive bits immediately to the right of the sign bit that have the same value as the sign bit. From this example it is seen that for $B = 0000b_3b_2b_1b_0$ it should be left shifted by 3 bits to preserve the sign bit. The result is $B = 0b_3b_2b_1b_0000$, but note that three zero

bits are shifted in from the right, meaning that they reduce the effects of the unformed products. If instead the number is negative with $B = 1111b_3b_2b_1b_0$ the result from shifting would be $B = 1b_3b_2b_1b_0000$ which would also reduce the effects from the unformed products. Shifting to the right by S bits after multiplication reduces the error by a factor of 2^S . This does, however, introduce a non-symmetric round-off error. The shifted sum is rounded prior to truncation so this error has a mean value that is close to zero. Rather than adding a one to the right of the least significant bit p_0 prior to truncation, the rounding bit is added to the appropriate column of the partial product matrix prior to shifting by S bits. These bits are shown in bold in Fig. 2(b). Here the value of B is shifted three places so, $S = 3$, $s_1 = 1$ and $s_0 = 1$. This adds a value of one to the column containing a_7b_0, a_6b_1, a_5b_2 , and a_4b_3 . In this case the multiplier supports shifts from 0 to 3 but if there is no shift $s_1 = 0$ and $s_0 = 0$ and there are no additional bits required for rounding. The number of shifts for each filter coefficient is shown in table 1 where it can be seen that the errors from each multiplication are reduced by a factor of 2^S once the shifting operation has been completed. An n -bit barrel shifter can be used to shift the result back to the appropriate magnitude from the output of the multiplier. In fact, a four-stage barrel shifter can shift from zero to 15 places which cuts down on the amount of required hardware. This aspect is explained in greater detail in [M. R. Pillmeier, et al., 2002].

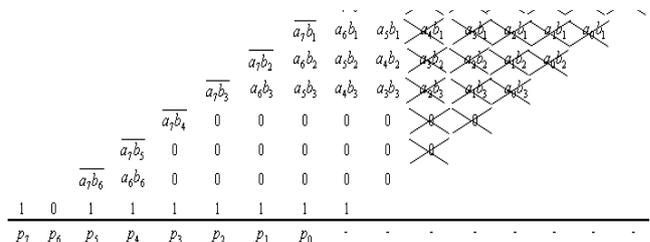


Figure 2 (a): Multiplication without coefficient shifting

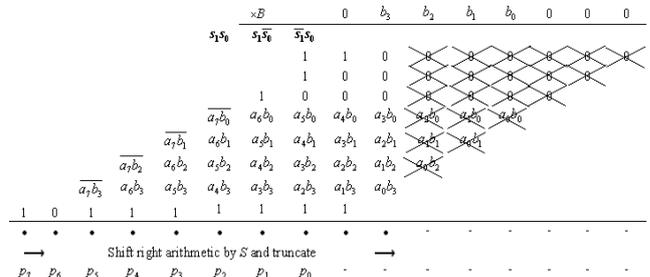


Figure 2 (b): Multiplication with coefficient shifting. $S = 3$

III. SIMULATIONS

This section describes the simulations that were employed when evaluating the performance of the multipliers. Fig. 3(a) shows an audiogram from a test subject indicating substantial high frequency loss in the left ear as compared to the right ear (see Fig. 3(b)). From the figure one can see that above a frequency of 2 kHz the subject has significant hearing loss, but at lower frequencies the response is relatively flat. This explains why the subject has little difficulty hearing a voice from a telephone with the left ear since that system is band-limited to about 3 kHz. There are a variety of hearing aid protocols, some having as many as 16 channels or more. However, for this work it was decided that to prove the efficacy of the design a reduced system with five channels would be sufficient. From Fig. 4 it can be seen that five channels were employed corresponding to a frequency range of 0 to 4 kHz, each having its associated gain. The subject's hearing is so poor above 4 kHz that it was deemed unnecessary to amplify sounds above that range. To be consistent with several other systems the sample rate was chosen to be 16 kHz using a 16-bit A/D converter. Each channel was amplified with gains that were determined by the losses indicated in the audiogram for the left ear. Studies have shown that using gain factors to cancel the measured losses shown in the audiogram do not produce acceptable results. For example, a hearing loss of 35-dB indicates an attenuation factor of about $10^{35/10} \approx 3160$. Instead, it has been determined through several studies over the years that using the half gain (or even the third gain) rule yields acceptable results. The half gain rule was chosen for these experiments. It involves amplifying the audio signal by one half of the auditory loss measured in dB. For example, if a person has a 35-dB loss within a specific frequency range it is acceptable to amplify the signal by 17.5-dB. This may seem counterintuitive, and certainly 17.5-dB is not anywhere near one half of 35-dB in terms of true gain or attenuation, but it is known that this is a good starting point when determining channel gains. Referring to Fig. 3(a) the gain to compensate for the channel centered on 3 kHz should be $10^{17.5/10} \approx 56$. To reduce the processing overhead and complexity, this value was converted to 64, and being a power of 2 corresponds to a shift operation of 6 bits. Since the rule is an approximation it was deemed that this would be an acceptable estimate. Fig. 4 shows the block diagram of the hearing-aid system used in this work. It illustrates the five channels of FIR filters that were employed along with their associated signal gains. When performing integer operations overflow is a concern, so the individual channels were not multiplied by their respective gains. In Fig. 4 it appears that channel three is multiplied by 2, channel four by 4, and channel five by 64. Instead, channel five remains unchanged and becomes the

reference channel in signal strength. Channel four is divided by 16 (right shift 4 bits), and channel three is divided by 32 (right shift 5 bits) with the remaining channels divided by 64. Of course, the final step is to recombine the channel outputs, next the result can be scaled up to provide the necessary overall gain. Fig. 5 illustrates the responses of each filter superimposed on the same frequency scale.

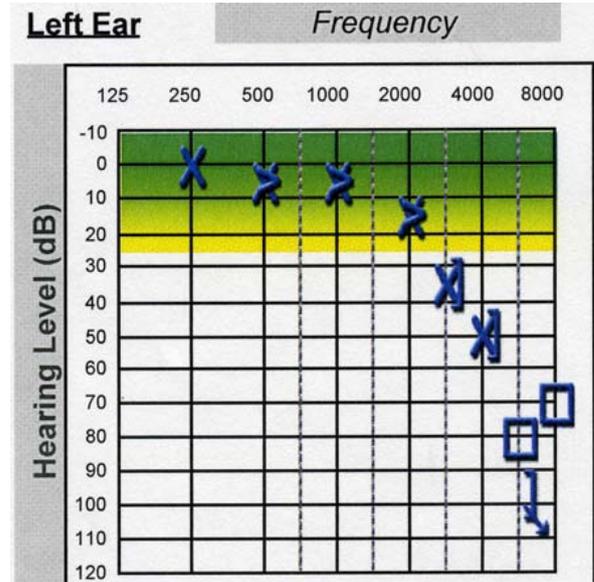


Figure 3 (a): Audiogram from test subject indicating substantial hearing loss in the left ear

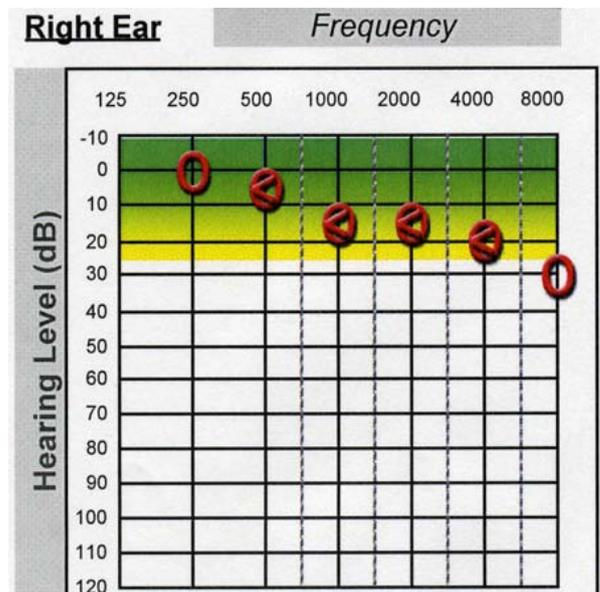


Figure 3 (b): Audiogram from test subject indicating some hearing loss in the right ear for comparison

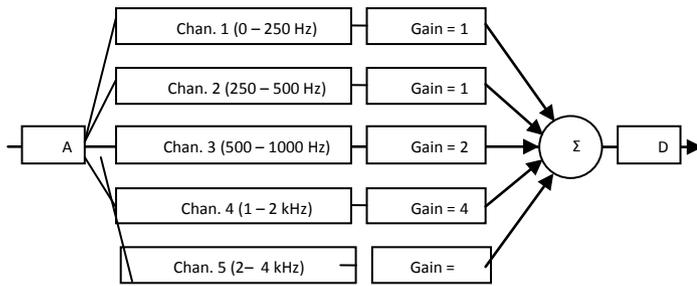


Figure 4 : Block diagram of digital signal processing Stage

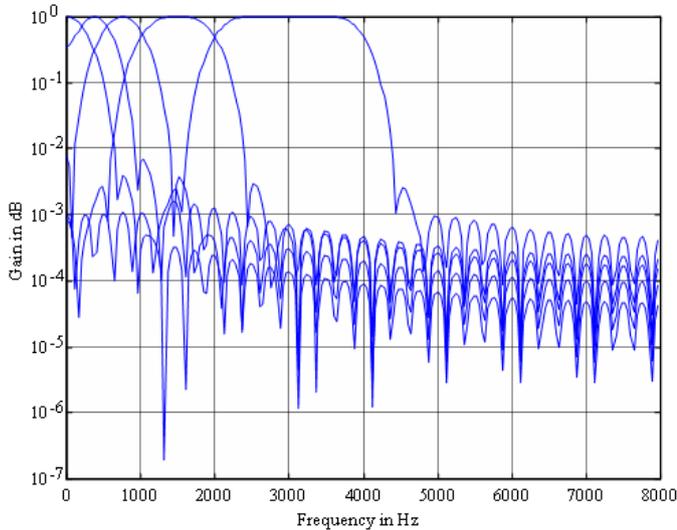


Figure 5 : The five channel filter prior to adjusting the gains

IV. RESULTS

The gains for this project were chosen to compensate for the hearing loss of the subject but also demonstrate a potentially significant dynamic range. It is not necessary for the gains (or attenuations) to be powers of two in order to capitalize on right and left shifts. By employing shifts accompanied by additions or subtractions, effective multiplication can be accomplished with many more gain factors. With 16-bit A/D sampling the quantization noise level is about 96-dB below moderate background levels. Therefore, this aspect will not be an issue since the subjects usually have limited aural acuity and cannot hear beyond a certain range. As a first experiment five sinusoids of equal magnitude were generated at a 16 kHz sample rate and combined into one file. These signals were chosen to correspond to the center frequencies of each filter, e.g., 125 Hz, 375 Hz, etc. The data file was processed with the five filters shown in Fig. 5 using full-width integer multipliers and compared against truncated-matrix multipliers ranging from $r=0$ to $r=15$. The normalized power spectrum of the result was computed as can be seen in Fig. 6 and it is apparent that the signals have been modified by the appropriate

gains corresponding to the filter channels. But more importantly this is for $r=15$. The plot resulting from the full-width multipliers looked identical so only this one was included.

The second experiment employed the use of uniformly distributed noise as an input signal. This was chosen so that the entire spectrum would be represented. From both experiments it was found that the error from increasing the value of r was virtually identical. Fig. 7 illustrates the mean-squared error between using full-width multipliers and progressively employing truncated arithmetic on both data sets. These numbers range from -32768 to +32767 yet the error for $r=15$ is just over five. Finally, Fig. 8 shows the normalized output spectrum from the white noise input separated into the individual channels, and multiplied by the associated gain factors. This and Fig. 6 illustrate that the weakest part of the subjects aural acuity is compensated for by an appropriate increase in signal gain. Lastly, the output signals from the sinusoids were provided to the test subject. The subject could not distinguish between any of the outputs whether using full-width multipliers or this new paradigm.

Next, it is useful to determine how this design can be beneficial to low-power, miniature devices. In the introduction it was stated that a standard hearing aid consumes about 2 mA and has a battery life of about 100 hours of normal use. It is also commonly known that a great deal of the required power consumption is directly due to the arithmetic units. For a 16x16 bit multiplier the number of AND gates (multipliers) is of order 256. However, with truncation of $r=15$ this could be reduced to $256 - [1 + 2 + 3 + \dots + 15] = 136$. This translates into about 53% of the original number. This does not include the barrel shifters but there are far less of those devices. From some earlier work and from the experiments conducted for this paper it appears that there can be an approximate hardware reduction of about 40% compared to conventional methods and it is quite possible that this could translate into roughly a 50 - 60% increase in battery life without any appreciable reduction in signal quality. Even a 40 - 50% increase would be a substantial improvement over the norm translating into about 150 hours of normal use.

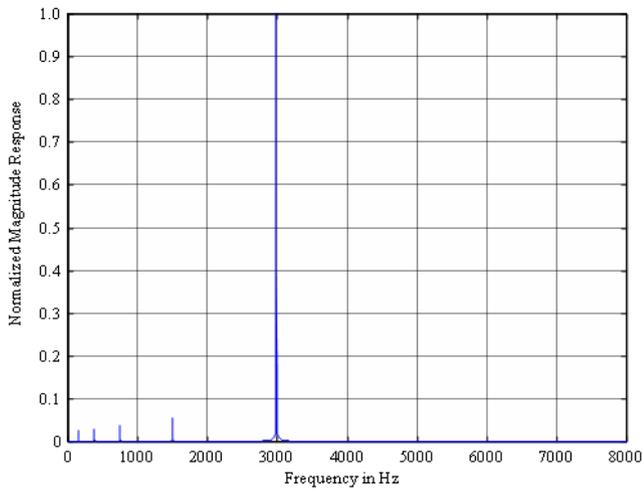


Figure 6 : Responses from five sinusoids. Their amplitudes were originally equal but now reflect the effects of gain

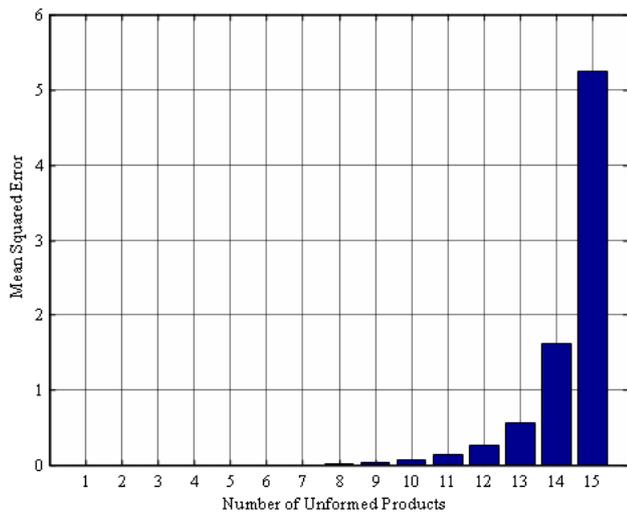


Figure 7 : Error against number of unformed product columns

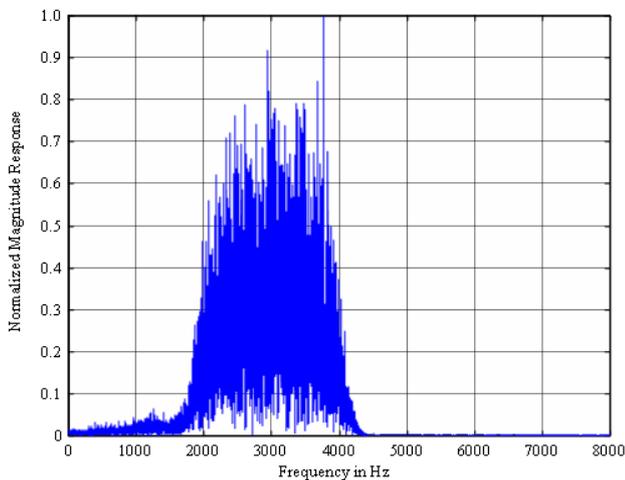


Figure 8 : Response of each filter with its associated gain from a white noise input

V. CONCLUSION

The results from this work were more encouraging than originally expected. Reducing the number of formed multiplier stages had a small numerical effect that was not discernible in the visual plots. Furthermore, the test subject could not determine the difference between the full-width integer or truncated arithmetic approaches. This was obviously a limited and preliminary experiment and the goal is to place this design on an ASIC so that a full hardware implementation can be realized. The development of high quality signal processing algorithms utilizing low power components is important. It is especially relevant when designing small consumer electronics like cell phones and hearing aids where consumers need to either recharge or replace batteries on a regular basis. There could be a wide application of this technology in the areas of signal and image processing. For example, smart phones, MP3 players, and tablet computers could be designed to employ this technology when performing video and audio processing where data loss is not critical. Other areas that have been suggested are facial and voice recognition along with data reduction techniques, e.g., JPEG and MPEG. For facial recognition the original data can be reduced in resolution using lower numerical accuracy prior to using higher precision methods. Lastly this technology could be employed to develop faster FFT algorithms which could also be useful in a large number of signal processing applications [R. Jiang, 2007].

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Performance Analysis of Building Integrated Photovoltaic Application with Tilt and Azimuth Angle in Bangladesh

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Keywords : tilt angle, azimuth angle, BIPV, solar irradiance.

GJRE-F Classification : FOR Code: 850504



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Performance Analysis of Building Integrated Photovoltaic Application with Tilt and Azimuth Angle in Bangladesh

Md. Hafizur Rahman ^α & Jinia Afrin ^σ

Abstract - This paper analyzes the dependency of power output of the building integrated photovoltaic application in Bangladesh on various tilt and azimuth angle. Again this paper shows the temperature dependency of the output power of the building integrated photovoltaic application in Bangladesh. From the analysis, it is seen that if tilt angle is decremented from 90 deg to 1 deg, the power of proposed arrays is incremented by 7.88% keeping azimuth angle fixed at 0 deg. If azimuth angle is incremented from 0 deg to 180 deg, the power is decremented by 46.72% keeping tilt angle fixed at 21 deg.

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I. INTRODUCTION

The BIPV application is a very important issue to overcome the world energy crisis. Now the building owners not only can fulfil their electricity demand but also can sell the surplus energy produced following this advanced system. Hence this BIPV system is getting highly preferable to the building owners for fulfilling the energy demand. According to the International Energy Agency (IEA), PV-suitable surfaces can be increased by about 35% incorporating BIPV on building facades [1], [2].

The performance of the BIPV is highly dependent on the tilt and azimuth angle. Since BIPV is related with fixed angle orientation of the solar modules, the optimum possible tilt angle orientation should be considered before building construction. For this reason this paper highlights the influence of tilt and azimuth angle on the BIPV application considering time and temperature issue.

II. SOLAR IRRADIANCE

Solar radiation is a very important factor that directly affects the solar cell output performance. Fig. 1 shows the radiation spectrum for the extraterrestrial space (AM0) & for the sea level or earth's surface (AM1.5). The irradiated solar energy is 1.353kW/m² at the average distance between sun and the earth. The

irradiation considered for the earth's surface is approximately 1kW/m² which is a reference value since it depends on many factors. The AM1.5 is a standard for the PV device whose surface is tilted at 37° facing the sun rays [4].

A solar cell is mainly designed for absorption of a portion of the total radiation spectrum. From the Fig. 1, it is seen that a large amount of irradiance spectral is available in the visible spectrum (390nm-700nm) which stands in the opposition of the UV (<390nm) and infrared light (>750nm). PV solar cells are designed for the absorption of the visible spectrum only [3], [5].

Table 1: Daily Average Bright Sunshine Hours In Dhaka City

Month	Daily mean	Minimum	Maximum
January	8.7	7.5	9.9
February	9.1	7.7	10.7
March	8.8	7.5	10.1
April	8.9	7.2	10.2
May	8.2	5.7	9.7
June	4.9	3.8	7.3
July	5.1	2.6	6.7
August	5.8	4.1	7.1
September	6.0	4.8	8.5
October	7.6	6.5	9.2
November	8.6	7.0	9.9
December	7.55	6.03	9.13

The solar irradiation exposed to the PV array for fixed position is calculated from the following equations [6].

$$G_s = G_d + G_r \quad (1)$$

Where, G_s is total solar irradiation in kW/m², G_d is direct component of solar irradiation in kW/m² and G_r is diffuse component of Solar Irradiation in kW/m².

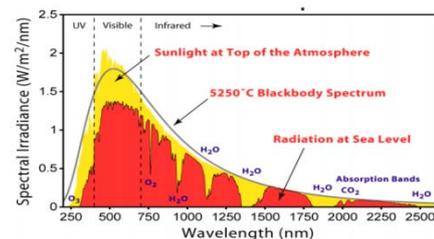


Figure 1 : Practical solar radiation spectrum [11]

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$$G_d = (H \cos \theta - \sin \theta \cos \alpha \sin \delta \cos \varphi_n + \sin \theta \cos \alpha \sin \varphi_n \cos \omega + \sin \theta \sin \alpha \cos \delta \sin \omega) \times G_{od} \quad (2)$$

Where, H is sun elevation, θ is oblique angle of the sun in radian, α is azimuth angle, δ is declination of the sun in radian, φ_n is north latitude, ω is hour angle in degree, G_{od} is direct irradiation in radian.

$$G_r = \frac{G_{or}(1 + \cos \theta)}{2} + 0.2G_o \frac{1 - \cos \theta}{2} \quad (3)$$

Where, G_{or} is diffuse (horizontal) irradiation in radian, G_o is global horizontal irradiation in kW/m². The sun elevation is given by (4) [6].

$$H = \sin^{-1}(\cos L \cos D \cos T + \sin D \sin L) \quad (4)$$

Where L is latitude in degree, D is declination of the sun in degree, T is hour angle in degree [6].

From Table 1, daily average sunshine hours are obtained from which the idea of average amount of solar power generation can be achieved. This type of statistics can help to determine the optimum tilt angle for grid connected building integrated photovoltaic application. Again, Fig. 2 represents the practical data curve of the solar irradiance against time which is obtained at KUET campus of Khulna city at 7th March, 2012.

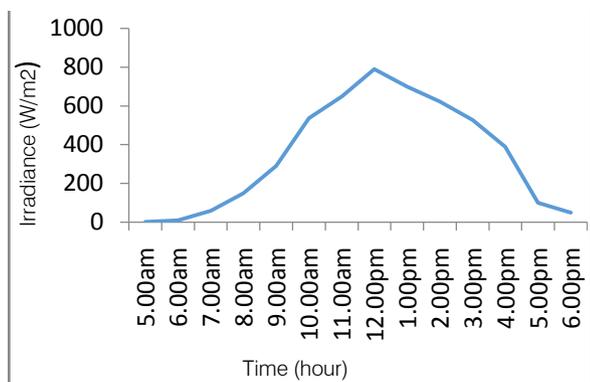


Figure 2 : Practical solar irradiance preview against time at KUET campus of Khulna city at 7th March

III. TILT AND AZIMUTH ANGLE

The BIPV system performance is mostly affected by tilt and azimuth angles. The solar irradiance exposed on the array is highly affected by the tilt and azimuth angles. The optimum tilt angle depends on the local latitude. According to Duffie and Beckman the optimum angle is $\beta_{opt} = (\phi + 15 \text{ deg}) \pm 15 \text{ deg}$ (where ϕ is local latitude) [7]. In the winter and summer season the tilt angle is to be increased and decreased respectively. The optimum tilt angle is 10° for March to

September and 40° for October to February estimated for November 2007 to October 2008 at Dhaka in Bangladesh [10].



Figure 3 : Orientation of PV modules at 4 different slopes [9]

Since it is not possible to move the PV panel for BIPV system, it is needed to analyze the yearly performance to obtain optimum average solar irradiation with consideration of tilt and azimuth angles. For a fixed orientation of PV panels the optimum tilt angle is calculated mathematically given by Eq. 5 [8].

$$\frac{d}{d\beta} \left(\sum_{i=1}^n G_{tt}(i) \right) = 0 \quad (5)$$

Where $G_{tt}(i)$ is the total irradiance for i hours and n is the total number of hours.

From Fig. 3, it is seen that there are 4 modules oriented at different slopes which can be taken as a model to analyze experimentally, where the researcher found that the monthly solar irradiation and temperature is 131kW/m² and 25°C respectively.

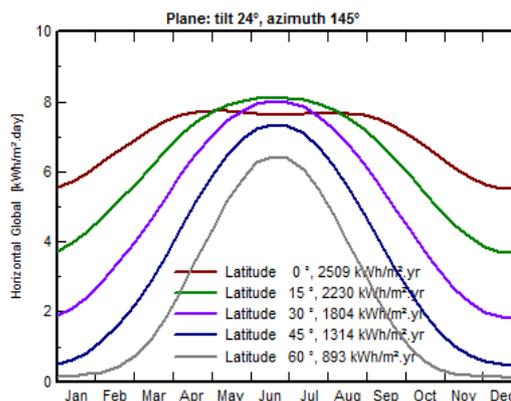


Figure 4 : Monthly Horizontal global radiation for different latitudes in Dhaka

At the tilt angle of 24° and azimuth of 145° monthly horizontal global radiation which is peak at June and July month is shown by Fig. 4. From figure it is seen

that the horizontal global radiation is increased for decrement of latitudes.

IV. SIMULATION OF PV ARRAY AT VARIOUS TILT AND AZIMUTH ANGLES

For simulation purpose two proposed arrays are taken in which each array consists of 50 strings in parallel and each string consists of 20 modules in series. The module taken for simulation is Solarex MSX-64. From the simulation study, eight various curves are obtained. From Fig. 5 to Fig. 8, it is seen that the obtained maximum powers are 114.66 KW (when tilt/azimuth angle is $21^{\circ}/0^{\circ}$), 61.3 KW (when tilt/azimuth angle is $21^{\circ}/180^{\circ}$), 95.18 KW (when tilt/azimuth angle is $1^{\circ}/0^{\circ}$) and 88.23 KW (when tilt/azimuth angle is $90^{\circ}/0^{\circ}$) respectively considering temperature throughout the day. Again from Fig. 9 to Fig. 12, it is seen that the maximum powers are obtained during 10:00hr to 13:30hr. So from these simulations it is seen that if azimuth angle is varied from 0° to 180° , 106.48 KW power can be improved keeping tilt angle fixed at 21° and if tilt angle is varied from 1° to 90° , 6.95 KW power can be improved keeping azimuth angle fixed at 0° at the time of 11:30hr.

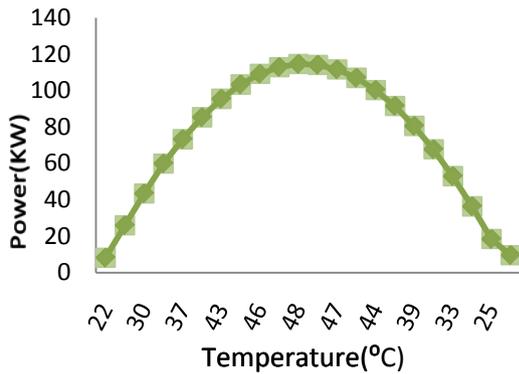


Figure 5 : Power data obtained against Temperature when Tilt/Azimuth is $21^{\circ}/0^{\circ}$

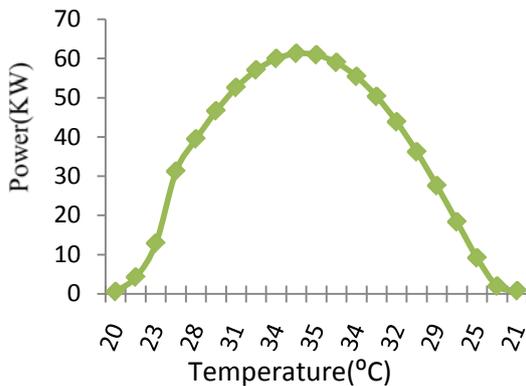


Figure 6 : Power data obtained against Temperature when Tilt/Azimuth is $21^{\circ}/180^{\circ}$

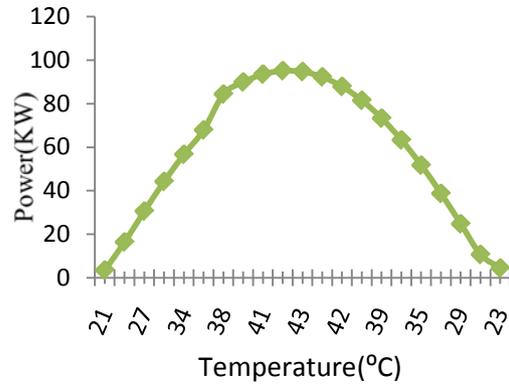


Figure 7 : Power data obtained against Temperature when Tilt/Azimuth is $1^{\circ}/0^{\circ}$

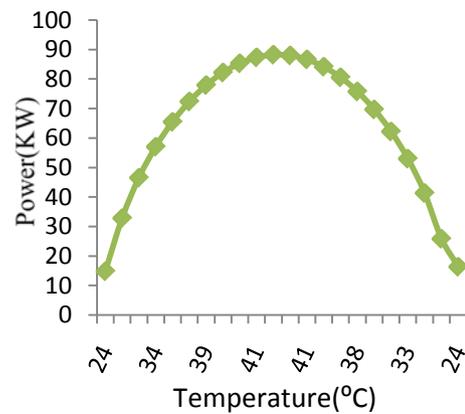


Figure 8 : Power data obtained against Temperature when Tilt/Azimuth is $90^{\circ}/0^{\circ}$

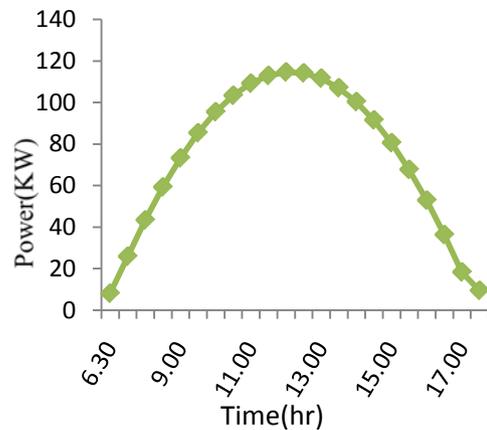


Figure 9 : Power data obtained against Temperature when Tilt/Azimuth is $21^{\circ}/0^{\circ}$

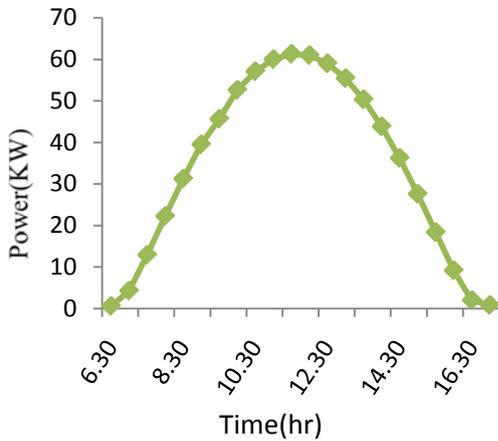


Figure 10 : Power data obtained against Time when Tilt/Azimuth is 21°/180°

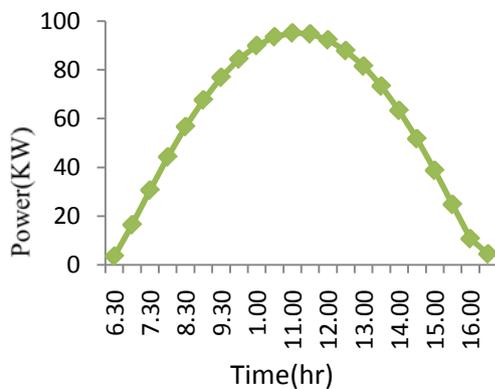


Figure 11 : Power data obtained against Time when Tilt/Azimuth is 1°/0°

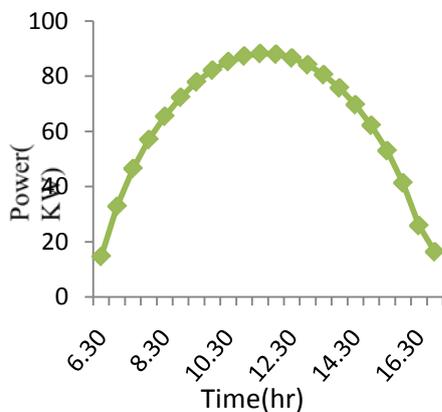


Figure 12 : Power data obtained against Time when Tilt/Azimuth is 90°/0°

V. CONCLUSION

The power performance of the Building integrated photovoltaic application is analyzed in the case of Bangladesh climate condition. In the BIPV application the tilt and azimuth angle should be considered strongly for optimization of power. The optimum tilt angle especially for BIPV should be

determined very carefully since PV modules are to be oriented at a fixed tilt angle. From the case study it is seen that both tilt and azimuth angle optimization plays a vital role for obtaining the optimal power.

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Sliding Mode Observer of a Grid Connected Photovoltaic Generation System with Active Filtering Function

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Keywords : harmonics, three phase apf, PWM rectifier, DPC, virtual line flux linkage observer, mvbpf, PV, sliding mode(SM), SMO.

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Sliding Mode Observer of a Grid Connected Photovoltaic Generation System with Active Filtering Function

A. Djerioui ^α, K. Aliouane ^σ & F. Bouchafaa ^ρ

Abstract - The first problem in our third millennium is energy. For this reason, we try to find a new solution to develop different ways of distribution and energy use. This article presents the design of a sliding mode controller using sliding mode observation technique which aims to simplify the control procedure. For ameliorating the quality of the energy transferred from the power supply to the load, and minimizing the harmful effects of the harmonics generated by nonlinear load. The virtual grid flux vector estimated in the sliding-mode observer yields robustness against the line voltage distortions. We propose a new multi-function converter as an efficient solution to improve the power quality. The good dynamic and static performance under the proposed control strategy is verified by simulation.

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I. INTRODUCTION

The widespread use of power electronics in domestic and industrial applications had induced power line losses and electrical interference problems, which resulted in low power factor, efficiency and bad quality of the power electrical distribution system.

Classical solutions use passive filters, made up of capacitors and inductors, to reduce line current harmonics and to compensate reactive power. But these filters have several drawbacks: risk of parallel and series resonance with the AC source, bulky passive components, and low flexibility due to fixed compensation characteristics.

Active filters can be connected in series or in parallel to the nonlinear loads. Shunt active filters are the most important and widely used industrial processes for active filtering. The main purpose of shunt filters is to cancel the load current harmonics fed to the supply, so that the power supply needs only to feed the fundamental active current component.

In this frame, photovoltaic generation systems have the opportunity to be as much as suitable for their important advantage being able to produce electrical energy very close to the electric loads. In this way the transmission losses are avoided and it is also possible to satisfy the daily load diagrams' peaks since they supply the maximum power quite in correspondence to the maximum request.

The sliding mode control (SMC) is one of the popular strategies to deal with uncertain control systems [9]. The main feature of SMC is the robustness against parameter variations and external disturbances. Various applications of SMC have been conducted, such as robotic manipulators, aircrafts, DC motors, chaotic systems, and so on [10]

The motivation for this work was to design a digitally controlled, combination active filter and photovoltaic (PV) generation system.

Sliding Mode Control of a Grid Connected Photovoltaic Generation System with Active Filtering Function

The motivation for this work was to design a digitally controlled, combination active filter and photovoltaic (PV) generation system. This work focuses on a proposed control scheme for the dual function system and on the effects of delay on the control of an active filter. The scheme of the proposed multi-function converter is shown in Fig.1

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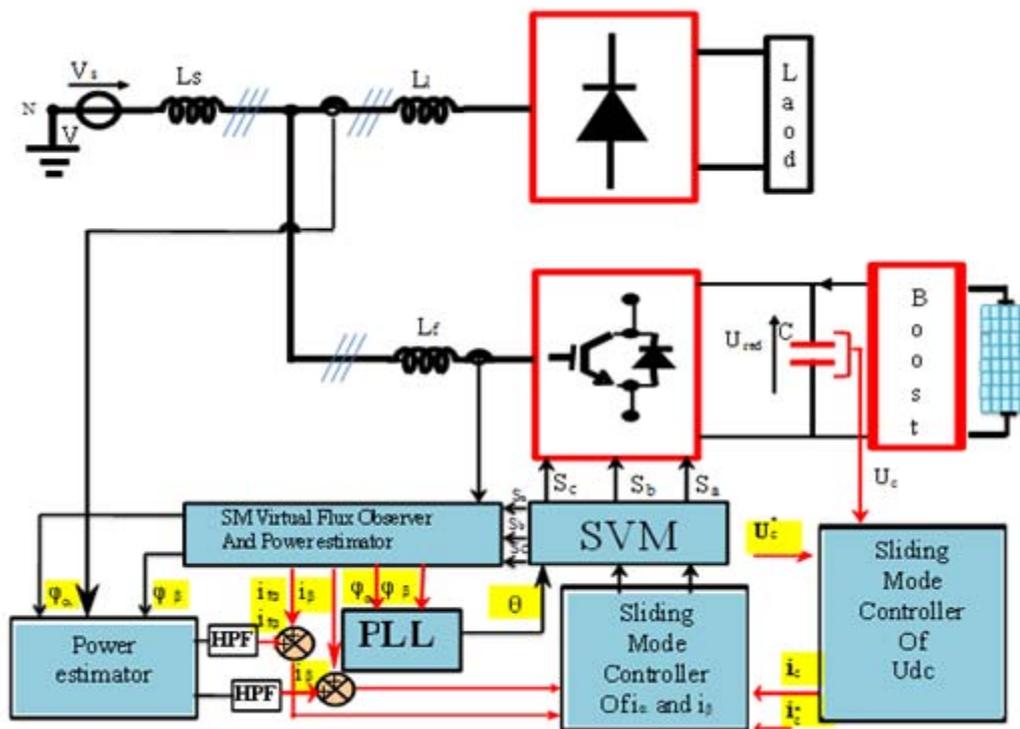


Figure 1 : Scheme of the multi-function converter

a) Modelling of the PVG

The mathematical model of the PVG is given by model 1.

$$I = I_{sc} - I_0 \left[e^{\left(\frac{V + IR_{sr}}{nkT_c/q} \right)} - 1 \right] - \frac{V + IR_{sr}}{R_{sh}} \quad (1)$$

With I and V are respectively the PV current and voltage, I_0 : leakage or reverse saturation current, q: electron charge, n: Ideality factor, K is the Boltzman's constant ($1.38 \cdot 10^{-23}$ J/K), R_{sr} :series cell resistance, R_{sh} :shunt cell resistance.

b) Boost converter

The Boost converter shown in Figure 2, it has step-up conversion ratio. Therefore the output voltage is always higher than the input voltage. The converter will operate throughout the entire line cycle, so the input current does not have distortions and continuous. It has a smooth input current because an inductor is connected in series in with the power source. In addition the switch is source-grounded; therefore it is easy to drive.

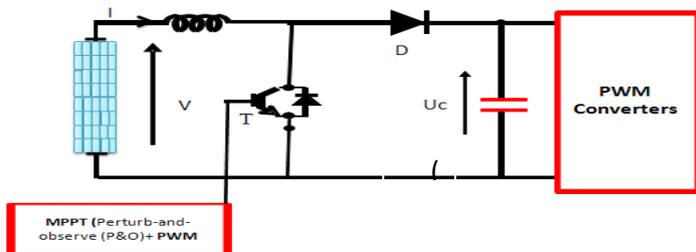


Figure 2 : Boost Converter

c) Mathematical Model of PWM Converters

A three phase voltage inverter is used to interface the PVG with the grid by converting the dc power generated by the PVG into AC power to be injected to the grid. The dynamic model of a PWM DC-AC Converter can be described in the well known (d-q) frame through the Park transformation as follows [1], see appendix:

$$\begin{aligned} \frac{di_{fd}}{dt} &= \frac{-R_f}{L_f} i_{fd} + \omega i_{fq} + \frac{1}{L_f} v_{fd} - \frac{v_{sd}}{L_f} \\ \frac{di_{fq}}{dt} &= \frac{-R_f}{L_f} i_{fq} + \omega i_{fd} + \frac{1}{L_f} v_{fq} - \frac{v_{sq}}{L_f} \\ \frac{dU_c}{dt} &= \frac{d_d}{C} i_{fq} + \frac{d_q}{C} i_{fd} \end{aligned} \quad (2)$$

Where d_{q1}, d_{q2} d- Axis and q- axis switching state functions, \hat{v}_{sd} and \hat{v}_{sq} - d- Axis and q- axis supply voltages.

The bi-directional characteristic of the converter is very important in this proposed photovoltaic system, because it allows the processing of active and reactive power from the generator to the load and vice versa, depending on the application. Thus, with an appropriate control of the power switches it is possible to control the active and reactive power flow.

$$\begin{bmatrix} \hat{v}_d \\ \hat{v}_q \end{bmatrix} = \frac{1}{i_{fd}^2 + i_{fq}^2} \begin{bmatrix} i_{fd} & -i_{fq} \\ i_{fq} & i_{fd} \end{bmatrix} \begin{bmatrix} P \\ Q \end{bmatrix} \quad (3)$$

Where \hat{v}_d and \hat{v}_q are the estimated main line

d) *The Regulators Synthesis*

The state equations are shown in (4) and summarized as (5)

$$S = \begin{bmatrix} S_d \\ S_q \end{bmatrix}; E_f = I^* - I; I^* = \begin{bmatrix} i_{fd}^* \\ i_{fq}^* \end{bmatrix}; K_{SMP} = \begin{bmatrix} k_{SMPd} & 0 \\ 0 & k_{SMPq} \end{bmatrix}; K_{SMI} = \begin{bmatrix} k_{SMId} & 0 \\ 0 & k_{SMIq} \end{bmatrix} \quad (7)$$

Where k_{SMPd} , k_{SMPq} , k_{SMId} and k_{SMIq} are positive constants And consequently, their temporal derivatives are given by:

$$\dot{S} = K_{SMP} \dot{E}_f + K_{SMI} E_f \quad (8)$$

$$u_{eq} = \begin{bmatrix} u_{eqd} \\ u_{eqq} \end{bmatrix} = (K_{SMP} B)^{-1} [K_{SMI} E_f - K_{SMP} (AI + Bu - G + I^*)] \quad (10)$$

Finally, the control law is given by:

$$u = u_{eq} + u_{dis} = \begin{bmatrix} u_{eqd} + u_{disd} \\ u_{eqq} + u_{disq} \end{bmatrix} = \begin{bmatrix} u_{eqd} + k_{sd} \text{sign}(S) \\ u_{eqq} + k_{sq} \text{sign}(S) \end{bmatrix} \quad (11)$$

For the sliding mode DC-link voltage controller based on integrator can be determined by substituting the reference line current, is chosen to determine switching surface functions:

$$S_{dc} = K_{SMPc} (U_c^* - U_c) + K_{SMIC} \int (U_c^* - U_c) dt \quad (12)$$

And consequently, their temporal derivative is given by:

$$\dot{S}_{dc} = K_{SMPc} (\dot{U}_c^* - \dot{U}_c) + K_{SMIC} (U_c^* - U_c) = 0 \quad (13)$$

Finally, the control law is given by:

$$i_{ceq} = C \left(\frac{K_{SMIC}}{K_{SMPc}} (U_c^* - U_c) + \dot{U}_c^* \right) + K_{SC} \text{sig} (U_c^* - U_c) \quad (14)$$

$$\begin{bmatrix} \frac{di_{fd}}{dt} \\ \frac{di_{fq}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & w \\ -w & \frac{-R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ \frac{1}{L_f} \end{bmatrix} \begin{bmatrix} v_{fd} \\ v_{fq} \end{bmatrix} - \begin{bmatrix} \frac{v_{sd}}{L_f} \\ \frac{v_{sq}}{L_f} \end{bmatrix} \quad (4)$$

$$\dot{I} = AI + Bu - G \quad (5)$$

The sliding surfaces (S) are equal to the error of state variables, which can be express as:

$$S = K_{SMP} E_f + K_{SMI} \int E_f dt \quad (6)$$

Where

The equivalent control can be calculated from the formula $\dot{S} = 0$, and the stabilizing control is given to guarantee the convergence condition (5).

$$\dot{S} = K_{SMP} \dot{I}^* + K_{SMI} E_f - K_{SMP} (AI + Bu - G) = 0 \quad (9)$$

The equivalent control u_{eq} is deduced by imposing the sliding regime condition \dot{S} obtaining:

The sliding mode observer uses the system model with the sign feedback function. The continuous time version of the SMO is described by Equation (15).

$$\frac{d}{dt} \begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} = \frac{1}{L_f} (\lambda \cdot \text{sign} \left(\begin{bmatrix} i_{f\alpha} - i_{fcest} \\ i_{f\beta} - i_{fbest} \end{bmatrix} \right)) (\mathbf{1} R_f \begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} - \begin{bmatrix} v_{f\alpha} \\ v_{f\beta} \end{bmatrix}) \quad (15)$$

The estimated values of the grid voltage are obtained from the low-pass filter:

$$\begin{bmatrix} v_{s\alpha est SMO} \\ v_{s\beta est SMO} \end{bmatrix} = LPF (\lambda \cdot \text{sign} \left(\begin{bmatrix} i_{f\alpha} - i_{fcest} \\ i_{f\beta} - i_{fbest} \end{bmatrix} \right)) \quad (16)$$

While the $(\alpha-\beta)$ components of the virtual grid flux are calculated as follows:

$$\begin{bmatrix} \varphi_{\alpha est} \\ \varphi_{\beta est} \end{bmatrix} = (\lambda \cdot \int \text{sign} \begin{bmatrix} i_{f\alpha} - i_{f\alpha est} \\ i_{f\beta} - i_{f\beta est} \end{bmatrix} dt) + \begin{bmatrix} \varphi_{\alpha est 0} \\ \varphi_{\beta est 0} \end{bmatrix} \quad (17)$$

Hence the structure of the virtual grid flux sliding-mode observer presented in Fig.3.

The sliding surface representing the error between the measured and references currents are given by this relation.

$$\begin{bmatrix} \sigma_{\alpha} \\ \sigma_{\beta} \end{bmatrix} = \begin{bmatrix} i_{f\alpha} - i_{f\alpha est} \\ i_{f\beta} - i_{f\beta est} \end{bmatrix} \quad (18)$$

The sliding mode will exist only if the following condition

$$\dot{\sigma}_{\alpha\beta} \sigma_{\alpha\beta} < 0 \quad (19)$$

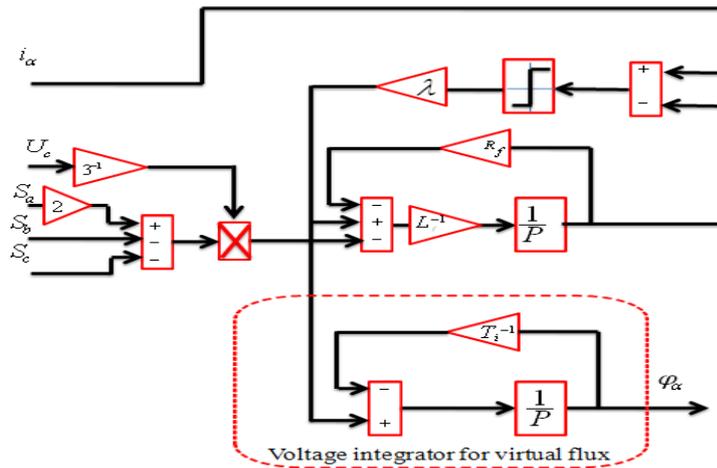


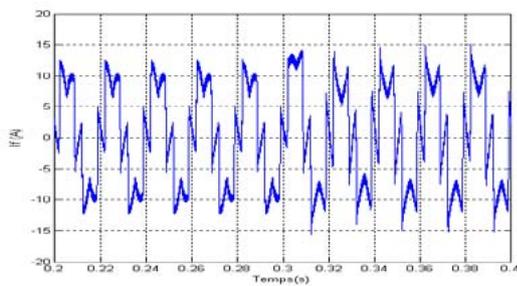
Figure 3 : Sliding-mode current observer for virtual grid flux

II. SIMULATION RESULT

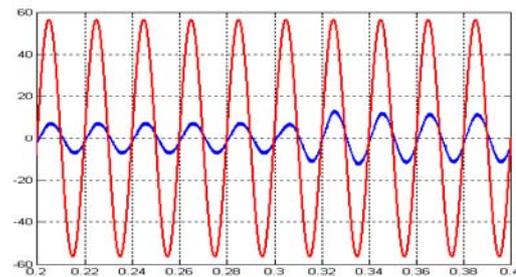
In simulation part, power system is modeled as 3wired 3-phase system by an RL load with uncontrolled diode rectifier. In the circuit, the ac source with frequency of 50Hz. The grid side line voltage is 220V. The line resistor is 0.25Ω. The line inductance of each

phase is 1mH. The dc capacitor is 5000μF; the dc voltage is set to be 700V. The switching frequency for three-phase is 15 kHz.

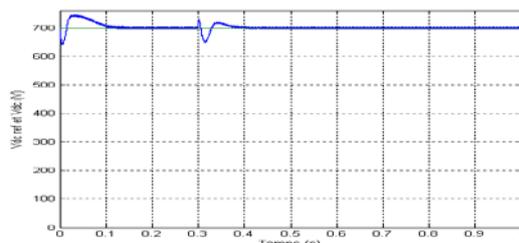
The Pv model applied in simulation is as Fig .4. Whose parameters are regulated for normal condition (25°C Temp. and sun radiation G=1kW/m).



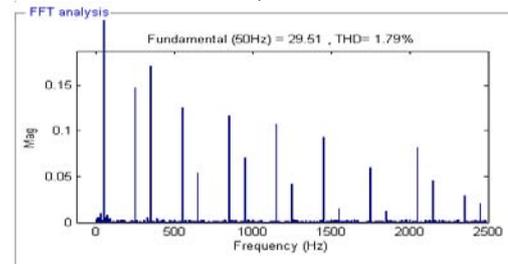
A)



B)



C)



D)

Fig.7. Simulated responses for a step change in the load resistor: A) Harmonic currents injected by the active power filter, Load change at 0.3 s. B) Source voltage, source current. C) DC side capacitor voltage and filter D) Current spectrum harmonic: Grid in Phase 1.

a) *Sliding mode control of a grid connected photovoltaic generation system with active filtering function*

The current reference of the active filter and the generated one are superposed in the same Fig.7.A

The Fig. 7.B. shows the behavior of the current and voltage in Phase 1 of the grid,. It is noted the linear currents are sinusoidal and the control technique presents a very good dynamic behavior, almost sinusoidal as well as in phase with line voltage, which gives near-to-unity power factor.

Fig .7.D shows simulation results for the DC bus voltage controller. The voltage vdc on the DC side of the inverter is stable and regulated around its reference. The THD before filtering for the first line is 27.46 % and becomes 1.79% after filtering.

III. CONCLUSION

This paper outlined the modeling and development of the control system for the active filter/PV generation system with sliding mode controller based on a Sliding Mode Observer. The results verify the validity of the proposed control scheme. Unity power factor is achieved, active and reactive current are decoupled controlled in the synchronous reference frame and the objective of maintaining balanced voltages in DC-link capacitors is carried out effectively with the proposed SVM, and it offers sinusoidal line currents (low THD) for ideal and distorted line voltage .

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Advanced Receiver Architectures in Radio - Frequency Applications

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Abstract - The general principles of several types of receivers fall under the two main headings of TRF (tuned radiofrequency) receivers, where the received signal is processed at the incoming frequency right up to the detector stage, and the superhet (supersonic heterodyne) receiver, where the incoming signal is translated (sometimes after some amplification at the incoming frequency) to an intermediate frequency for further processing. There are however, a number of variants of each of these two main types. Regeneration ('reaction' or 'tickling') may be applied in a TRF receiver, to increase both its sensitivity and selectivity. This may be carried to the stage where the RF amplifier actually oscillates – either continuously, so that the receiver operates as a synchrodyne or homodyne, or intermittently, so that the receiver operates as a super-regenerative receiver, both of which have been described previously. The synchrodyne or homodyne may be considered alternatively as a superhet, where the IF (intermediate frequency) is 0 Hz. In this paper we present the new type of receiver architectures which work in radiofrequencies.

Keywords : *supersonic heterodyne, tuned radio frequency.*

GJRE-F Classification : *FOR Code: 890405*



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Advanced Receiver Architectures in Radio-Frequency Applications

Solomon Lule Workneh ^α, Dr.M V Raghavendra ^σ, Dr. Vuda Sreenivasarao ^ρ & Dr. Babu PG Reddy ^ω

Abstract - The general principles of several types of receivers fall under the two main headings of TRF (tuned radiofrequency) receivers, where the received signal is processed at the incoming frequency right up to the detector stage, and the superhet (supersonic heterodyne) receiver, where the incoming signal is translated (sometimes after some amplification at the incoming frequency) to an intermediate frequency for further processing. There are however, a number of variants of each of these two main types. Regeneration ('reaction' or 'tickling') may be applied in a TRF receiver, to increase both its sensitivity and selectivity. This may be carried to the stage where the RF amplifier actually oscillates – either continuously, so that the receiver operates as a synchronyne or homodyne, or intermittently, so that the receiver operates as a super-regenerative receiver, both of which have been described previously. The synchronyne or homodyne may be considered alternatively as a superhet, where the IF (intermediate frequency) is 0 Hz. In this paper we present the new type of receiver architectures which work in radiofrequencies.

Keywords : *supersonic heterodyne, tuned radio frequency.*

I. INTRODUCTION

The dominant receiver architecture, since the 1930s, has been the superhet in various forms, replacing the earlier TRF sets. Prior to and for a while after the Second World War 'table radio' sets were popular, typically with long, medium and short wave bandstand a 5 valve line-up of frequency changer, IF amplifier, detector/AGC/AF amplifier, output valve and double diode full wave rectifier. The TRF architecture made a reappearance with the recommencement of television broadcasting after the war, only to be replaced by superhet 'televisors' with the advent of a second channel. Since then, TRF receiver have virtually vanished into history, and the superhet architecture has reigned supreme, except for some very specialized applications. For example, equipment containing a TRF receiver can be telecommanded from a distance, without any danger of the item being discovered by monitoring for radiation from a local oscillator.

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The superhet is susceptible to certain spurious responses, of which the image responses one of the most troublesome. With the 'local oscillator running high', i.e. at $(F_s + n)$, where F_s is the frequency of the wanted signal and n is the intermediate frequency or IF, an unwanted signal at $(F_s + 2n)$, i.e. n above the local oscillator frequency, will also be translated to the IF. If n is a small fraction of F_s , it will be difficult if not impossible to provide selective enough front end tuning, adequately to suppress the level of the image frequency signal reaching the mixer. In the case of an HF communications receiver covering 1.6 to 30 MHz, a commonly employed arrangement is to use a double superhet configuration, with the first IF much higher than 30 MHz. The image frequency is now in the VHF band, and easily prevented from reaching the first mixer.

II. NEW TELEVISION RECEIVERS

Television receivers commonly use an IF in the region of 36 MHz or 44 MHz in the early days when TV signals were in Bands I or III, i.e. at VHF, the image presented no great problem. With the move to the UHF Bands IV and V (470–860 MHz), great care necessary at the design stage to ensure satisfactory operation. An example of the economy which can result from the introduction of new components, concerns the burgeoning multimedia market. Figure .1 shows a block diagram of the front end of a conventional three band single conversion tuner. Three tracking filters as shown are needed to suppress the image, which is only some 80 MHz away from the wanted signal. Figure .2 shows a dual conversion tuner where, due to the high first IF of 1.22 GHz, the image is no longer a problem. This arrangement is possible due to the introduction of highly selective SAW (surface acoustic wave) filters operating at 1.22 GHz. The response of such a filter is shown in Figure 3. Whilst not a fundamentally different receiver architecture it represents a distinct advance in TV receiver design. SAW filters operating at UHF and higher frequencies are available from a number of manufacturers, including mu Rata and Fujitsu in addition to EPCOS.

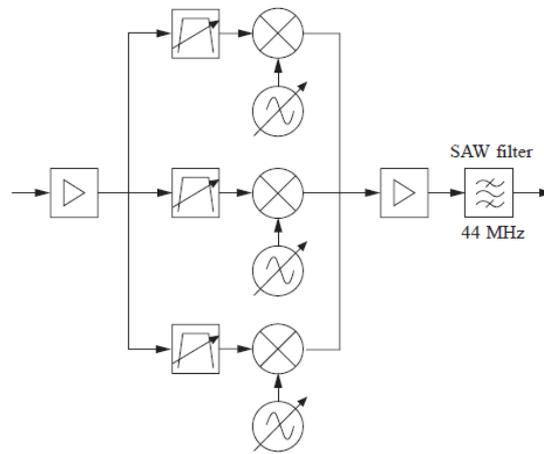


Figure 1: Basic front end block diagram of a conventional three band TV tuner. (Reproduced by courtesy of EPCOS AG)

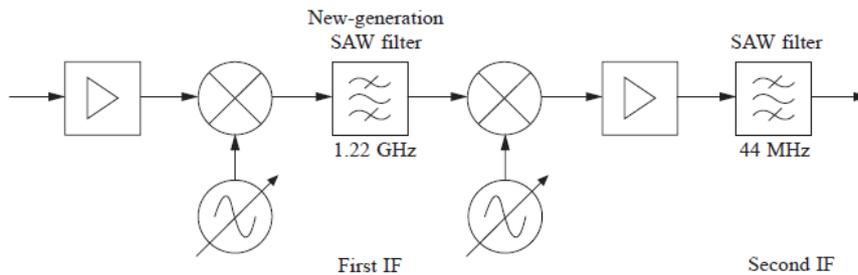


Figure 2 : Basic front end block diagram of a dual conversion tuner

The homodyne receiver gave an example of its use to receive FSK signals. With the local oscillator tuned midway between the tones, each will be translated to precisely the same baseband frequency. It is possible, by using two mixers fed with local oscillator drives in Quadrature, to distinguish between signals in the two channels.

side of the local oscillator frequency n , simultaneously. The upper sideband translates to $F_s\text{-upper} - n$, a positive frequency. In the case of the lower sideband, since n is greater than $F_s\text{-lower}$, the sideband translates to a 'negative frequency'. Thus both the I and the Q channels would contain both lots of information; special processing is then necessary to separate them. A signal which contains both positive and negative frequencies is called a 'complex' signal, as distinct from a 'real' signal. The latter, like the output from a microphone, contains only real frequencies and can consequently be entirely defined by the signal on a single circuit. On the other hand, two distinct circuits or channels are necessary to fully define a complex signal. Figure .4 shows two local oscillator drives to two mixers, where the drive to the lower Q mixer lags that to the upper I mixer by 90° , translating a signal input centered on the LO frequency (or offset from it) to 0 Hz or 'baseband' (or an intermediate frequency). A signal 100 Hz above the LO frequency will translate to baseband as 100 Hz, a positive frequency, whereas a signal 100 Hz below this frequency will translate to baseband as -100 Hz, a negative frequency. Vector diagram Figure .5a shows a positive frequency coming into phase with the Q local oscillator drive 90° before coming into phase with the I LO drive, so for a positive frequency the Q channel

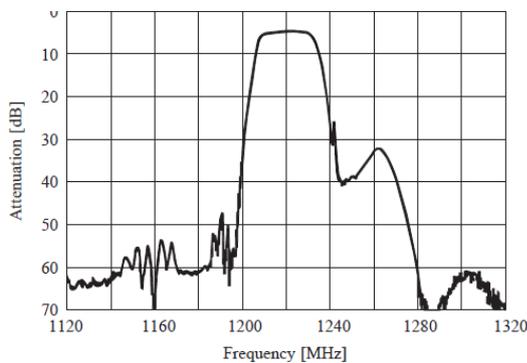


Figure 3 : Attenuation versus frequency of the 1.22 GHz SAW filter used in Figure .2. (Reproduced by courtesy of EPCOS AG)

However, consider a modulation system where there are signal components in both sidebands, each

output leads the I channel by 90°, and vice versa for a negative frequency. (Note that coincident vectors have been offset slightly, for clarity.)

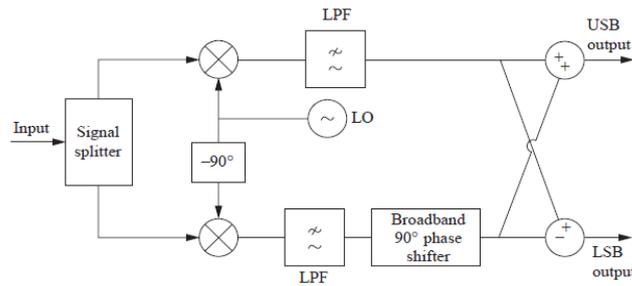


Figure 4 : The arrangement of an image reject mixer, translating the input signal (centered on the same frequency as the local oscillator) to centered on 0 Hz. Where the signal and local oscillator frequencies differ, giving a finite intermediate frequency, the low-pass filters would be replaced by band-pass filters

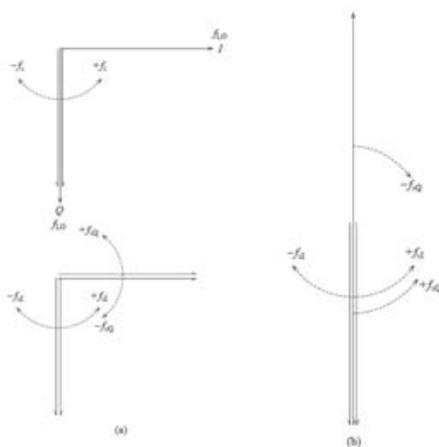


Figure 5 (a) : Showing how, for a positive frequency f_s , the Q channel baseband output leads the I channel by 90°(b) After a 90° phase shift, the components due to $+f_s$ in both channels are in phase, those due to $-f_s$ in anti phase. So summing recovers the upper sideband; differencing, the lower

Figure .5a also shows the phases and phase rotation of the upper and lower sidebands out of the mixers, after translation to baseband.

The baseband signal out of the Q mixer is subsequently passed through a broadband 90° phase shifter, and Figure .5b shows the positions of the Q components coming out of the 90° delay. Each is shown as where the Q components out of the mixer were, one quarter of a cycle earlier. The baseband signal due to the upper sideband is now in phase in both channels, whilst that due to the lower sideband is in anti phase. So if the two channels are added, the lower sideband contribution will cancel out leaving only the signal due to the upper sideband, whilst conversely, differencing the I and Q channel will provide just the lower sideband signal. This arrangement is known as an image reject mixer (Figure.4). The baseband 90° phase-shifter (or ‘Hilbert transformer’) should cover the baseband of interest –outside this band the out-phasing

no longer holds so sideband separation would not be complete. Such a receiver would be capable of receiving ISB (independent sideband) signals, where one suppressed carrier is modulated with two separate 300– 2700 Hz voice channels, one on each sideband.

III. POLY PHASE FILTER

In practice, due to limitations in mixer and channel balance and accuracy of the quadrature phase shifts, the rejection of the unwanted sideband is often limited to about 35–40 dB. Since, generally, each sideband will be received at much the same level; this would be adequate for ISB wireless telephony use. The image reject mixer can also be used for the reception of analog FM signals such as NBFM (narrow band FM) voice traffic [1]. An alternative to the arrangement of Figure .4 is shown in Figure .6. Here, a poly phase filter is used in place of low pass filters and Hilbert transformer. The poly phase filter is a network which has a pass band to positive frequencies and a stop band to negative frequencies, so combining the roles of the two filters and the broadband 90° phase shifter of Figure .4. Poly phase filters provide a band-pass response, and can be used in low IF architecture receivers, where the data bandwidth is significant compared with the centre frequency. They have the advantage that the frequency response is symmetrical, avoiding ISI (inter-symbol interference). They may be realized as entirely passive networks [2], or active networks [3, 4]. The operation of poly phase filters is described in [5].



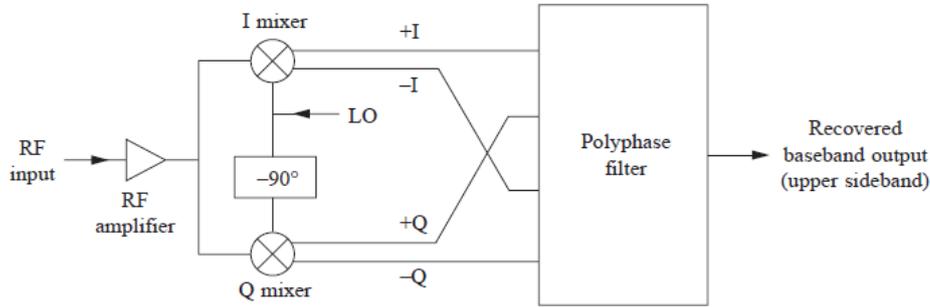


Figure 6 : A poly phase filter combines the functions of the two low-pass filters and the Hilbert transformer of Figure 4

IV. IMAGE REJECTION MIXER

An image reject mixer may be used either at the incoming signal frequency direct, or as the final IF stage in a superhet. However, an image reject mixer is often of limited use as the first mixer in a superhet, due to the limited degree of available image rejection mentioned above. But it can be useful to provide extra image rejection where there is some front end tuning, but which is not quite selective enough on its own. The I and Q signals can be digitized in ADCs (analogue to digital converters) and subsequently processed in digital form, bringing us to the realm of modern architecture. A typical arrangement is shown in Figure .7. Many variations are possible upon this basic scheme. Thus Figure .7 shows a single superhet, but the RF amplifier (if fitted) might be followed by a first mixer, first IF band-pass filter and first IF amplifier, ahead of the I and Q

mixers, implementing a double superhet. The local oscillator might be chosen to translate the signal to a zero IF, i.e. direct to baseband, or might be offset slightly, so as to use a low 'near zero' IF. This avoids some of the problems, described below, that can occur with image reject mixers. The ADC sampling rate may be greater than twice the highest frequency component applied to it, meeting the Nyquist sampling criterion. Alternatively, with a high IF, having a small percentage bandwidth, the ADC may be run at a much lower frequency, one of its harmonics being centered in the IF band. It thus subsamples the IF signal, but aliasing does not occur provided the signal bandwidth on either side of the harmonic does not reach out as far as half way to the adjacent harmonics of the sampling frequency. Any of the architectures described may be used with the signal direction reversed, as a transmitter.

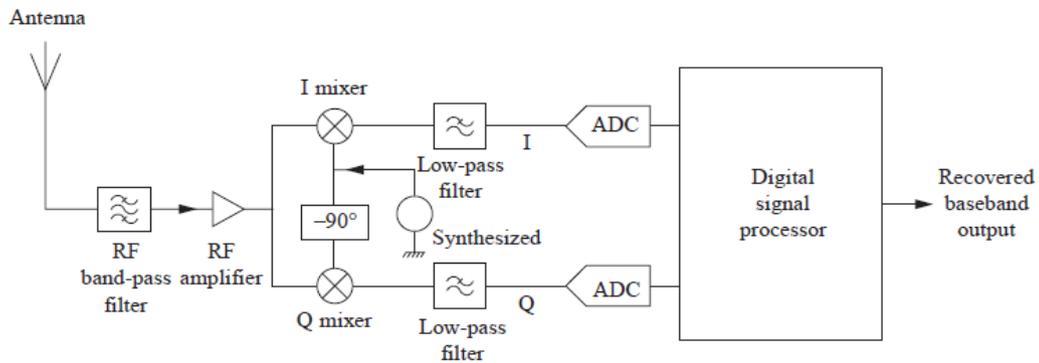


Figure 7 : Block diagram of a digital receiver, using an image reject mixer followed by digital signal processing

The image reject mixer suffers from limitations such as dc offsets and gain differences in the two channels, and imperfect quadrature between them. One of the advantages of digitizing the two mixer outputs is that it may be possible to correct for quadrature, gain and offset errors, resulting in greatly enhanced rejection, at the expense of a greater workload for the DSP (digital signal processor). For many non-deterministic signals such as digitized speech, there is no dc component,

and the long term average levels expected in the I and Q channels are equal. Two digital integrators with a long time constant can thus be used in a negative feedback loop to apply a correcting offset to each channel, to drive the long term average to zero. Similarly, a gain adjustment can be applied to one channel, to drive the long term average level to equal that in the other channel. Finally, if there is no quadrature error (i.e. the two channels are truly orthogonal), the long term average

of the product of the two channels should be zero. So another servo loop, including multiplier and a long term integrator, can be arranged to add or subtract a small fraction of one channel to/from the other, driving the quadrature error to zero. Thus the signals applied to the sum and difference stages are fully corrected.

The explosive growth of the mobile phone market has been built upon a carefully organized frequency- and power-control plan. Various architectures are used by different manufacturers, but all depend upon the way communications between base station and mobile are organized. In particular, in the GSM system, used in Europe and many other countries (but not in the USA or Japan), the frequency band is split, into base station to-mobile links at one end, and mobile-to-base station at the other. On initiating a call, the mobile receiver scans the base station band looking for the nearest (strongest signal) base station. It then calls the base station on a channel marked as free, starting at low power and notching up until communication is achieved. Thereafter, the mobile transmit at the level dictated to it by the base station. In this way, at the base station, more distant mobiles are not blotted out by nearer mobiles, and due to the split band arrangement, image signals do not interfere with reception at the mobile. This scheme only works if the mobile's power output is accurately controlled, for which purpose ICs providing accurate true rms level sensing are available, from Analog Devices and other manufacturers. DECT (variously described as Digitally Enhanced Cordless Telephony, Digital European Cordless Telephone or Cordless III) operates rather differently, with ten 1.78 MHz wide channels in the 1.88 to 1.9 GHz band.

It uses alternate 5 ms time slots for two way communication between the base unit and one or more handsets, and thus uses both FDMA and TDMA (frequency division multiple access and time division multiple access). Each 5 ms period is further divided into 12 time slots, and each connection needs a time slot in each 5 ms period. Thus the system has 120 available channels, and when powered up, each unit scans the range of frequencies and time slices, preparing a table of 120 RSSI (received signal strength indication) figures. A free channel is chosen for communication, and furthermore, scanning continues during operation, to provide a seamless handover to another frequency or time slot if interference is encountered. Whilst most receivers at the present time are of the superhet variety, much activity is aimed at producing chip sets for GSM (now known as Global System Mobile, but originally the 'Groupe Speciale Mobile'), the alternative DCS/PCS systems, and DECT receivers, using the direct conversion architecture, i.e. operating as homodynes. However, for some specialized applications the TRF architecture may be making a come-back, despite the difficulty of achieving

sufficient gain at the signal frequency, without instability due to unintentional feedback from output to input. Ref. [6] describes a system known as ASH – amplifier-sequenced hybrid. Here, front end selectivity is provided by a SAW filter, the signal then passing through two amplifiers, separated by a SAW delay line. The first amplifier typically provides a gain of 50 dB, the second 30 dB. Despite the design being aimed at implementation at a frequency in the range 300 MHz to 1 GHz, instability is avoided by powering up the amplifiers alternately. Thus whilst the first amplifier is active, the second is off, and the second receives the resultant signal, via the SAW delay line, during its on-period, i.e. the off-period of the first amplifier. Sensitivity is claimed as -102 dBm at a 2.4 kps data rate, and the module doubles, as needed, as a transmitter on the same frequency, with an output of 0 dBm.

V. CONCLUSION

The advanced architectures of different receivers like super heterodyne including IF (intermediate frequency) signal processing techniques in super heterodyne receivers have been clearly explained.

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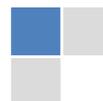
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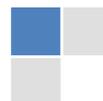


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<i>References</i>	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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