Online ISSN : 2249-4596 Print ISSN : 0975-5861 DOI : 10.17406/GJRE

Global Journal

OF RESEARCHES IN ENGINEERING: F

Electrical and Electronic Engineering

SINR and Outage Analysise

GateElectrodeWorkFunction

Solar Power Charge Controller

Highlights

Effect of Gate Insulator Thickness

Discovering Thoughts, Inventing Future

VOLUME 16 ISSUE 8 VERSION 1.0

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GLOBAL JOURNAL OF RESEARCHES IN ENGINEERING: F Electrical and Electronics Engineering

GLOBAL JOURNAL OF RESEARCHES IN ENGINEERING: F Electrical and Electronics Engineering

Volume 16 Issue 8 (Ver. 1.0)

Open Association of Research Society

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GLOBAL JOURNAL OF RESEARCHES IN ENGINEERING: F ELECTRICAL AND ELECTRONICS ENGINEERING Volume 16 Issue 8 Version 1.0 Year 2016 Type: Double Blind Peer Reviewed International Research Journal Publisher: Global Journals Inc. (USA) Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Simulation based Characterization of the Transport Channel Parameters of Pentacene Thin Film Transistor: Effect of Gate Insulator Thickness and Gate Electrode Work Function

By W. Wondmagegn & R. J. Pieper

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Abstract- In this paper we have presented the simulation and analysis of the channel field, potential, mobility, hole concentration, and the threshold voltage of pentacene thin film transistor with gate metal work function and gate insulator thickness. The top contact transistor from pentacene active material, paryelene dielectric and gold source/drain electrodes, has been used for our simulation. The simulations have been performed using Silvaco's Atlas device simulator. The Poole-Frenkel transport model was used in the pentacene active material. The results of the simulation have shown an impact of the gate metal work function on threshold voltage, channel potential, channel charge concentration, channel field, and mobility of the device.

Keywords: pentacene; simulation; organic thinfilm transistor; Poole-Frenkel mechanism; threshold voltage; gate-electrode; workfunction.

GJRE-F Classification: FOR Code: 091599, 090699



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Simulation based Characterization of the Transport Channel Parameters of Pentacene Thin Film Transistor: Effect of Gate Insulator Thickness and Gate Electrode Work Function W. Wondmagen " & R. J. Pieper "

Abstract- In this paper we have presented the simulation and analysis of the channel field, potential, mobility, hole concentration, and the threshold voltage of pentacene thin film transistor with gate metal work function and gate insulator thickness. The top contact transistor from pentacene active material, paryelene dielectric and gold source/drain electrodes, has been used for our simulation. The simulations have been performed using Silvaco's Atlas device simulator. The Poole-Frenkel transport model was used in the pentacene active material. The results of the simulation have shown an impact of the gate metal work function on threshold voltage, channel potential, channel charge concentration, channel field, and mobility of the device. When the high work function gate electrode is used, there exists a built in field in the transistor channel. As a result there exists built in channel charge concentration at zero gate voltage and increased channel mobility is observed. As expected, when the gate insulator thickness decreases, the channel charge density increases due to increased vertical field and this increases the drain current. The field effect mobility decreases as the thickness of the dielectric decreases. The threshold voltage changes with gate electrode work function but remains the same when the thickness of the dielectric changes.

Keywords: pentacene; simulation; organic thinfilm transistor; Poole-Frenkel mechanism; threshold voltage; gate-electrode; workfunction.

I. INTRODUCTION

Pentacene Field Effect Transistors (FETs) have been attractive for applications in the areas of Flexible display, RFIDs, sensors because its performances are similar to that of amorphous silicon thin film transistors [1-5]. Apart from these comparable electronic characteristics and promising low-cost fabrication, there are still important parameters of the device that needs better understanding and precise control for proper operation of the device. Some of the key issues are environmental stability, leakage current, threshold voltage and mobility [6-12]. In general organic FETs have higher threshold voltages than normally required for integrated circuit applications. The threshold voltage can depend on different factors such as gate bias stress [13,14], gate dielectric [15], and the thickness of the active layer material [16]. Properties of gate electrode and dielectric are also important parameters that affect the performance of the transistor. The dependence of threshold voltage on gate metal work function has also been reported [17,18]. In this paper we have simulated a top contact transistor and systematically studied the effect of gate work function and gate insulator thickness on channel parameters such as field, potential, charge concentration, threshold voltage, and field effect mobility.

II. SIMULATION

Bottom contact pentacene Thin Film transistor is simulated and matched with experimental data, previously reported by our group [19-21]. Poole-Frenkellike electric-field dependence (equation below), which is the inverse variation in activation energy against the square root of electric-field strength [22,23], has been employed for pentacene active channel. Nonlinear transport organic semiconductor materials is intensively (PF) explained through Poole-Frenkel transport mechanism [24-27]. The model explains the temperature and electric-field dependencies of charge carrier drift mobilities in disordered materials.

$$\mu(E) = \mu_0 \exp\left[-\frac{\Delta}{kT} + (\frac{\beta}{kT} - \gamma)\sqrt{E}\right]$$

where $\mu(E)$ is the field dependent mobility, $\mu 0$ is the zero field mobility, E is the electric field, Δ is the zero field activation energy, β is the electron Poole-Frenkel factor, k is the Boltzmann's constant, and T is the temperature. The Poole-Frenkel parameters extracted from the best match between simulation and experiment are Δ =0.1, β =3.58x10-5, and γ =10-5.

Figure 5 (a) shows the characteristic family of curves of pentacene TFT for gate voltages 5 – 20 volts in

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steps of 5 V. Figure 5 (b) shows transfer curves for experiment and simulations.



Fig. 1: ID -VD plots of the transistor (a); ID -VG plots of the transistor (b)

III. Transistor Channel Parameter Simulation Results and Discussion

A top contact device (Fig. 2) with a width of 100 μm and channel length of 10 μm is used for simulation.

A 30 nm pentacene active layer and a 6 nm gate dielectric is used. The thickness of gold source drain contacts is 30 nm and that of aluminum gate electrode is 20 nm



Fig. 2: Top contact device structure (not drawn to scale)

a) Impact of gate electrode work function

Fig. 3 shows drain current versus gate voltage characteristics of the device for different gate electrode work functions simulated at a drain voltage of-3 V.





The current increases as the work function increases which implies that there is a change in the transport channel parameters of the transistor such as the channel field and charge concentration.

The change in threshold voltage associated with change in electrode work function and change in the flat band voltage is also expected. With no charge present in the oxide or at the oxide-semiconductor interface, the flat-band voltage simply accounts for the work function difference between the semiconductor and the metal gate. As has been reported [28], the effect of gate work function is significant, particularly when the transistor is biased at accumulation. The gate work function can affect both the gate leakage current and the source drain current. As shown in Fig.3, the current increases by about a factor of 3 when the gate metal work function increases from 3.8 eV to 5.4 eV.





To account for this change in drain current as a function of gate metal work function, we have extracted the threshold voltage for each gate work function. The threshold voltage was extracted from the square-root of the drain current versus gate voltage curve. Fig. 4 represents the relationship between the threshold voltage of the transistor, extracted from the simulated transfer curve, and the work functions of the gate electrode. The simulations show a linear relationship between the threshold voltage and workfunction which is consistent with the relationship mentioned in the literature [17]. The gate electrode work function is one of the factors which affect the threshold voltage. The threshold voltage decreases as the work function of the gate electrode increases towards the HOMO level of pentacene. Matching the gate electrode and pentacene work functions would reduce the threshold voltage.

The effect of the work function on the electric field, which is responsible for the channel charge

accumulation, has also been examined. We probed the electric field at the interface between the gate insulator and pentacene for fixed drain voltage (-3 V). The change in the flat band voltage or the threshold voltage is also reflected in a change on the channel electric field and

channel charge concentration. As shown in Fig. 5, simulation results indicate that there exists a built in field at zero gate voltage. For each gate voltage, higher work function gate electrodes create higher channel field.



Fig. 5: Plot of extracted channel field against gate voltage for different gate electrode work functions

This field forms a channel charge at zero applied gate voltage as shown in the Fig. 6. The simulation shows about 1018 cm -2 charge concentration at zero gate voltage for 5.4 eV work function as opposed to about zero for 3.8 eV work

functions. This implies that the increase seen in the drain current, as an increase in gate work function, resulted from both the field increase and threshold voltage reduction.



Fig. 6: Plot of extracted channel charge concentration versus gate voltage for different gate electrode work functions

We have extracted the mobility for different work functions and presented in Fig. 7. The channel mobility is also higher for higher work functions. For lower work function gate electrodes, the mobility starts at very low value at zero gate voltage and increases with gate voltage. But for the higher work function electrodes, the mobility has a higher value at zero gate voltage. This is the result of the high electric field and charge density. Experimental studies in the literature indicate that channel mobility increases when the channel field and charge concentration increases [29].



Fig. 7: Channel mobility vs gate voltage for different gate electrode work functions

To study the variation of the channel parameters the channel from the source to the drain, we have extracted the channel potential at -3V gate and drain voltages at different points along the channel. From the potential plots (Fig. 8), we can observe two important observations such as the voltage drop at the interface between the source drain electrodes and the polymer; and the nonlinearity of the channel potential. The voltage drop between the interface electrode and the semiconductor indicates a contact resistance due to different work functions plus the bulk



Fig. 8: Channel potential at different positions along the channel from source to drain for different gate electrode work functions

resistance of pentacene between the channel and the electrode [30]. This is attributed to low mobility or depletion near the contacts and Schottky barriers at the contacts [31,32]. The potential profiles are clearly nonlinear as seen in the figure. The nonlinearity of the potential profile is more pronounced near the drain electrode than near the source. This is due to the fact that the relative decrease of the induced charge density in the accumulation layer when going from source to drain as well as an associated decrease of the field effect mobility [33]. In going from the source (x=0) to the drain (x=12) along the channel, the potential drops fast for higher gate electrode work function. This faster drop of potential gradient is associated with the higher channel electric field we have observed at higher gate electrode work functions.

b) Impact of gate dielectric thickness

In addition to studying the impact of the work function on the channel properties, we have simulated devices at different gate insulator thicknesses to study its effect on channel field, channel charge concentration, threshold voltage, and channel charge mobility. As shown in Fig. 9 a, the field increases as the thickness of the dielectric decreases and this increase in field increases the charge accumulation in the channel (Fig. 9 b). However we haven't seen variation of the threshold voltage with thickness of the dielectric. This is because there is no variation of the flat band voltage, interface traps and charges as a function of the dielectric thickness. Fixed charge in the dielectric has not been included in our simulation model.



Fig. 9: a) Electric field (a) and Channel charge concentration (b) probed at insulator/pentacene interface at different gate electrodes but same gate voltage (-3 V)

The change in the thickness of the dielectric has also brought the change in the channel field effect mobility. Fig. 10 shows that the mobility variation with gate voltage and thickness of the dielectric. The mobility increases as a function of electric field only up to a little over the threshold voltage. After the channel is fully formed, the mobility starts to drop as the gate voltage increases to a more negative value. The drop is significant for lower dielectric thicknesses. Increasing the gate voltage increases both the electric field and the channel charge concentration.



Fig. 10: Channel mobility vs gate voltage for different gate dielectric thicknesses

We have also shown this by simulating the device at a gate voltage of -3 V and dielectric thickness of 6 nm for various values of dielectric constant. The extracted mobility versus channel charge density is shown in Fig. 11. The figure shows an increase of mobility with channel charge density. So the decrease in mobility we observed in Fig. 10 at more negative gate voltages, with the decrease in dielectric thickness, should be from the high electric field strength. This is because the lower the dielectric thickness the higher the field and the higher the impact on mobility.

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Simulation Based Characterization of the Transport Channel Parameters of Pentacene Thin Film Transistor: Effect of Gate Insulator Thickness and Gate Electrode Work Function





IV. Conclusion

In summary, our simulation results show an impact of the gate metal work function and the gate dielectric thickness on channel field, channel potential, channel charge concentration, and mobility of the device. When the high work function gate electrode is used, there exists a built in field in the transistor channel. As the result there exist built in channel charge concentration and increased channel mobility at zero gate voltage. As expected, when the gate insulator thickness decreases the vertical electric field and the channel charge density increases. This increase in field and charge concentration slightly increases the mobility and the drain current. The field effect mobility decreases as the thickness of the dielectric decreases. The threshold voltage changes with gate electrode work function but remains the same when the thickness of the dielectric changes. The threshold voltage has changed from -1.3 V to -0.07 V by changing the work function from 3.8 eV to 5.4 eV. We also have seen a potential drop at the electrode/polymer interface and a nonlinear decrease in potential from source to drain.

V. Acknowledgments

We gratefully acknowledge DOD for support of this work. We also wish to thank the fabrication group at UTD for provided stimulating discussions which motivated this study.

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GLOBAL JOURNAL OF RESEARCHES IN ENGINEERING: F ELECTRICAL AND ELECTRONICS ENGINEERING Volume 16 Issue 8 Version 1.0 Year 2016 Type: Double Blind Peer Reviewed International Research Journal Publisher: Global Journals Inc. (USA) Online ISSN: 2249-4596 & Print ISSN: 0975-5861

SINR and Outage Analysis for the Jt Comp Technique based Downlink Lte -A Multi-Cell Cellular Networks with Hexagonal Layout

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Abstract- Now-a-days a multi-cell cellular network has drawn broad attention for data rate due to continuously increasing user populations using wireless service. That's why, recent researches focus on the concept of joint transmission coordinated multi-point (CoMP) transmission which can provide high spectral efficiency for cellular systems. The performance of the Joint Transmission Coordinated Multipoint technique has been analyzed on the basis of signal-to-interference-noise ratio and outage probability variation with both minimum acceptable signal quality and cell radius. In this paper the results are compared with the performance of traditional techniques without coordinated multipoint and obvious improvement has been observed.

Keywords: LTE-A; cellular network; path-loss; SINR; SINRth; CDF; comp; JT comp; outage probability.

GJRE-F Classification: FOR Code: 090699



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Keywords: LTE-A; cellular network; path-loss; SINR; SINRth; CDF; comp; JT comp; outage probability.

Ι. INTRODUCTION

TE-A is the most popular 4G cellular network standard, which is continuously evolving to meet the expectations of the visionary 5G networks., has been brought the high speed wireless technology for mobile users[1]. It is a major advancement of LTE which targets higher data rate, higher spectral efficiency, less latency, two times higher cell edge user throughput, three times higher average throughput than LTE [2]. Coordinated multipoint (CoMP) is new technique for LTE-A where a User Equipment (UE) receives signal from more than one base station and hereby signal quality and fidelity increases. Joint Transmission (JT) is a special kind of CoMP where a UE receives signals from two base stations and interferences from the others [3]. It potentially eschews co-channel interference due to its implicit feature. In this paper, performance of JT CoMP is simulated and compared in terms of SINR (signal-to-

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interference-noise ratio), CDF (Cumulative Density Function) and outage probability. In Section II and III, CoMP technique has been discussed in general. In section IV, the proposed technique has been stated. The simulation procedure and the result analysis are in section V.

II. The Coordinated Multipoint (COMP TECHNIQUE)

In case of CoMP technique shown in Fig. 1 when a UE is in the cell-edge region, it may be able to receive signals from multiple base stations and the UE's transmission may be received at multiple base stations regardless of the system load [4]. If the signal transmitted from the multiple base stations is coordinated, the downlink performance can be increased significantly. This coordination can be simple as the techniques that focus on interference avoidance or more complex as in the case where the same data is transmitted from multiple cell sites. For the uplink, since the signal can be received by multiple base stations, if the scheduling is coordinated from the different base stations, the system can take advantage of this multiple reception to significantly improve the link performance [5].



Fig. 1: LTE Advanced Coordinated Multipoint.

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III. THE JT COMP TECHNIQUE

In Joint Transmission CoMP, a UE receives signal from the cell where it is located and also from the cell closest to it. All other base stations in the adjacent cell are considered as interferences. In order to turn inter-cell interference into a useful signal the JT-CoMP can be used as a MIMO (Multiple Input Multiple Output) approach so that it can transmit the same information to individual UEs located at the cell edge [7] where the received power can be very low. It can improve the spectrum efficiency by avoiding the co-channel interferences and increase the overall throughput [3]. In Fig. 2, base stations (BS-1 and BS-2) coordinate the transmission to user equipments (UE-1 and UE-2).

BS---base station UE---User Equipment



Fig. 2: Joint Transmission CoMP concept.

IV. System Model

A downlink multi-cell cellular network deployed using regular hexagonal cell layout is shown in Fig. 3. Before starting the analysis, some parameters are assumed such as base station, antenna height, transmitted power, channel bandwidth, path-loss model, fading, thermal noise power and interference.



Fig. 3: LTE-A cellular network using regular hexagonal cell.

a) Ue Distribution

100 users are randomly distributed within the cell considering the radius (r) from the center (base station) and the azimuth (θ) as uniform random variable. Here, r is considered as uniform in the interval [0, radius of the cell] and θ in the interval $[0, 2\pi]$. The user distribution is illustrated in Fig. 4.



Fig. 4: UE and base station distribution.

b) Base Station Setup

All the base stations are set up at the center of each cell which has also been illustrated in Fig. 4.

V. Simulation and Result

The simulation has been performed on a MATLAB based Monte-Carlo simulation platform. A central cell and 2-tiers of its adjacent cells are implemented. Users' equipment (UE) in only central cell is considered.

a) Path Loss Model

Path loss models describe the signal attenuation between a transmitting and a receiving antenna as a function of the propagation distance and other parameters. It has been calculated using the *WINNER* + model for urban and rural area. Here, for shadowing (large scale fading) with standard deviation, $\sigma = 8db$ the path loss in urban and rural area is described respectively by the following equations: For urban area:

Path loss(in dB)

$$= (44.9 - 6.55 \log_{10}(h_{BS})) \log_{10}(d) + 5.83 \log_{10}(h_{BS}) + 14.78 + 34.97 \log_{10}(f_c)$$

For rural area:

Path loss (in dB)

$$= 25.1 \log_{10}(d) + 55.4 - 0.13(h_{BS} - 25) \log_{10}\left(\frac{d}{100}\right) - 0.9(h_{MS} - 1.5) + 21.3 \log_{10}(f_c/5)$$

Here, *d* is the distance of a UE from any base station in kilometer, h_{BS} is the base station antenna height in meter and f_c is the carrier frequency in gigahertz.

b) SINR and Outage Probability Calculation

The SINR is the ratio of received power to the sum of interference power and noise power. The Outage probability has been calculated taking different SINR values as threshold. Also, outage probability for various cell radiuses has been computed and plotted to compare with case of non-coordinated multipoint scheme. Instead of simulating 1000 times with 100 UE at the central cell, it has been simulated once with 100000 randomly distributed UEs exploiting the ergodic nature of this random process.

c) Comparison With No-Comp

The SINR for Joint Transmission Coordinated Multipoint (JT-CoMP) scheme is right-shifted than the SINR of No-CoMP scheme. That means higher SINRs are more probable in JT-CoMP which is illustrated in Fig.5 for urban and in Fig.6 for rural area.



Fig. 5: CDF of SINR for Urban Region.



Fig. 6: CDF of SINR for Rural Region.

The improvement can also be seen in the graphs of outage probability. Here, also the curve for JT CoMP is right shifted than the curve for No-CoMP scheme which means compared to the No-CoMP schemes outage (call drop etc.) happens if we consider higher quality signals as threshold statistically which is shown in Fig.7 for urban and in Fig. 8 for rural cases.



Fig. 7: Outage Probability Vs. threshold SINR for Urban Region.

Outage Probability Vs. Threshold SINR



Fig. 8: Outage Probability Vs. threshold SINR for Rural Region.

The difference has also been clear in the outage probability vs radius curve considering fixed threshold 0db which is illustrated in Fig.9 for urban and in Fig.10 for rural area.



Fig. 9: Outage Probability Vs. cell radius for Urban Region.



Fig. 10: Outage Probability Vs. cell radius for Urban Region.

VI. Conclusion

In this paper, the performance of Joint Transmission Coordinated Multipoint is analyzed using MATLAB and the performance evaluation shows how the CDF and outage probability varies with SINR and cell radius respectively. It also shows that the performance of JT CoMP is obviously better than the traditional techniques in all the aspects analyzed.

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GLOBAL JOURNAL OF RESEARCHES IN ENGINEERING: F ELECTRICAL AND ELECTRONICS ENGINEERING Volume 16 Issue 8 Version 1.0 Year 2016 Type: Double Blind Peer Reviewed International Research Journal Publisher: Global Journals Inc. (USA) Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Solar Power Charge Controller

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Abstract- The demand of renewable energy (alternative energy sources) is increasing day by day as our non renewable sources have started depleting. The other reason for increased demand is that it has a cleaner, easy setup and has a very low cost of maintenance during its operation. Due to which, solar powered equipments and appliances are making its way into various sectors of our day to day life. This research paper deals with the scenario that a storage or battery is needed in order to harness the solar energy when the sunlight is available and supply it in vice versa conditions. For this, a cost effective system is built which charges a battery with the help of solar panel and protection is given to the battery in case of overcharge, deep discharge and under voltage condition. The block diagram, circuit diagram, hardware design are discussed in the paper.

Keywords: solar panel, battery, transistors, Im-324, op-amps, load.

GJRE-F Classification: FOR Code: 850505



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I. INTRODUCTION

Solar Power Charge Controller can be used in various sectors. For instance, it can be used in solar home system, Hybrid systems, solar water pump system etc. In this, a solar panel converts sunlight energy into electrical energy through an electrochemical process also know as photovoltaic process. Energy is stored in the battery with the help of solar panel through a diode and a fuse. Energy stored in the battery can be used when there is no sunlight as during discharge, chemical energy is converted into electrical energy

SOLAR PANEL

which in turn illuminates electrical appliances or helps in pumping water from the ground [1]. Hence, it is needed to protect battery form overcharge, deep discharging mode while dc loads are used or in under voltage as it is the main component in a solar power charge controller. [2]

In this project, indications are provided by a red LED for fully charged battery while a green LED indicates that battery is charging. White LED is provided in order to indicate overcharge, deep discharge or under voltage condition. Charge controller also uses MOSFET as power semiconductor switch to ensure cut off the load in low battery or overload condition. When the battery gets fully charged, a transistor is used in order to bypass the solar energy to a dummy load which protects the battery from getting over charged.

A solar charge controller or regulator is a small box placed between a solar panel and a battery consisting of solid state circuits PCB. They are used to regulate the amount of charge coming from the solar panel in order to protect the battery from getting overcharged. Adding to this, it can also be used to allow different dc loads and supply appropriate voltage. [2]

II. BLOCK DIAGRAM

In figure 1, the basic arrangement of the implemented project can be found.

LOAD SWITCH



SETTING

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CHARGING SWITCH

a) Components Used

The main components used in order to establish the project are Photovoltaic Cells and Solar panel, battery, LM 324 and Transistors.

i. Photovoltaic Cells and Solar panel

Photovoltaic (PV) cells are the one which are made from special materials called semiconductors like Silicon. They are used for conversion of light into electricity using semiconductor materials that exhibit the photovoltaic effect. When the light strikes the cell, certain amount of light gets absorbed into the semiconductor material which triggers the flow of electrons that causes current to flow. We can place metal contacts on top and bottom of the cell, from which we can draw current externally.

Solar panel is a panel designed to absorb sun's rays in order to generate electricity or heat. A PV module is a packaged consisting of solar cells. Solar panels constitute the solar array of a PV system that helps in generating and supplying electricity to commercial and residential sectors. Following are the advantages of solar panels-

- These are the equipments that can covert solar energy into electrical energy directly, easily and efficiently.
- They can easily last for 25 years and does not require much operational maintenance. [4]





ii. Battery

In this project a Sealed Rechargeable Battery (6V4.5AH/20HR) is used in order to store energy. An Electrical battery converts chemical energy directly into electrical energy comprising of one or more electro chemical cells. The battery comes in all shapes and sizes and can be used for household, robotics, industrial applications etc. For example, miniature (small) cells can be used to power devices such as

hearing aids, wristwatches etc. whereas as large batteries can be used telephone exchanges, computer data centres, power substations etc. A 12V, lead-acid battery has 6 cells. The range is 0.1C rate, where C is the battery capacity in Ah in order to charge lead acid batteries safely. The major disadvantage of overcharging a battery is that it can cause reduction in its life span. [3][9]



Figure 3: Sealed Rechargeable Battery (6V4.5AH)

iii. LM 324

It is a general purpose op-amp consisting of four independent, high-gain, internally compensated operational amplifiers designed to operate from a single power supply over wide range of voltages. It has a wide range of applications such as in transducer amplifiers, DC gain Blocks and Conventional op-amp circuits. Opamps in LM 324 are used as comparators in this project. [6]



Figure 4: Pin Diagram



Figure 5: Schematic Diagram

iv. Transistors

There are three types of transistors used in this project.

- SL 100

It is a general purpose, medium power NPN transistor and is commonly used as a switch in common emitter configuration. The transistor terminal requires a fixed DC voltage in order to operate in a desired region of its characteristic curves. It is known as biasing and is used for switching applications. Biasing is done in such a way that it will remain fully on if there is a signal at its base otherwise not. The emitter can be recognized as it will be projecting out. The base is nearest to emitter while collector is far away in the casing. [5]





Figure 6: SL 100

In Figure 6 (b): C, B and E indicates collector, base and emitter.

BC 547

It is an NPN bi-polar junction transistor. A transistor means transfer of resistance which is used to

amplify current. In BC547, its base having small current controls larger current at emitter and collector terminals. [7]



Figure 7: BC 547

- IRF 630

It is an N-type power MOSFET. It can be used in high current switching, uninterruptible power supply

(UPS), DC-DC converters for telecom, industrial and lighting equipment etc. [8]



Figure 8: IRF 630

In Figure 8 (b): D, G and S represents Drain, Gate and Source.

b) Quantities of components used

Table 1	
Major Components Used	Quantity
Solar Panel	1
Battery (6V4.5AH/20HR)	1
LM 324	1
Transistors	3
LEDs	3
Slide Switch	2
PCB Connector 2-PIN	2
Diodes- IN 4007	3
Diodes- IN 4148	6
DC Fan (12V)	1

c) Voltage at IC Pins

Table 2

Integrated Chip (IC)	Pin (No.)	Voltages at Pin Without IC (Voltage)	Voltages at Pin With IC (Voltage)
LM 324	1	0	3.2
(Operational	2	2	1.9
Amplifier)	5	2	1.9
	8	0	3.2
	14	0	5



Figure 9: Voltages at IC Pins without IC (PCB)

Source: - http://www.edgefxkits.com/



Figure 10: Voltages at IC Pin with IC (PCB)

Source: - http://www.edgefxkits.com/

III. Schematic Diagram





a) Connections

A solar panel is used in a solar charging circuit. In this project, the base of SL 100 (power transistor) is connected to the emitter of the transistor (BC 547), collector is connected to the +VE terminal and emitter is connected to GND. Transistor (SL 100), battery (6V) and a transistor (BC 547) are connected parallel to each other. The collector of BC 547 is connected to +VE terminal through R1 of resistance 18K and the emitter is connected to GND through R2 of resistance 82K. The base of BC 547 is connected to the Pin no. 1 of LM 324 through R3 of resistance 100K. Pin no. 4 is connected to +VE terminal and 11th is connected to GND for all four op-amps U1: A and U1: B. 2nd Pin of U1: A is connected to Pin 1 of op-amp through two resistors R4 of 330K and R5 of 330k. Pin 3 of U1: A and Pin 5 of U1: B are shorted and connected to POT of 5K. 6th Pin of U1: B is

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connected to GND through resistor R10 of 120K. 7th Pin of U1: B is an O/P pin connected to Led Green and Red through R7 of 1K and R15 of 2K respectively. . VI: C is also an op-amp whose 10th Pin is connected to POT of 5K of which one of the terminal is connected to 2nd Pin of U1:A whereas 9th Pin is connected to GND. 8th Pin of U1: C is an O/P Pin which is connected to Gate of MOSFET Q2 through Diode IN4148. Along with this, 9th Pin of U1: C is also connected to drain of MOSFET whose gate is also connected to POT of RV1 which will also get O/P of U1: D known as Pin 14. 12th Pin and 13th Pin of U1: D is connected to RV5 (22K PRESET) and to 4 diodes in series known as D5, D6, D7, D8 respectively. The Source of U1: D is connected to GND.

b) Working

Step 1

Solar panel section

In this, battery B1 is charged via d10 and fuse. After battery getting fully charged, Q1 conducts from output of the comparator ie Pin 1, resulting in Q2 to conduct and divert the solar power through D11 and Q2. In this way battery is not over charged.

The project uses one IC LM 324 having four opamps used as comparators that is U1: A, B, C, D. U1: A is used for sensing over charging of the battery to be indicated by action of U1: B output fed D1 (Red) and D12 (Green) for indicating battery status. Diodes D5 to D8 all are connected in series and forward biased through R14 and D3. This provides a fixed reference voltage of 0.65*4=2.6v at anode (+) point of D8 which is fed to pin 2 (-) of U1: A through R11, pin 13 of U1: D, pin 6 of U1:B via R9 and pin 10 of U1:C via 5K variable resistor. Solar panel being a current source is used to charge the battery B1 via D10. While the battery is fully charged, the voltage at cathode point of D10 goes up resulting in the set point voltage at pin 3 of U1: A to go up above the reference voltage because of the potential divider formed by R12 of 22K, 5K variable resistor, R13 of 15K goes up.

This results in pin no 1 of U1: A to go high to switch 'ON' the transistor Q1 that places drive voltage to the transistor SL 100 such that the current from solar panel is bypassed via D11 and the transistor's collector and emitter. Simultaneously pin 7 of U1: B also goes high to drive a led D1 indicating battery is being fully charged. While the load is used by the switch operation Q2 usually provides a path to the (-ve) while the (+ve) is connected to the DC (+ve) via the switch in the event of over charge, the reference voltage at Pin 10 results in pin 8 of U1: C going low to remove the drive to the gate through the D4 of the MOSFET Q2 which in turn disconnects the load. In the event of over charge, Q2 voltage across drain and source goes up which results in Pin no 9 going above pin no 10 via R22. In the event of battery voltage falling below minimum voltage is duly sensed by the combination of D3, R6, RV5 and R16 in Pin 12 resulting in Pin 14 going zero to remove the drive to Q2 gate via R20 and RV1. The correct operation of the load in normal condition is indicated by D9 when the MOSFET Q2 conducts.

IV. HARDWARE IMPLEMENTATION

First, the circuit is implemented on the Printed Circuit board (PCB).





Then, all the connections should be done on PCB as discussed above.



Figure 11: Components fitted on the PCB

After this, a solar panel, battery and the load i.e. a fan (12V DC/0.15A) is attached to the PCB.



Figure 12: Solar Power charge Controller Hardware Module

Step 2 Powering the Circuit

The "slide switch on the side of solar panel and battery" is switched "On" due to which, Red LED glows indicating that battery is fully charged.



Figure 13: Powering the circuit

Now, switch "ON" the "second slide switch nearer to the load". After switching both, load will also switch on and the fan will start rotating.

The "Preset 1 nearer to red and green led" is adjusted in this project in order to set the battery charge. A battery while charging is indicated by a glowing "Green" LED.



Figure 14: After switching "On" both switches

- First Test of Protection given to the battery

In order to test overcharge protection, rotate Preset 2 one which is close to white LED and is subjected to deep discharge/overcharge. So, when the preset is rotated, the white LED starts glowing and the fan will stop rotating.



Figure 15: Overcharge/Deep Discharge Protection Test

- Second Protection

Secondly, in order to test under voltage protection, rotate Preset 3 which is second to white LED. After preset is rotated, the white LED will glow and the fan will stop rotating. This will conclude our under voltage test.



Figure 16: Under voltage Protection Test

Finally rotate a Preset 4 closer to the load's PCB Connector 2 PIN. After rotating the preset we will see that the rotating speed of the fan will increase and vice versa will happen when done in opposite direction.

V. Conclusion

In this paper, a solar power charge controller has been discussed effectively i.e. how rechargeable

battery is used to store energy with the help of solar energy through a solar panel and how it can be used in order to supply power when there is no sun. It also includes protection methods for the battery in order to curb problems like overcharging, deep discharge or under voltage which harm the life of a battery. The proposed system used solar PV module as an input and DC load (fan) as an output. Further the project can be enhanced by using microcontroller and GSM modem to communicate the status of the system to a control room via SMS. This system can also be upgraded to control normal UPS, when connected with the solar charger will convert to SOLAR INVERTER/UPS with solar charge as priority. [2]

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The Editorial Board reserves the right to make literary corrections and to make suggestions to improve briefness.

It is vital, that authors take care in submitting a manuscript that is written in simple language and adheres to published guidelines.

Format

Language: The language of publication is UK English. Authors, for whom English is a second language, must have their manuscript efficiently edited by an English-speaking person before submission to make sure that, the English is of high excellence. It is preferable, that manuscripts should be professionally edited.

Standard Usage, Abbreviations, and Units: Spelling and hyphenation should be conventional to The Concise Oxford English Dictionary. Statistics and measurements should at all times be given in figures, e.g. 16 min, except for when the number begins a sentence. When the number does not refer to a unit of measurement it should be spelt in full unless, it is 160 or greater.

Abbreviations supposed to be used carefully. The abbreviated name or expression is supposed to be cited in full at first usage, followed by the conventional abbreviation in parentheses.

Metric SI units are supposed to generally be used excluding where they conflict with current practice or are confusing. For illustration, 1.4 I rather than $1.4 \times 10-3$ m3, or 4 mm somewhat than $4 \times 10-3$ m. Chemical formula and solutions must identify the form used, e.g. anhydrous or hydrated, and the concentration must be in clearly defined units. Common species names should be followed by underlines at the first mention. For following use the generic name should be constricted to a single letter, if it is clear.

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All manuscripts submitted to Global Journals Inc. (US), ought to include:

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Key Words

A major linchpin in research work for the writing research paper is the keyword search, which one will employ to find both library and Internet resources.

One must be persistent and creative in using keywords. An effective keyword search requires a strategy and planning a list of possible keywords and phrases to try.

Search engines for most searches, use Boolean searching, which is somewhat different from Internet searches. The Boolean search uses "operators," words (and, or, not, and near) that enable you to expand or narrow your affords. Tips for research paper while preparing research paper are very helpful guideline of research paper.

Choice of key words is first tool of tips to write research paper. Research paper writing is an art.A few tips for deciding as strategically as possible about keyword search:



- One should start brainstorming lists of possible keywords before even begin searching. Think about the most important concepts related to research work. Ask, "What words would a source have to include to be truly valuable in research paper?" Then consider synonyms for the important words.
- It may take the discovery of only one relevant paper to let steer in the right keyword direction because in most databases, the keywords under which a research paper is abstracted are listed with the paper.
- One should avoid outdated words.

Keywords are the key that opens a door to research work sources. Keyword searching is an art in which researcher's skills are bound to improve with experience and time.

Numerical Methods: Numerical methods used should be clear and, where appropriate, supported by references.

Acknowledgements: Please make these as concise as possible.

References

References follow the Harvard scheme of referencing. References in the text should cite the authors' names followed by the time of their publication, unless there are three or more authors when simply the first author's name is quoted followed by et al. unpublished work has to only be cited where necessary, and only in the text. Copies of references in press in other journals have to be supplied with submitted typescripts. It is necessary that all citations and references be carefully checked before submission, as mistakes or omissions will cause delays.

References to information on the World Wide Web can be given, but only if the information is available without charge to readers on an official site. Wikipedia and Similar websites are not allowed where anyone can change the information. Authors will be asked to make available electronic copies of the cited information for inclusion on the Global Journals Inc. (US) homepage at the judgment of the Editorial Board.

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Tables: Tables should be few in number, cautiously designed, uncrowned, and include only essential data. Each must have an Arabic number, e.g. Table 4, a self-explanatory caption and be on a separate sheet. Vertical lines should not be used.

Figures: Figures are supposed to be submitted as separate files. Always take in a citation in the text for each figure using Arabic numbers, e.g. Fig. 4. Artwork must be submitted online in electronic form by e-mailing them.

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21. Arrangement of information: Each section of the main body should start with an opening sentence and there should be a changeover at the end of the section. Give only valid and powerful arguments to your topic. You may also maintain your arguments with records.

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24. Never copy others' work: Never copy others' work and give it your name because if evaluator has seen it anywhere you will be in trouble.

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26. Go for seminars: Attend seminars if the topic is relevant to your research area. Utilize all your resources.

27. Refresh your mind after intervals: Try to give rest to your mind by listening to soft music or by sleeping in intervals. This will also improve your memory.

28. Make colleagues: Always try to make colleagues. No matter how sharper or intelligent you are, if you make colleagues you can have several ideas, which will be helpful for your research.

29. Think technically: Always think technically. If anything happens, then search its reasons, its benefits, and demerits.

30. Think and then print: When you will go to print your paper, notice that tables are not be split, headings are not detached from their descriptions, and page sequence is maintained.

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33. Report concluded results: Use concluded results. From raw data, filter the results and then conclude your studies based on measurements and observations taken. Significant figures and appropriate number of decimal places should be used. Parenthetical remarks are prohibitive. Proofread carefully at final stage. In the end give outline to your arguments. Spot out perspectives of further study of this subject. Justify your conclusion by at the bottom of them with sufficient justifications and examples.

34. After conclusion: Once you have concluded your research, the next most important step is to present your findings. Presentation is extremely important as it is the definite medium though which your research is going to be in print to the rest of the crowd. Care should be taken to categorize your thoughts well and present them in a logical and neat manner. A good quality research paper format is essential because it serves to highlight your research paper and bring to light all necessary aspects in your research.

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The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently. You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.



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- Sum up your conclusion in text and demonstrate them, if suitable, with figures and tables.
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Topics	Grades		
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Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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ISSN 9755861

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