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Modified Lifting Based DWT/IDWT Architecture for OFDM on Virtex-5 FPGA

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Abstract - A future Wireless communication requires high performance and high speed integrated data, audio, video and multimedia services. This performance is achieved using discrete wavelet transforms in terms of ISI and bandwidth compatibility over FFT based OFDM. Where FFT based OFDM has very compact spectral utilization which cannot satisfy the future needs. This project proposes implementation of new modified lifting wavelet transform for designing wavelets and performing the transform. By implementing LDWT, it is able to increase the spectral efficiency and also decrease the bit error rate. This paper presents a performance measure of mean squared error by using lifting wavelet transform. This paper shows that DWT-OFDM outperformed FFT-OFDM by approximately 6dB gain in BER, Haar wavelet showed best performance over other wavelets by approximately 2dB. However, computation complexity of DWT restricts use of DWT for OFDM due to its hardware requirements on VLSI platform. In this work, lifting based DWT is modified and a new architecture is derived that can compute DWT in less than 3.429ns, and consumes power of less than 28mW.

Keywords : OFDM, DWT, MULTIWAVELETS, DMWT.

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Modified Lifting Based DWT/IDWT Architecture for OFDM on Virtex-5 FPGA

Anitha.K^α, Dr.Dharmistan.K.Varugheese^σ & Dr N.J.R.Muniraj^ρ

Abstract - A future Wireless communication requires high performance and high speed integrated data, audio, video and multimedia services. This performance is achieved using discrete wavelet transforms in terms of ISI and bandwidth compatibility over FFT based OFDM. Where FFT based OFDM has very compact spectral utilization which cannot satisfy the future needs. This project proposes implementation of new modified lifting wavelet transform for designing wavelets and performing the transform. By implementing LDWT, it is able to increase the spectral efficiency and also decrease the bit error rate. This paper presents a performance measure of mean squared error by using lifting wavelet transform. This paper shows that DWT-OFDM outperformed FFT-OFDM by approximately 6dB gain in BER, Haar wavelet showed best performance over other wavelets by approximately 2dB. However, computation complexity of DWT restricts use of DWT for OFDM due to its hardware requirements on VLSI platform. In this work, lifting based DWT is modified and a new architecture is derived that can compute DWT in less than 3.429ns, and consumes power of less than 28mW. The modified DWT is realized on Virtex II FPGA and occupies resources less than 114 slices. Thus the proposed DWT architecture is suitable for OFDM application.

Keywords : OFDM,DWT ,MULTIWAVELETS,DMWT.

I. INTRODUCTION

Wireless communication systems, limited bandwidth allocations coupled with a potentially large group of users restrict the bandwidth availability to the users. The success of wireless communication systems thus depends heavily on the development of bandwidth efficient data transmission schemes. Wireless multicarrier modulation (MCM-OFDM) is a technique of transmitting data by dividing the input data stream into parallel sub streams where each stream is modulated and multiplexed onto the channel at different carrier frequencies [1]. In OFDM, the message which is symbol mapped using QAM scheme is modulated using complex carrier which introduces orthogonality between multiple carrier signals. The orthogonally modulated signal is transmitted in the channel with narrow band requirements, thus improving throughput as well as high data rate.

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At the receiver, the inverse transform is performed to retrieve message symbols from the orthogonally modulated data. Currently FFT is used for forward and inverse transform operation performing orthogonal modulation at the receiver and transmitter respectively. The limitations of FFT such as ISI and bandwidth occupation due to cyclic prefix can be minimized with use of Wavelet Transform. Wavelets are known to have compact support (localization) both in time and frequency domain, and possess better orthogonality [8]. A hopeful application of wavelet transform is in the field of digital wireless multicarrier communication where they can be used to generate waveforms that are fit for transmission over fading channels [1, 2, 3, 4, 30].

The major advantage of wavelet based OFDM is its optimal performance over conventional OFDM (FFT based OFDM). Wavelet bases therefore appear to be a more logical choice for building orthogonal waveform sets usable in communication. In this work we study orthogonal wavelet bases OFDM. Inter Symbol Interference (ISI) and Inter Carrier Interference (ICI) causes by loss of orthogonality between the carriers is reduced by using orthogonal wavelets. The work addresses performance of wavelet OFDM using different orthogonal wavelet basis families such as Haar, Daubechies, Symlets, Coiflets and Discrete Meyer over wireless channels and tries to investigate a suitable wavelet based OFDM for its better performance.

II. REVIEW OF RELATED RESEARCH

There are several papers reporting the advantages of DWT over FFT for orthogonal modulation. Wornell and Oppenheim outlined the design of the transmitter and receiver for wavelet modulation (WM) [30]. They proved that the estimate of the received bit becomes more accurate as the number of noisy observations is increased. Haixia Zhag et al. based on tharfeir work titled research of discrete Fourier transform based OFDM (DFT-OFDM) and discrete wavelet transform based OFDM (DWT-OFDM) on different Transmission Scenarios concluded that DWT-OFDM performs much better than DFT-OFDM. But they observed an error floor in DWT- OFDM systems [2]. They suggested that it may be resulted from the Haar wavelet base, since different wavelet base is of different characteristics.

Some other wavelet bases are expected to be employed to improve performance of DWT- OFDM [2]. Akansu et al. [24] emphasized the relation between filter banks and transmultiplex theory and predicted that wavelet packet based modulation has a role to play in future communication systems. Dereje Hailemariam [3] investigated the performance of MultiCarrier-CDMA in the three transmission scenarios and in his direction to the future work he predicts that designing of wavelet filters which are better suited to OFDM left as an area to be explored. Yesuf Shiferaw [32] showed that Daubechies wavelet family can be a viable alternative suitable basis for future OFDM communication scheme. It reduced the probability of bit error rates, providing better performance gains. Mohammed About kadhim and Widad Ismail [33] proved that proposed DWT-OFDM design achieved much lower bit error rates and better performance than FFT-OFDM. The proposed system obtains higher spectral efficiency, therefore this structure can be considered an alternative to the conventional OFDM, and can be used at high transmission rates with better performance. Mohamed H. M. Nerma et al. [34]

Dual-Tree Complex Wavelet Transform (DT-CWT) is used to replace the fast Fourier transform (FFT) in the conventional OFDM and also to the wavelet packet modulation (WPM) based OFDM system. With considerable improvement in terms of bit error rate (BER) and achieves better peak-to-average power ratio (PAPR) performance at acceptable increase in computational complexity. Most of the work reported in literature is based on software simulations carried out. However, for practical implementation of DWT based OFDM, the major bottleneck is the hardware efficient architecture for DWT and IDWT. In this paper, we propose a modified DWT/IDWT architecture that reduces the computation complexity and improves throughput and latency is designed and implemented on FPGA. Section III provides a brief introduction to Wavelet Transforms, Section IV discusses lifting scheme based DWT architecture, section V discusses modified lifting based DWT. Results and discussion is presented in section V and conclusion in section VI.

III. DISCRETE WAVELET TRANSFORM

Discrete Wavelet Transform (DWT) wavelets are better localized in both time and frequency with desirable characteristics. DWT possess the property of orthogonality across scale and translation. The discrete wavelet transform (DWT) provides a means of decomposing sequences of real numbers in a basis of compactly supported orthonormal sequences each of which is related by being a scaled and shifted version of a single function. The DWT of a signal $x(t)$ is the set of coefficients $X(m, k)$ DWT for m and k obtained as the inner product of the signal $x(t)$ and the wavelet function, $\Psi_{m,k}$. The discrete wavelet and inverse discrete

representation of a signal $x(t)$ is given by (3.1) and (3.2) respectively

$$X_{DWT}^m_k = \int_{-\infty}^{\infty} x(t) \frac{1}{\sqrt{2^m}} \psi(2^m t - k) dt \quad (3.1)$$

$$X_{IDWT}(t) = \sum_{m=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} X_k^m \frac{1}{\sqrt{2^m}} \psi(2^m t - k) \quad (3.2)$$

Where is $\Psi_{m,k}$ the wavelet function [30]. Mallat's fast wavelet transform (FWT) provides a computationally efficient, practical, discrete time *algorithm* for computing the DWT.

IV. PROPERTIES OF WAVELETS

The most important properties of wavelets are the *admissibility* and the *regularity* conditions and these are the properties which gave wavelets their name.

a) Admissibility

The square integral function $Y(t)$ satisfying the *admissibility condition*,

$$\int \frac{|\psi(\omega)|^2}{|\omega|} d\omega < +\infty \quad (3.3)$$

Can be used to first analyze and then reconstruct the signal without loss of information. In the above equation $Y(\omega)$ is the Fourier Transform of $Y(t)$. The admissibility condition implies that the Fourier Transform of $Y(t)$ vanishes at zero frequency, i.e.

$$\int \frac{|\psi(\omega)|^2}{|\omega|} d\omega < +\infty \quad (3.4)$$

This means that wavelets must have a band-pass like spectrum. A zero at the zero frequency also means that the average value of the wavelet in time domain must be zero,

$$|\psi(\omega)|^2|_{\omega=0} = 0 \quad (3.5)$$

Therefore it must be oscillatory. That is $Y(t)$ must be a wave.

b) Regularity

As can be seen from equation below

$$X_{CWT}(s, \tau) = \int x(t) \psi_{s,\tau}(t) dt \quad (3.6)$$

The wavelet transform of a one-dimensional function is two-dimensional. The time-bandwidth product of the wavelet transform is the square of the input signal and for most practical applications this is not a desirable property. Therefore one imposes some additional conditions on the wavelet functions in order to make the wavelet transform decrease quickly with decreasing scale s . These are the *regularity* conditions and they state that the wavelet function should have some smoothness and concentration in both time and frequency domains. Regularity is a quite complex concept and we will try to explain it a little using the concept of vanishing moments (approximation order).

c) Vanishing moments

If we expand the wavelet transform (2.1) into the Taylor series at $t=0$ until order n (let $\tau = 0$ for simplicity) we get

$$X(s, 0) = \frac{1}{\sqrt{s}} \left[\sum_{p=0}^N x^{(p)}(0) \frac{t^p}{p!} \psi\left(\frac{t}{s}\right) dt + R(n+1) \right] \quad (3.7)$$

Here $x^{(p)}$ stands for the p^{th} derivative of x and $R(n+1)$ means the rest of the expression. Now if we define the moments of the wavelet by

$$N_p = \int t^p \psi(t) dt \quad (3.8)$$

Then we can write the equation (2.49) into the finite development

$$X(s, 0) = \frac{1}{\sqrt{s}} \left[x(0)N_0s + \frac{x^{(1)}(0)}{1!}N_1s^2 + \dots + \frac{x^{(n)}(0)}{n!}N_ns^{n+1} + R(s^{n+2}) \right] \quad (3.9)$$

From the admissibility condition we already have that the 0^{th} moment $N_0 = 0$ so that the first term in the right hand side of (2.50) is zero. If we now manage to make the other moments up zero, then the wavelet transform coefficients $x(s, t)$ will decay as fast as s^{n+2} for a smooth signal $x(t)$. This is known in as the vanishing moments or approximation order. If a wavelet has N vanishing moments, then the approximation order of the wavelet transform is also N . With increasing number of vanishing moments the wavelet becomes smoother or more regular. Summarizing, the *admissibility* condition gave us the wave, *regularity* and *vanishing moments* gave us the fast decay or the let, and put together they give us the wavelet.

V. SOFTWARE REFERENCE MODEL

In order to compare the performances of OFDM model using DWT, in this work Simulink model is developed to compute BER performances of FFT OFDM with DWT OFDM. A sinusoidal signal of 10-100 MHz frequency is preprocessed and is symbol mapped. The symbol mapped data is modulated using IFFT as well as IDWT and the modulated data is transmitted through a noisy channel. A gain factor is used to improve the transmission gain at the transmitter. The received data is demodulated and BER computation is carried out. Table 1 shows the software simulation results of BER values for FFT-OFDM and DWT-OFDM using different modulations. From the results obtained it is found that DWT based OFDM achieves better BER for most of the modulation schemes.

Modulation schemes	FFT-OFDM	DWT-OFDM
16-QAM	0.9688	0.9196
32-QAM	0.9031	0.8703
64-QAM	0.9987	0.8547
128-QAM	1	0.8704
512-QAM	0.7071	0.6911
64-PSK	0.9774	0.8889
128-PSK	0.9921	0.8897

Table 1 : BER comparison of OFDM schemes (FFT vs. DWT)

The BER for FFT based OFDM and DWT based OFDM are almost closer thus it would be very difficult to conclude the performances. Thus in order to estimate the performances, the channel noise and gain factor were varied to the worst cases to prove the performances of DWT to be better than FFT. In FFT the basis function is complex sine wave, in DWT there are multiple basis functions. Thus in order to identify a suitable wavelet, an experimental setup is developed to compare the performances of various wavelet functions in OFDM. We limit our performance analysis to wavelet OFDM based on widely used wavelet families such as Haar, Daubechies, Symlets, Coiflets Meyer & biorthogonal. The primary wavelet family we have been focusing is the one that satisfies the characteristics which are demanded features for representing the signal in wireless transmission over fading channels as in the table 2. Daubechies, the asymmetric wavelet family satisfies these characteristics which are demanded feature for representing the signal in communication.

Wavelets	AWGN	Rayleigh Fading	Rician Fading
Haar	0.9762	0.9916	0.9754
Daubechies	0.9773	0.9900	0.9858
Symlets	0.9773	0.9900	0.9858
Coiflets	0.9767	0.9977	0.9855
Biorthogonal	0.9762	0.9916	0.9754
Discrete Meyer	0.9765	0.9866	0.9823

Table 2 : BER values for DWT-OFDM in Different channels using 64-QAM

Table 2. BER Comparisons between AWGN channel and Rayleigh Fading Channel using 64-QAM the results obtained, it is found that Haar wavelet

achieves better BER compared with other techniques. Hardware implementation of Haar is complex and thus biorthogonal filter is adopted for hardware implementation as it achieves BER closer to haar. In the next section, a detailed discussion on design and implementation of 9/7 wavelet filter for OFDM is presented.

VI. DWT BASED OFDM SYSTEM

Figure 1 shows the block diagram of a typical OFDM transceiver. The digital data is to be transmitted by the transmitter section. Then it is applied into a mapping of subcarrier amplitude and phase. Then by using an Inverse Fast Fourier Transform (IFFT) it transforms this spectral representation of the data into the time domain.

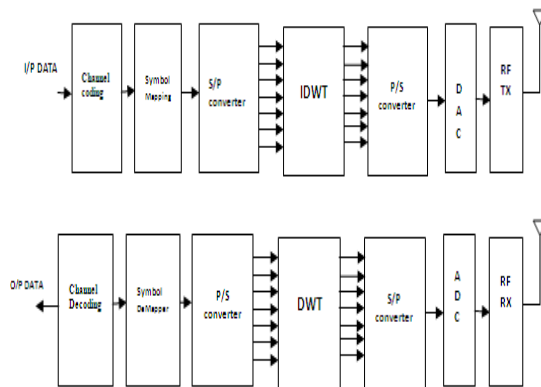


Figure 1 : Complete OFDM system

To modulate the data bits on the sub carriers, different modulation techniques are used. The N sub blocks are created by dividing the stream of bits. By using constellation modulator such as QPSK and QAM the n sub blocks are mapped. Depends on the quality of communication channel the modulators are selected. The calculated time domain signal is mixed up to the required frequency to transmit the OFDM signal.

The reverse operation of the transmitter is performed by the receiver section. The Conversion of RF signal to base band is done by using the mixing process. To analyze the signal in the frequency domain Fast Fourier Transform (FFT) is used.

Transmitted data is typically in the form of a serial data stream. In OFDM, each symbol typically transmits 40 - 4000 bits, and so a serial to parallel conversion stage is needed to convert the input serial bit stream to the data to be transmitted in each OFDM symbol. The parallel to serial converter is the reverse process. Robustness against multi path delay is one of the most important properties of OFDM.

The accomplishment is done by adding the guard period between transmitted symbols. The most successful guard period is a "cyclic prefix", which is appended at the front of every OFDM symbol. To

eliminate the inter symbol interference (ISI) completely; the guard time is needed for each OFDM symbol. The chosen guard time is to be larger than the estimated delay spread, such that the multipath components from one symbol do not interfere with next symbol. A copy of the last part of the OFDM symbol is cyclic prefix, and is of equal or greater length than the maximum delay spread of the channel.

VII. IMPROVED DWT ARCHITECTURE

Daubechies (9,7) wavelet filter with $N=2$ is used for architecture development. Lifting scheme is used for the development of architecture. Here $N=2$ means, we will be having two stages of lifting scheme i.e predict1, update1 and in second stage predict2, update2.

VIII. LIFTING BASED DWT ARCHITECTURE

The convolution-based 1-D DWT requires both a large number of arithmetic computations and a large memory for storage. Such features are not desirable for either high speed or low-power applications. Recently, a new mathematical formulation for wavelet transformation has been proposed by Swelden as a light-weighted computation method for performing wavelet transform. The main feature of the lifting-based wavelet transform is to break-up the high pass and the low pass wavelet filters into a sequence of smaller filters. The lifting scheme requires fewer computations compared to the convolution based DWT. Therefore the computational complexity is reduced to almost a half of those needed with a convolution approach. The lifting-based wavelet transform basically consists of three steps, which are called split, lifting, and scaling, respectively, as shown in Figure 2

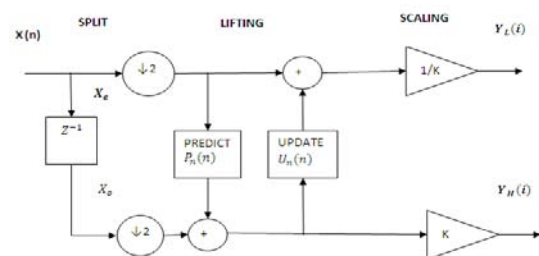


Figure 2 : The lifting scheme implementation of 1D-DWT [11]

The basic idea of lifting scheme is first to compute a trivial wavelet (or lazy wavelet transform) by splitting the original 1-D signal into odd and even indexed sub sequences, and then modifying these values using alternating prediction and updating steps. The lifting scheme algorithm can be described as follow:

1. Split step: The original signal, $X(n)$, is split into odd and even samples (lazy wavelet transform).

2. Lifting step: This step is executed as N sub-steps (depending on the type of the filter), where the odd and even samples are filtered by the prediction and update filters, $Pn(n)$ and $Un(n)$.

3. Normalization or Scaling step: After N lifting steps, a scaling coefficients K and 1/K are applied respectively to the odd and even samples in order to obtain the low pass band (YL(i)), and the high-pass sub-band (YH(i)). Fig. 4.2 illustrates how the lifting scheme can be implemented using these steps. The diagram shows the lifting scheme for Daubechies (9, 7) biorthogonal filter.

The lifting scheme algorithm to the (9,7) filter is applied as:

a) Split step

$X_e \leftarrow X(2i)$ Even Samplesequation 4.1.1

$X_o \leftarrow X(2i+1)$ Odd Samplesequation 4.1.2

b) Lifting Steps

For (9, 7) filter, N=2

Predict P1: $D(i) = X_o(i) + a [X_e(i) + X_e(i+1)]$
.....equation 4.1.3

Update U1: $S(i) = X_e(i) + b [D(i-1) + D(i)]$
.....equation 4.1.4

Predict P2: $Y_H(i) = D(i) + c [S(i) + S(i+1)]$
.....equation 4.1.5

Update U2: $Y_L(i) = S(i) + d [Y_H(i-1) + Y_H(i)]$
.....equation 4.1.6

c) Scaling Step

$Y_H(i) = K Y_H(i)$ equation 4.1.7

$Y_L(i) = 1/K Y_L(i)$ equation 4.1.8

where $a=-1.586134342$, $b=-0.0529801185$, $c=0.882911076$, $d=-0.443506852$, and $K=1.149604398$. These fractional values are multiplied by a factor of 128 to convert them to decimal values.

Stage1: In this stage even and odd bits are considered accordingly and equation 4.1.3 is computed to get predict1 output $D[i]$.

Stage 2: The predict1 output ($D[i]$) along with even position of initial inputs are taken to compute equation 4.1.4, which results in update1 output $S[i]$.

Stage 3: Predict1 ($D[i]$) and Update1($S[i]$) outputs are taken to compute equation 4.1.5, which results in Predict2 output $Y_H[i]$.

Stage 4: Predict2 ($Y_H[i]$) and Update1 ($S[i]$) outputs are taken to compute equation 4.1.6, which results in Update2 output $Y_L[i]$.

Just reverse operation of this with corresponding sign change is carried out to compute IDWT.

IX. MODIFIED DWT FOR OFDM

From the lifting scheme equation presented in the previous section, it is found that the final scaling and dilation coefficients are interdependent on predict and update outputs, thus there is a delay and also affects throughput. In order to improve the latency and throughput of DWT computation it is required to minimize the interdependence of partial outputs of lifting scheme, thus a modified lifting scheme is derived. The modified equations for a_i and d_i can be obtained by substituting eqn. (4.1.1)-(4.1.6) in (4.1.7) and (4.1.8). The lifting coefficients were substituted and the results were scaled by multiplying with 256 to avoid decimal and to round off the values. The modified lifting scheme equation is as follows:

The approximation coefficient is:

$$\begin{aligned} a_i = & 294*(8*(6*x_{2i}+4*x_{2i-2}+x_{2i+4}+x_{2i+4}+x_{2i-4}+4*x_{2i+2}) - \\ & 5*(3*x_{2i+1}+x_{2i+3}+x_{2i+3}+3*x_{2i-1}) + \\ & 100*(2*x_{2i}+x_{2i+2}+x_{2i+2}) - \\ & 180*(2*x_{2i}+x_{2i+2}+x_{2i+2}) + \\ & 113*(x_{2i+1}+x_{2i+1}) + \\ & 21*(2*x_{2i}+x_{2i+2}+x_{2i+2}) - \\ & 13*(x_{2i+1}+x_{2i+1}+x_{2i-1}). \text{----- eqn 4.1.9} \end{aligned}$$

The detail coefficient is:

$$\begin{aligned} d_i = & 19*(3*x_{2i}+3*x_{2i+2}+x_{2i+4}+x_{2i-2}) + \\ & (-12)*(2*x_{2i+1}+x_{2i-1}+x_{2i+3}) + \\ & 226*(x_{2i}+x_{2i+2}) - \\ & 406*(x_{2i}+x_{2i+2}) + x_{2i+1} \text{-----eqn 4.1.10} \end{aligned}$$

By substituting $i=2$ for the above equations we get,

$$\begin{aligned} a_2 = & 294*(8*((6*x_4)+(4*2)+(2*x_8)+x_0+(4*x_6)) - \\ & 5*((3*x_5)+(2*x_7)+(3*x_4)) + \\ & 100*((2*x_4)+(2*x_6)) - \\ & 180*((2*x_4)+(2*x_6)) + \\ & (226*x_5)+42*(x_4+x_6)- \\ & (13*x_5)+x_4+x_3 \text{----- eqn 4.1.11} \\ d_2 = & 19*((3*x_4)+(3*x_6)+x_8+x_6) - \end{aligned}$$

$$12*((2*x5)+x3+x7) +$$

$$226*(x4+x6) -406*(x4+x6)+x5-----eqn 4.1.12$$

The modified lifting scheme equations are realized using multipliers, adders and intermediate registers. Wallace tree multiplier is chosen for faster multiplication operation. Carry save adder is adopted for addition operation as it uses minimum gates and also has very less delay compared with ripple carry adder. The input samples are loaded into the input data register, after every 9 clock cycles the multiplication and addition operations are performed. Computation of a_i and d_i coefficients requires 4 clock cycles. Thus the latency of the proposed architecture is 13 clock cycles (9 + 4), and the throughput is 5 clock cycles. The modified lifting based DWT architecture is faster than generic DWT architecture by 4 clock cycles.

The equation shown above for $i=2$, computation of a_i and d_i requires input samples x_8 to x_0 , thus a serial in parallel out 8-bit shift register is used to load the input data after 9 clock cycles, the input samples are multiplied by the coefficients and wavelet coefficients are computed. Thus the modified architecture shown in the figure above has a initial latency of 9 clock cycles and throughput of 0.5. By interchanging the coefficients of low pass and high pass, IDWT can be computed.

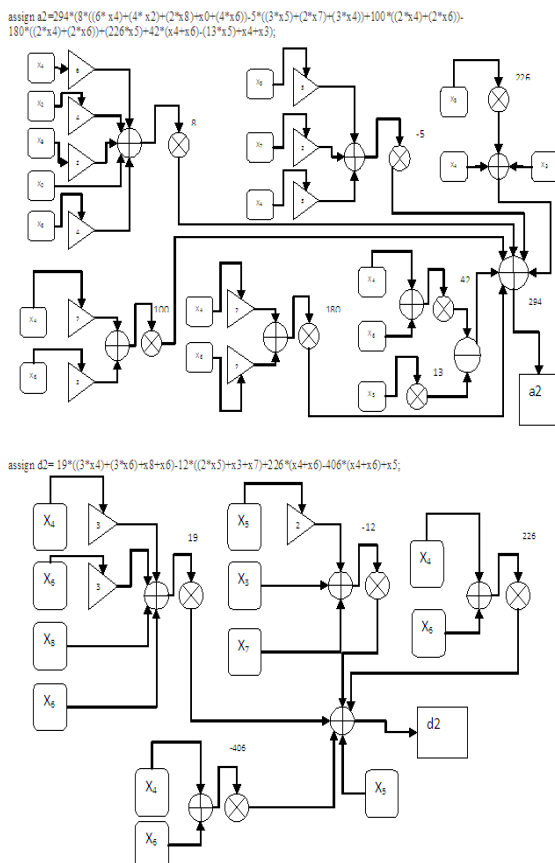


Figure 3 : Modified architecture for Lifting Discrete Wavelet Transform

Thus the proposed architecture is better in terms of latency and throughput when compared with generic lifting scheme architecture. The modified lifting scheme is model using HDL and is functionally verified using ModelSim. The functionally correct HDL model is synthesized using Xilinx ISE targeting Virtex-5. For OFDM, the QAM modulated output is stored in intermediate memory and the samples are sequentially read and modulated using IDWT, the modulated data is stored in output memory. At the receiver, the data stored in memory is further processed using DWT, and is demodulated using QAM demodulator.

X. FPGA IMPLEMENTATION OF DWT FOR OFDM

Synthesis is the transformation of design from higher level of abstraction to lower level of abstraction .The DWT design using Lifting Scheme is carried out on Virtex5 FPGA development kit. In our implementation, Xilinx Virtex5 using device xc2vp30-7-f896 with 1000K gate count FPGA is used. It has total 10K numbers of configurable logic blocks (CLBs) arranged in 32 X 28 matrix fashion. Each CLB has four slices and two of them are named as SLICEM and rest two as SLICEL. Each SLICEM can be used as 16 bit (embedded)shifregister(SRL16).i.e

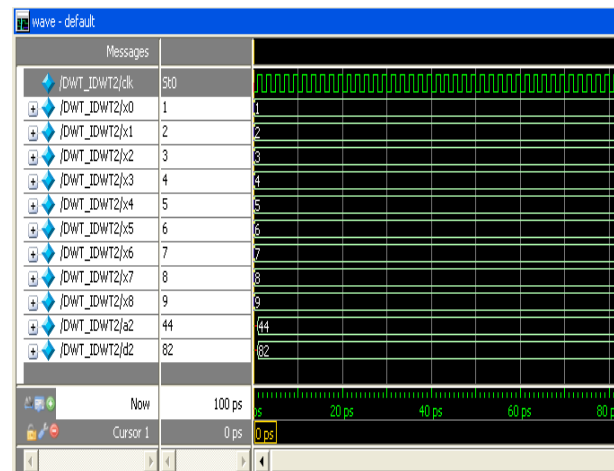


Figure 4 : Post Place and Route Simulation

It is seen in figure 4 that the pre-simulation and post place and route simulation results match, thereby proving that the design is perfectly mapped onto FPGA meeting the required design specifications.

a) Synthesis on Virtex5

The design summary is shown below highlighting the major device utilization in terms of LUT's and slices. Device utilization summary:

Selected Device : 2vp30ff896-7

- Number of Slices: 114 out of 13696 0%
- Number of 4 input LUTs:220 out of 27392 0%

- Number of IOs: 89
- Number of bonded IOBs: 73 out of 556 13%
- IOB Flip Flops: 8
- Number of MULT18X18s: 12 out of 136 8%
- Number of GCLKs: 1 out of 16 6%
- Total CPU time to Xst completion: 31.44secs
- Total delay: 3.459ns
- Total estimated power consumption 28mW

b) RTL Schematic of the design

Figure 6 below shows the RTL schematic of the proposed design with interconnects between the various blocks. It is a technology independent schematic.

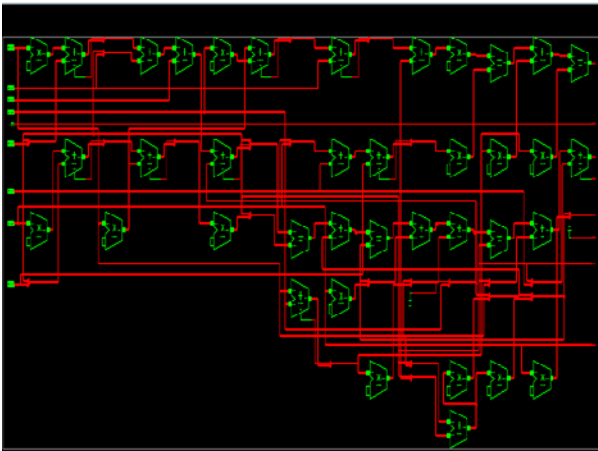


Figure 5 : RTL Schematic

c) HDL Co-Simulation

The HDL co simulation of the design is performed using matlab simulation which is shown in Figure 6 below.

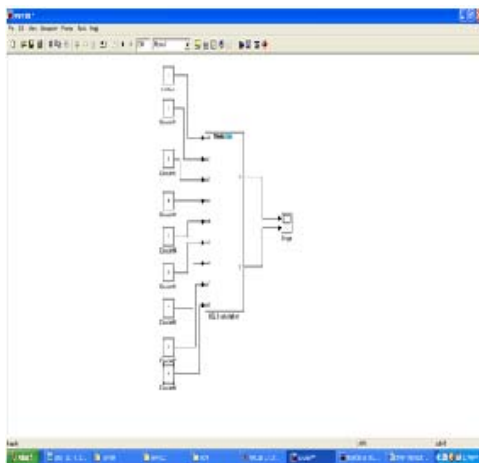


Figure 6 : HDL Co-Simulation

XI. CONCLUSION

DWT based OFDM is finding importance due to its performance in terms of ISI and bandwidth

compatibility over FFT based OFDM. The DWT-OFDM outperformed FFT-OFDM by approximately 6dB gain in BER, Haar wavelet showed best performance over Biorthogonal (bior3.3, bior5.5), Daubechies (db2,db4), reverse biorthogonal (rbior3.3, rbior5.5) by approximately 2dB. However, computation complexity of DWT restricts use of DWT for OFDM due to its hardware requirements on VLSI platform. In this work, lifting based DWT is modified and a new architecture is derived that can compute DWT in less than 3.429ns, and consumes power of less than 28 mW. The modified DWT is realized on Virtex II FPGA and occupies resources less than 114 slices. Thus the proposed DWT architecture is suitable for OFDM application. The performance of DWT architecture can be further enhanced by introducing parallel processing and pipelining schemes to improve throughput and latency.

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Performance Analysis of Dynamic OCDMA using Matlab

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Abstract - A DOCDMA (dynamic optical code division multiple access) communication system is projected for high-bandwidth communication systems. At the receiver, a synchronized TOF with the same function is used as a decoder. In this system, an electrically controlled tunable optical filter (TOF) is used to encode the modulated broadband light source. This technique dynamically modulates the central wavelength of a TOF as per a functional code at the transmitter during the bit period earlier the transmission of the data. The system is examined taking into account multiple access interference (MAI), thermal noise, and phase-induced intensity noise (PIIN). In these paper we understand that the performance of proposed dynamic OCDMA. It's improve the bit error rate & reduce the MAI (multiple access interference) & PIIN (Phase Induced Intensity Noise). The simulation result show that the proposed DOCDMA system reduces the PIIN effect on the performance of the system and improves the bit error rate (BER) performance at a maximum number of users. Also, it is found that when the effective power is large enough, the MAI becomes the main factor that limits system performance, whereas when the effective power is comparatively low, both thermal noise and PIIN develop the main restrictive factors with thermal noise having the main effect.

Keywords : DOCDMA, BER, TOF, MAI, PIIN.

GJRE-F Classification : FOR Code : 090601



Strictly as per the compliance and regulations of:



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I. INTRODUCTION

Numerous optical CDMA communication systems have been proposed in the last two eras. Attractive incoherent systems are, among others, spectral amplitude coding (SAC), direct sequence (DS), and fast frequency hopping (FFH) optical CDMA systems. DS optical CDMA system encodes the incoherent pulses in time domain and recovers the data at the receiver using tapped delay lines. The performance of this system is pitiable because of the correlation properties of the unipolar codes used, which contributes to a high level of multiple access interference (MAI). SAC scheme is a more recent technique in optical CDMA systems where the spectrum of a broadband source is amplitude-encoded. In both systems, MAI can be canceled by balanced detection and code sequences with fixed in-phase cross correlation. However, its performance is still narrow by phase induced intensity noise (PIIN). This limits the maximum

number of users in the system. Furthermore, the spatial distance between the gratings and the number of gratings limits the users data bit rate in the system. Moreover, all the above systems are either non-reconfigurable, or they need complicated reconfigurable encoders. In this paper we propose an easily reconfigurable optical CDMA (OCDMA) system. The encoder varies the central frequency of a pulse of optical signal according to the functional code set to the controller. The system can recover the encoded data by matched decoders at the receiver. In OCDMA, the TOF should be able to follow the functional code given as an electrical signal by the controller during one bit interval. The small data bit interval of the high data bit rate system requires fast TOF or special code with tuning range suitable with the speed of the TOF. However, tunable optical filters which can scan 10's of Nanometers within few nanoseconds have been reported. Thus, the encoder and decoder can be easily and quickly reconfigured to any of the functional codes. The implementation of the system leads to better performance of the network. It is shown here that the system performance is better than that of SAC and FFH systems recently.

II. SYSTEM CONFIGURATION AND DESCRIPTION

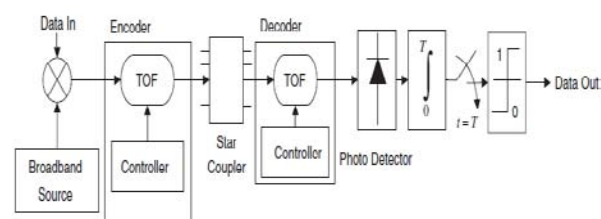


Fig. 1 (a) : Block diagram of dynamic OCDMA system

The block diagram in Fig. 1(a) shows the dynamic OCDMA Configuration . The incoming signal from the light source (OOK) modulated with the binary data. If the data bit is "1", encoder will filters the spectrum of the pulse at a central wavelength varies with time according to a functional code, otherwise no power is transmitted. The encoder is a TOF controlled with an electrical signal that represents the functional code. Signals transmitted from all synchronized users will be joint using a star coupler before received by all users. At the receiver, the complex signal is decoded by a

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matched TOF. For recuperate the transmitted data, the signal passes through a photo detector, an integrator, and a threshold decision. The source spectra are assumed to be flat over the bandwidth of ν_0 with magnitude P_r/u , where u_0 is the central optical frequency, D_u the system bandwidth, and P_r the received effective average power from a single source. Some additional losses in the route of the signal and the receiver are supposed to be integrated in P_r . Ideal covering at the TOF is also assumed, and every operator is considered to have the similar effective average power at each receiver

III. CODE DETAILS

The core condition in the functional codes construction is toward reduce the number of intersecting points among any couple of functions then they increase the interfering power between users. The part of intersection among any two functions is associated directly to the cost of interfering power. The code family is given by

$$F^j(t) = \Delta/2(\sin(2\pi ft - j\phi)) \quad (1)$$

Where K is the no. of simultaneous users, f is the ϕ frequency of functional codes and f is the phase shift between different functions. Shifted sine functions are offered for their ease and the possibility of completing the large number of required codes by decreasing the phase shift. The TOF in dynamic OCDMA should be capable to follow the functional code driving the filter. The required speed of the TOF and its controller is defined as the derivative of the code and given by

$$S^j(t) = \Delta \nu \pi f (\sin(2\pi ft - j\phi)) \quad (2)$$

It is directly related to the frequency and amplitude of the functional code. Hence, other codes could be proposed to improve the system performance and operation of the system for high data bit rates. Also, the functional codes should start and stop at the same central wavelength in the data bit interval (T) for even modulation of the TOF and its controller. For these explanations, we use the smallest frequency probable for the SSC which matches to the data bit rate.

IV. DYNAMIC-OCDMA PERFORMANCE ANALYSIS

The PSD $G(\nu, t)$ of the signal at the receiver's input is the sum of all active users transmitted signals.

$$G_m^i(\nu, t) = \frac{P_r}{\Delta \nu} \sum_{j=1}^K b^j \text{rect} \left(\frac{\nu - \nu_0 - F^j(t)}{BW} \right) \quad (3)$$

where P_r is the effective power
The decoder output is given below

$$G_M^0(\nu, t) = \frac{P_r}{\Delta \nu} b^m \text{rect} \left(\frac{\nu - \nu_0 - F^m(t)}{BW} \right) + \left(\frac{P_r}{\Delta \nu} \sum_{j=1, j \neq m}^K b^j \text{rect} \left(\frac{\nu - \nu_0 - F^j(t)}{BW} \right) \right) * \text{rect} \left(\frac{\nu - \nu_0 - F^m(t)}{BW} \right) \quad (4)$$

After the integrator and sampler, the optical photocurrent is

$$I_m = 1/T \int_{T=0}^T I_m(t) dt = K b^m \frac{P_r}{\Delta \nu} BW + K \frac{P_r}{T \Delta \nu} \sum_{j=1, j \neq m}^K b^j * \sum_{i=1}^{N_{mj}} (BW (t H_i^{mj} - t L_i^{mj}) - \int_{t L_i^{mj}}^{t H_i^{mj}} |F^j(t) - F^m(t)| dt). \quad (5)$$

In the analysis of bit error rate (BER), we consider the effect of MAI, PIIN, and the thermal noise. Other sources, like shot noise and receiver's dark current noise, are neglected. Gaussian approximation is assumed for the distribution of the noise in the calculation of the BER.

Since the system is synchronized, users m and j will interfere at the same points in time relative to the beginning of the bit period and the intersecting edges ($1L_{i,m,j}, 1H_{i,m,j}$) are the same whenever users m and j are active. This results in a constant value of $DAI(m, j)$ if users m and j are active, otherwise $DAI(m, j)$ is zero. For equi probable data, $DAI(m, j)$ is a random variable with Average

$$\mu_{DAI} = \frac{1}{K^2 - K} \sum_{m=1}^K \sum_{j=1, j \neq m}^K DAI(m, j) \quad (6)$$

And variance

$$\sigma_{DAI}^2 = \frac{1}{K^2 - K} \sum_{m=1}^K \sum_{j=1, j \neq m}^K (DAI(m, j) - \mu_{DAI})^2 \quad (7)$$

Since we do not know which user will be active at any given time, we average over all code pairs. The mean MAI can be approximated as $4DAI$ and the variance is $(K-1) V2DAI$.

Incoherent light sources mixed at the input of the photodetector will cause intensity noise in the output current (PIIN). The variance of the photocurrent due to this type of noise is

$$\sigma_{PIIN_m}^2(t) = I^2 \tau_c(t) B \quad (8)$$

Then, the variance of PIIN is zero at no interference and at the points of interference, Averaging along the bit period and averaging over all users will get the PIIN

Variance equation as

$$\frac{1}{\sigma_{PIIN}^2} = \frac{1}{K} \sum_{m=1}^K \frac{1}{T} \int_0^T B K^2 \sum_{j=1, j \neq m}^K \left(\frac{P_r}{\Delta \nu} b_m + \frac{P_r}{\Delta \nu} b_j \right)^2 * (BW F^m(t) - F^j(t)) + \left(\frac{P_r}{\Delta \nu} b \right)^2 |F^m(t) - F^j(t)| * (u(t - \tau L_i^{mj}) - u(t - \tau H_i^{mj})) dt. \quad (9)$$

The Signal to Noise ratio is

$$\text{SNR}(K) = \frac{I^2}{(K-1)\sigma_{DAI}^2 + \sigma_{PIN}^2 + \frac{4K_b T_N B}{R_t}} \quad (10)$$

According to the Central Limit Theorem, we can consider that the pdf of the variables obeys the Gaussian Distribution.

The Probability of Error is

$$\text{BER}(K) = 1/2\text{erfc}(\text{SNR}(K)/2)$$

V. SIMULATION TOOLS

For this implementation MATLAB is very suitable tool. **MATLAB** (matrix laboratory) is a calculating environment and fourth-generation programming language. Developed by Math Works, MATLAB allows matrix manipulations, plotting of functions and data, implementation of algorithms, creation of user interfaces, and interfacing with programs written in other languages, including C, C++, Java, and Fortran.

Although MATLAB is intended primarily for numerical computing, an optional toolbox uses the MuPAD symbolic engine, allowing access to symbolic computing capabilities. An additional package, Simulink, adds graphical multi-domain simulation and Model-Based Design for dynamic and embedded systems.

In 2004, MATLAB had around one million users across industry and academia.^[2] MATLAB users come from various backgrounds of engineering, science, and economics. MATLAB is widely used in academic and research institutions as well as industrial enterprises.

VI. SIMULATION RESULTS

The BER for Dyanmic-OCDMA using proposed sine functional code family and another two OCDMA systems, one is FFH and the other is SAC system using either Hadamard code, MQC code with $p \frac{1}{4} 13$ [2], or modified frequency hopping (MFH) code with $q \frac{1}{4} 16$ [3] are plotted in Fig. 2 for the sake of comparison. It shows the relation between the BER and the number of simultaneous active users when $P_r = -10\text{dBm}$. In our calculations, we take quantum efficiency 0.6, Spectral width 30 nm and filter bandwidth $BW = 0.165\text{ nm}$. In the simulation, the total numbers of users considered are $31 * 31 = 961$. The active no. of users considered is 100. The effective source power is fixed at $0.1 * 10^{-4}\text{ watts}$ (-20 dBm) & $0.1 * 10^{-5}\text{ watts}$.

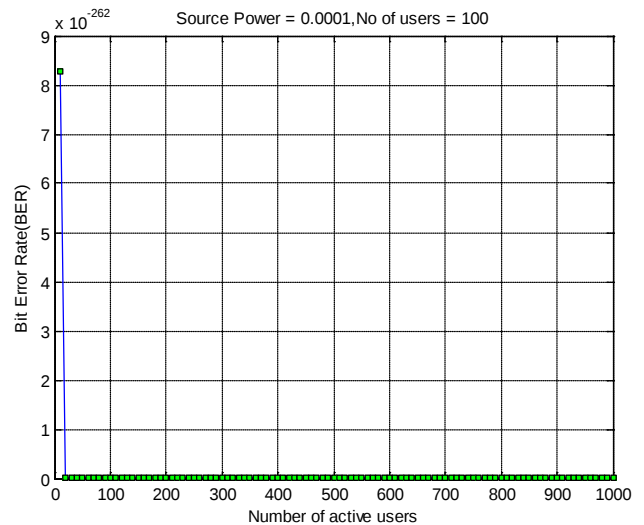


Fig. I : Comparison between BER & related users

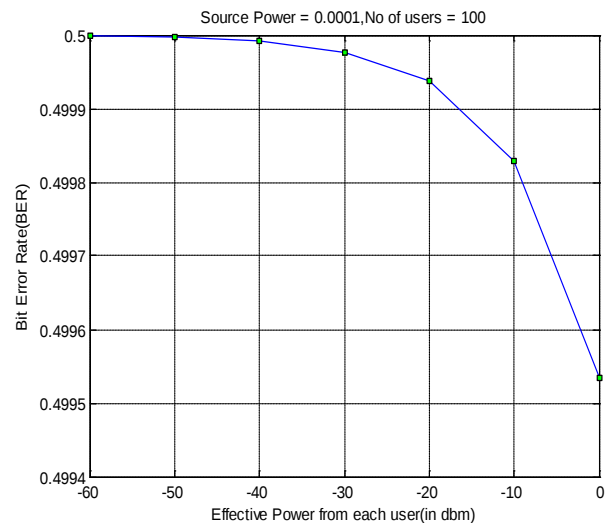


Fig. II : Comparison between BER & effective power

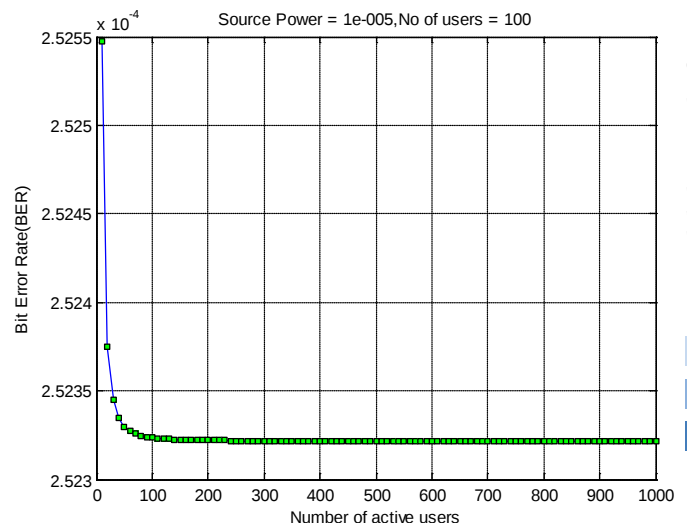


Fig. III : Comparison between BER & active users (100)

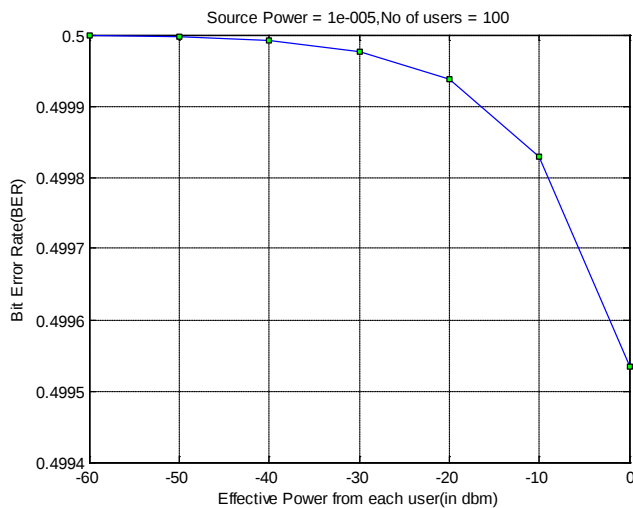


Fig. IV : Comparison between BER & Power from user

VII. CONCLUSION

We have planned a inventive low noise optical dynamic OCDMA communication system using a new two dimensional functional code. In transmitter side encoder used fast TOF & decoder design is based on fast TOF. The dynamically controlled of all filters and transfers one cycle through the data bit period. This encoder is simply reconfigured to some code by varying the electrical signal of the controller. The system is examined with a simple sine shifted functional code taking into account the MAI, the thermal noise, and the Phase Induced intensity Noise (PIIN). In these paper shows the comparison between BER with effective power from users & active users. In these system shows very small BER at large number of simultaneous active users compared with other systems like SAC and frequency hopping OCDMA systems. At 100 users, e.g., the system BER is improved. While in the dynamic OCDMA system, the data transmission rate is restricted by the tuneable filter's tuning speed, additional functional code relations can be used whereby the requirement for tuning speed can be reduced so that the system can support higher bit rates. The results show that the proposed DOCDMA system reduces the PIIN effect on the performance of the system and improves the bit error rate (BER) performance at a large number of users.

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A Multiband Free Space Antenna for High Bandwidth Wireless Applications

By M. A. Masud Khan, Md. Jobayer Hossain & Kawser Hossain

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Abstract - This paper presents a free space wire antenna having two larger bandwidths with satisfactory forward gain, return loss and VSWR. With center frequency 914MHz the antenna provides a bandwidth 174MHz from 880MHz to 1054MHz. Another band lies between 1478MHz and 1540MHz range with center frequency 1508MHz. These two larger bandwidths enable the antenna to support a wide range of wireless applications such as GPS, cellular communication, CT2, ZigBee, Wi-Fi and biomedical applications. The simulation of the antenna in 4NEC2 shows VSWR 1.08002, Return Loss -28.298dB and Gain 1.99dB. The characteristic impedance of the antenna is 49.7346 Ω without the use of any matching network. Both the simulation and experimental result shows that the antenna is omni-directional in nature.

Keywords : Wire antenna, Multiband antenna, VSWR, Return loss, gain, bluetooth, ZigBee, GPS, RFID, WiMAX.

GJRE-F Classification : FOR Code : 100510, 100502



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A Multiband Free Space Antenna for High Bandwidth Wireless Applications

Md. Jobayer Hossain^a, M. A. Masud Khan^σ & Kawser Hossain^ρ

Abstract - This paper presents a free space wire antenna having two larger bandwidths with satisfactory forward gain, return loss and VSWR. With center frequency 914MHz the antenna provides a bandwidth 174MHz from 880MHz to 1054MHz. Another band lies between 1478MHz and 1540MHz range with center frequency 1508MHz. These two larger bandwidths enable the antenna to support a wide range of wireless applications such as GPS, cellular communication, CT2, ZigBee, Wi-Fi and biomedical applications. The simulation of the antenna in 4NEC2 shows VSWR 1.08002, Return Loss -28.298dB and Gain 1.99dB. The characteristic impedance of the antenna is 49.7346 Ω without the use of any matching network. Both the simulation and experimental result shows that the antenna is omni-directional in nature.

Index Terms : Wire antenna, Multiband antenna, VSWR, Return loss, gain, bluetooth, ZigBee, GPS, RFID, WiMAX.

I. INTRODUCTION

Wire antennas [6] are the most common and simpler type of antenna. The antenna is generally made by copper or other metallic substances. A wire antenna may be a single piece or a combination of different pieces of variable length and radius. Whatever the types of antenna the use of it depends upon several characteristics such as VSWR, antenna gain, return loss, radiation characteristics etc.

Voltage Standing Wave Ratio (VSWR)[9] is a important term in describing the performance of an antenna. It is the ratio of the maximum to the minimum voltages along an antenna. Ideally it is desired that an antenna posses VSWR value 1 with all the power reaching the destination and no reflected power. But in practical case due to impedance mismatches in the antenna the VSWR deviates from this standard value. Again due to this power reflection from the destination to the source causes loss in signal power. This loss is called return loss [8]. Return loss is expected to be as smaller as possible. Antenna gain is another characteristic that indicates the ability to direct the input power into radiation in a particular direction.

The proposed antenna in the two specified bandwidths has VSWR 1.08002 and return loss - 28.298dB that is desirable for practical wireless communications. The gain of the antenna is 1.99dB that is also acceptable. A usual antenna system uses 50 Ω

transmission line. So the designed antenna should be matched with this vale to decrease return loss significantly. Our antenna provides characteristics impedance of 49.7346 Ω .

An antenna's bandwidth [7] is the range of frequencies over which its performance does not suffer from poor impedance matching. The higher the bandwidth of an antenna, the greater is the possibility to use it in different wireless applications. Sometimes an antenna operates over two or more frequency bands with satisfactory performances. Such type of antenna is called a multiband antenna [11]. The proposed antenna shows two bandwidths. Depending upon the allocated frequency band, an antenna can be used in different wireless applications. The wider the bandwidth, the higher is the usability of the antenna in wireless communication. The first band of this antenna provides a wide band of 174 MHz and the second one 62 MHz. Such wide frequency bands enables the antenna to be used in RFID, ZigBee, CT1, CT2, GPS, bluetooth and mobile communications.

Radio Frequency Identification or RFID [1], is a technology for automated identification of objects and people. This can operate in LF, HF and UHF in the 860-960 MHz range [3]. It is desirable the antenna size be smaller. The highest dimension of our antenna is 9cm. So it can be used to identify larger objects such as cars, ships and other types of vehicles. The antenna can also used for personal area network such as ZigBee[12]. It is a specification for high level communication protocols using small, low-power digital radios based on an IEEE 802 standard. Applications of it include wireless light switches, electrical meters with in-home-displays, and other consumer and industrial equipment that require short-range wireless transfer of data. The technology defined by the ZigBee specification is intended to be simpler and less expensive than other WPAN systems such as Bluetooth. The standard specifies operation in the unlicensed 2.4 GHz worldwide, 915 MHz in Americas and Australia and 868 MHz in Europe. Our antenna can be used to support this.

On the contrary, the antenna can be used in bluetooth communications. Today bluetooth wireless technology operates on an open frequency within the 914MHz band, which is the same cordless phones and various other wireless devices. Bluetooth is able to share the same frequency band without experiencing any interference because it utilizes various key

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technologies. It can also be used in cordless telephone version 1 and 2 with proper radiation and gain characteristics.

The wider frequency band of the antenna also enables to support space-based satellite navigation system GPS and Mobile communications. GPS [14] provides location and time information in all weather, anywhere on or near the Earth. The satellite communication for GPS comprises two frequencies i.e. uplink and downlink. These two frequency band lies in the second band of our antenna [13]. On the other hand the antenna can be used for widely adopted mobile communications. In mobile phone technology, there are two main transmission protocols. One is GSM and the other is CDMA. The Global System for Mobile Communication (GSM) is the dominant protocol used in India and most European countries. GSM phones use transmission frequencies of 890 - 915 MHz or 1710 - 1785 MHz for uplink (handset to base station) and 935 - 960 MHz or 1805 - 1880 MHz for downlink (base station to handset). The CDMA phones use frequencies of 824 - 849 MHz for uplink and 869 - 889 MHz for downlink. These frequency ranges lie in the first band of our antenna. So it can be used in mobile communication applications.

Nowadays, the wireless local area network (WLAN) and the worldwide interoperability for microwave access (WiMAX) systems are very popular techniques for wireless internet access. With the complementary capability between WLAN and WiMAX systems, seamless internet access for mobile users becomes possible. To cover WLAN and WiMAX operation, however, a wide operating band for the employed antenna in portable mobile devices is required. Having two larger bands, our antenna is very promising in providing a wide operating band with a compact antenna size.

II. ANTENNA GEOMETRY

The antenna is made of 12 gauge copper wire With all the pieces of same radius. The antenna structure is shown in figure 1. The longest dimension is 90mm that is along the main axis of the antenna. The total wire length required to construct the antenna is 310.06mm.

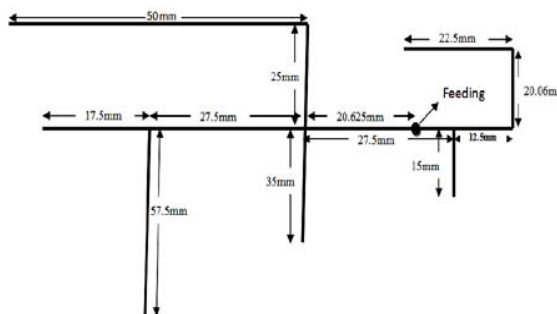


Fig 1 : Physical structure of the antenna for 914MHz

The antenna is assumed to be fed by 50 ohm coaxial cable with its central conductor connected to the feeding point. The feeding point is indicated in the figure.

III. SIMULATED AND EXPERIMENTAL RESULT

The antenna is designed and simulated in 4NEC2 software air interface. The analysis is done for radiation pattern, return loss, VSWR, impedance curve and forward gain.

a) Radiation Pattern

Radiation pattern [6] of an antenna is a graphical representation of the radiation properties of the antenna as a function of three dimensional space coordinate. The simulated radiation pattern of the antenna is shown in figure 2(a) and 2(b) for E (horizontal) and H (vertical) plane. The two figures for horizontal and vertical plane are almost identical. Figure 2(c) and 2(d) demonstrates the radiation pattern that was found in our experiment.

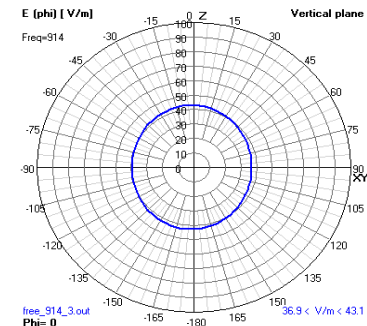


Fig 2(a) : Simulated Radiation pattern for E - Plane

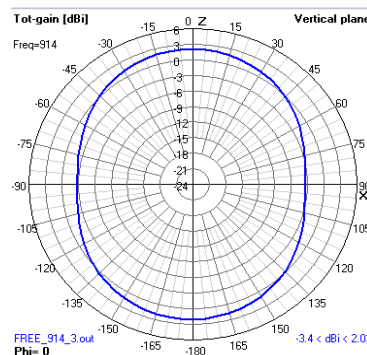


Fig 2(b) : Simulated Radiation pattern for H-plane

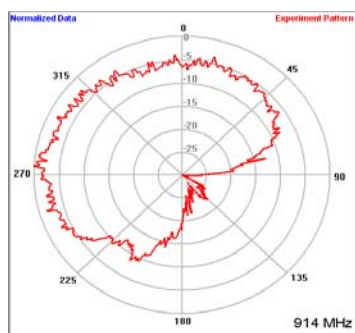


Fig 2(c) : Experimental radiation pattern for E-plane

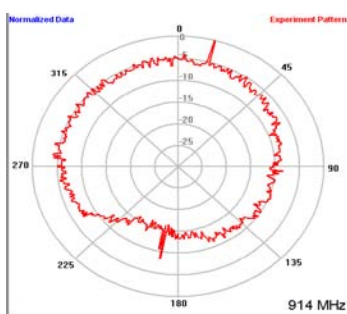


Fig 2(d) : Experimental radiation pattern for H-plane

The radiation patterns of the antenna are almost circular in two dimensional planes. It denotes that the antenna is omni-directional. So it can be used efficiently for a wireless communications.

b) VSWR

The voltage standing wave ratio of the antenna is depicted in figure 3 for different frequencies. From the curve we see that VSWR is almost 1 in three frequency bands. The VSWR values at the centre frequencies of these bands are given in Table 1. VSWR at these frequencies are very near to the ideal value.

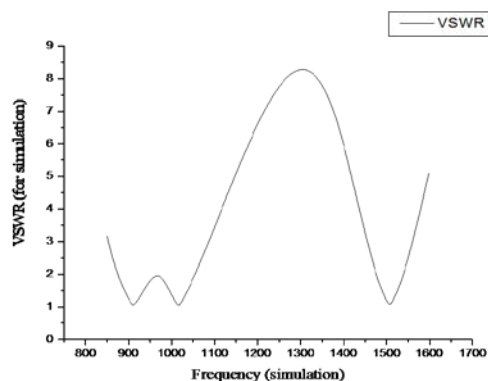


Fig 3 : Simulated VSWR curve

Table 1 : VSWR and Return Loss

Frequency (MHz)	VSWR	Return loss (dB)
914	1.08002	-28.298
1012	1.05894	-30.805
1506	1.07928	-28.373

Within frequency band from 880MHz to 1054MHz, $VSWR \leq 2$. So it can provide wideband applications sufficiently. Another band lies between 1478MHz and 1540MHz where VSWR is very near to 1. Here VSWR change is sharp. So it can also be used for narrowband applications.

c) Return Loss

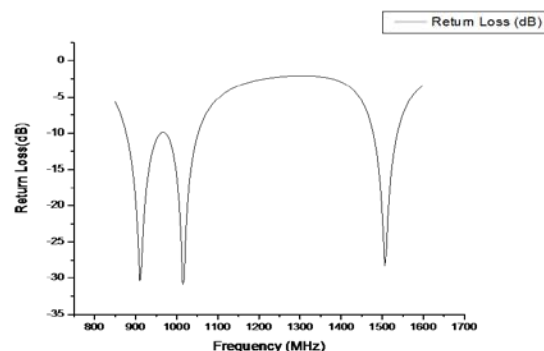


Fig 4 : Simulated Return loss Curve

The simulated return loss curve is demonstrated in figure 4. The lower the return loss the better the antenna and it provides lower loss. In the three bands return loss peaks touch -30 dB. This value is satisfactory to use in typical wireless applications.

d) Gain

The gain curves 5(a), 5(b) and 5(c) shows the variation in antenna gain for different directions and at different orientations. It may be noticed that horizontal gain equally varies with distance but vertical gain does not.

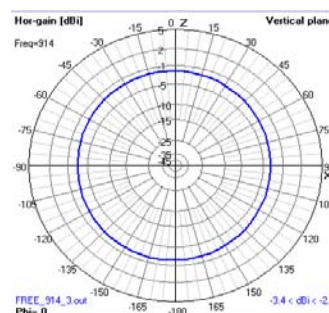


Fig. 5(a) : Simulated Radiation for Horizontal Gain

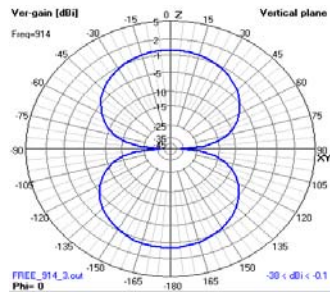


Fig. 5(b) : Simulated Radiation for Vertical Gain

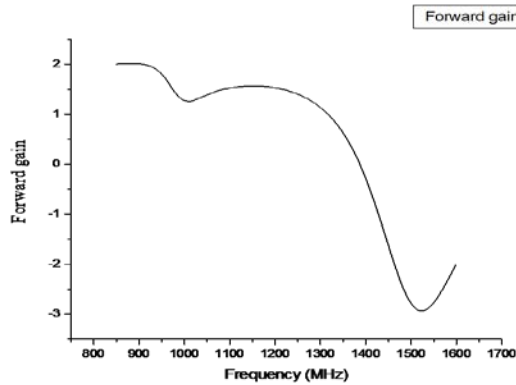


Fig 5(c) : Simulated forward gain

From the figures we see that forward gains in 914 MHz and 1012 MHz are 1.99 and 1.26 respectively. These values are satisfactory. But gain in third band is negative that is undesirable. It is not a major problem. This problem can be overcome using additional networks.

e) Impedance Curve

For maximum power transfer from transmitter to the antenna or from antenna to receiver, the antenna should be impedance matched.

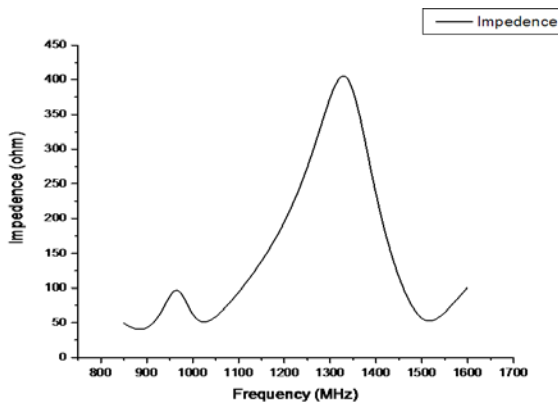


Fig 8 : Simulated impedance curve

The proposed antenna is designed for 50 Ω transmission line feeding. At the three bands, the antenna shows characteristics impedance almost the ideal value with negligible deviations. So there is no

need of a matching network while practically using them.

IV. CONCLUSION

A multiband wire antenna with wider bandwidth is designed, implemented and has been presented in this paper. The antenna provides three successive band of operating frequencies with excellent performance measures. Each of these band is wider enough to serve wider bandwidth requiring applications. In these bands the antenna shows satisfactory VSWR, return loss, gain, impedance and radiation properties. So the same antenna can support GPS, cellular communication, CT2, ZigBee, Wi-Fi, bluetooth and WiMAX applications. It does not require any additional matching network for feeding with 50 Ω transmission line or coaxial cables. In addition to this, the proposed antenna provides simple structure, thin profile and low cost. Therefore, it can be used in inexpensive communication applications with sufficient bandwidth and radiation properties.

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Dynamic Power Reduction in Modified Lifting Scheme Based DWT for Image Processing

By Prof. C. Chandrasekhar & Dr. S. Narayana Reddy

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Abstract - Image compression is one of the major applications in image processing that imposes greater design challenges for VLSI design engineers in design and development of low power and high speed architectures. DWT is used in image compression for transformation of image from spatial to frequency domain. In this paper, DWT architecture based on lifting scheme is considered and dynamic power reduction is achieved with suitable modifications to the architecture and adoption of low power techniques. The interdependency of scaling and dilation coefficients is simplified to single hierarchy and thus reduces latency and increases throughput. Wallace tree multiplier and carry select adder are used in realizing 1D DWT architecture. The hierarchy in the design enables to adopt multi-stage and hierarchical clock gating technique thus reducing dynamic power. Power gating and DVFS techniques are also adopted to optimize power dissipation.

Keywords : Dynamic power dissipation, DWT, Lifting Scheme, Hierarchical design, low power design ASIC implementation.

GJRE-F Classification : FOR Code : 080106



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Keywords : Dynamic power dissipation, DWT, Lifting Scheme, Hierarchical design, low power design ASIC implementation.

I. INTRODUCTION

DWT is recommended by JPEG2000 standards as it supports features like progressive transmission, higher compression and region of interest encoding schemes. Convolution based DWT or FIR filter bank based DWT architectures occupy large area as they require more number of multipliers and adders, thus making the computations complex and time consuming. Mobile phones and other similar hand held devices that support image/video applications demand high speed and low power architectures with reduced memory size for DWT processing. There are several architectures discussed in literature to perform lifting based DWT. General approach for 2-D DWT is to apply the 1-D DWT row-wise which produces L and H subbands and then process these sub-bands column-wise to get LL, LH, HL and HH coefficients. Several architectures like direct mapped [2], folded [3], and flipping [4] for single level and multi-level DWT have been proposed to implement 1-D lifting DWT. Many architectures that implement the Two-Dimensional

separable Forward (2D-DWT) and Inverse DWT (2D-IDWT) in order to be applied on 2D signals have been presented in the past [5], [6], [7] and [8]. These architectures are consisting of filters for performing the 1D-DWT and memory units for storing the results of the transformation. Due to the fact that streaming multimedia applications - in which the DWT is present - are characterized by high throughput requirements, this imposes the need for optimizing the design of the filters in terms of speed. Moreover, portable multimedia devices require low power consumption for increasing the battery lifetime and this can be achieved by minimizing the storage size and number of memory accesses [9]. Low power DWT architectures based on pipelining and parallel processing has been discussed in [10] and [11], in their work low power is achieved by modifying the architecture to reduce number of computations the design was implemented on FPGA. Many of the low power techniques reported in literature [12],[13], [14] and [15] for DWT propose modifications in the architecture level to reduce power dissipation. Power reduction can be accomplished at various levels of abstraction starting from architecture level to circuit level. Power reduction at the sub system level or at the circuit level can be accomplished when ASIC design of DWT architecture is performed. Many of the work reported in literature have restricted to FPGA implementation. In this paper, in order to demonstrate the dynamic power reduction techniques at various levels of abstraction, DWT architecture is considered as a test case for illustration. ASIC design of DWT architecture optimizing dynamic power reduction using 65nm TSMC libraries is performed.

Section II discusses wavelet transforms, DWT architecture and dynamic low power reduction techniques. Section III discusses proposed low power schemes for design DWT architecture sub systems. Section IV presents ASIC implementation of DWT architecture based on low power schemes. Section V discusses implementation results and performance comparison and section VI presents conclusion.

a) DWT and Low Power Schemes

In this section, DWT architecture and low power schemes are presented. Lifting scheme based DWT architecture is considered as test case for dynamic power reduction and is briefly discussed in this section. Major sources of power dissipation on VLSI circuits are also presented in this section.

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i. DWT architecture

In wavelet analysis, signals are represented using a set of basis functions derived by shifting and scaling a single prototype function, referred to as "mother wavelet", in time [16]. Wavelet transforms are closely related to tree structured digital filter banks and multiresolution analysis. A set of wavelet basis functions can be generated by translating and dilating the mother wavelet. A number of architectures have been proposed for calculation of DWT [2], [3], [4], [5] and [6]. The architectures are mostly folded and can be broadly

classified into serial architectures (where the inputs are supplied to the filters in a serial manner) and parallel architectures (where the inputs are supplied to the filters in a parallel manner). A methodology for implementing lifting-based DWT that reduces the memory requirements and communication between the processors, when the input is broken up into blocks is presented in [17]. Figure 1(a) and 1(b) shows the forward and inverse DWT based on lifting scheme architecture.

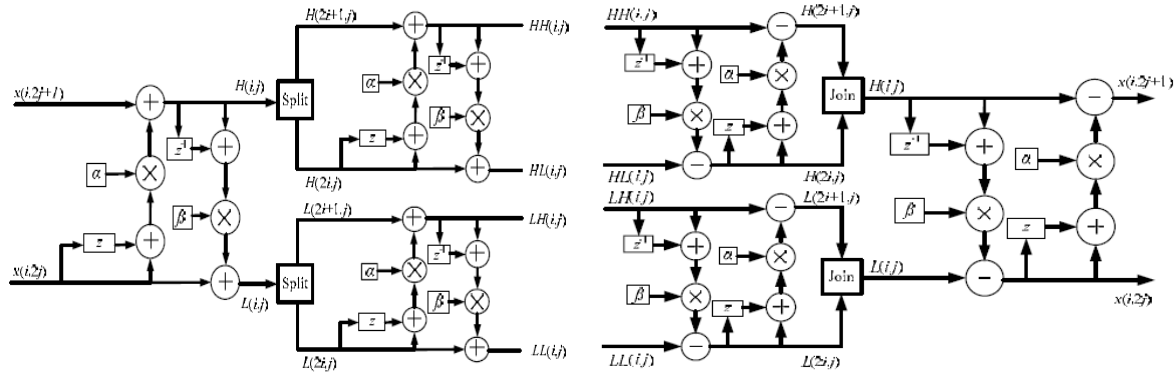


Figure 1 : Lifting based architecture (a) Forward DWT (b) Inverse DWT [17]

The z^{-1} blocks are for delay, $\alpha, \beta, \gamma, \delta, \zeta$ are the lifting coefficients and the shaded blocks are registers. 9/7 filter has been used for implementation which requires four steps for lifting and one step for scaling. The input signal x_i is split into two parts even part x_{2i} and odd part x_{2i+1} then the first step of lifting performed is given by the equations [17].

$$d_i^1 = \alpha (x_{2i} + x_{2i+2}) + x_{2i+1}$$

$$a_i^1 = \beta (d_i^1 + d_{i-1}^1) + x_{2i}$$

Then the second lifting step performed gives:

$$d_i^2 = \gamma (a_i^1 + a_{i+1}^1) + d_i^1$$

$$a_i^2 = \delta (d_i^2 + d_{i-1}^2) + a_i^1$$

Then scaling is performed and the following equations are obtained:

$$a_i = \zeta a_i^2$$

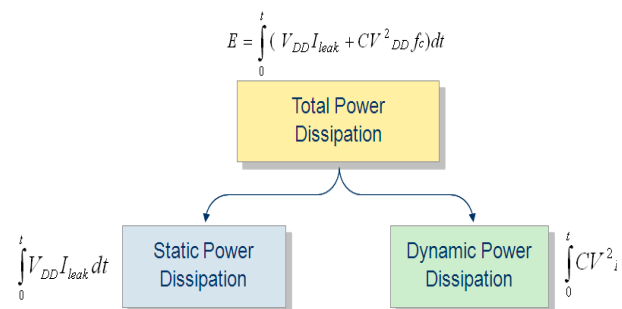
$$d_i = d_i^2 / \zeta$$

The predict step helps determine the correlation between the sets of data and predicts even data samples from odd. These samples are used in the update step for updating the present phase. Some of

the properties of the original input data can be maintained in the reduced set also by construction of a new operator using the update step. The lifting coefficients have constant values of -1.58613, -0.0529, 0.882911, 0.44350, -1.1496 for $\alpha, \beta, \gamma, \delta, \zeta$ respectively. a_i and d_i are DWT outputs after level 1 decomposition.

ii. Sources of power dissipation in CMOS VLSI circuits

Power consumption in CMOS digital circuits is divided into two major components (Static and Dynamic) as shown in Figure 2 (a).



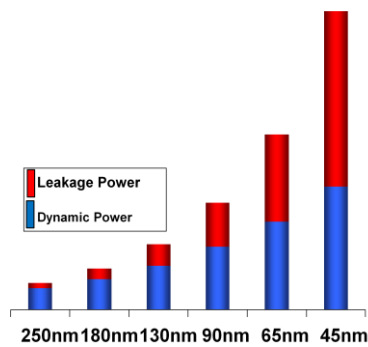


Figure 2 : nPower dissipation in CMOS circuits (a) Types of power dissipation (b) Power dissipation with technology scaling

Static power is due to leakage current and short circuit current, dynamic power is due to switching current. Power dissipation in CMOS is exponentially increased with scaling in transistor size. Figure 2(b) shows the power dissipation in CMOS with technology scaling. Dynamic power dissipation was dominating with 250nm technology, with technology scaling towards lower geometries (65nm and below), leakage power has significantly increased. However, dynamic power has also exponentially increased; this is due to the fact in increase in switching current and frequency of operation of CMOS circuits. There are various low power reduction techniques such as [18]:

- (a) Reducing voltage for lower performance blocks,
- (b) Cut off of power on blocks when they are not required
- (c) Combination of MV and/or Power Gating (shutdown), optionally retaining state on shutdown block
- (d) Lower voltage when blocks not needed, but leave them powered enough to save state w/o extra retention overhead.
- (e) Vary the voltage and/or frequency dynamically, adaptively on-the-fly, depending on immediate performance/power requirement.
- (f) Vary the well voltage to adjust threshold voltage, which in turn increases speed (forward bias) / reduces leakage (backward bias). Also known as Variable V_{th}
- (g) Reduce gate lengths in transistors along the non-critical paths
- (h) Source biasing, push the transistor to operate in cut-off region by increasing the source ground potential
- (i) Isolation/level shifting bugs, control sequencing bugs, retention scheme/control errors, Retention selection errors
- (j) Electrical problems like memory corruption hardware-software deadlock

- (k) Power gating failure/dysfunction, power-on-reset/bring-up problems, power sequencing/voltage scheduling errors

Power reduction techniques mentioned above are to be applied to the DWT architecture to optimize for low power. The major building blocks in DWT and IDWT as shown in Figure 2 are the adders, multipliers, registers and control unit for data flow control. As the focus of this work is to reduce power dissipation at various levels of abstraction, adders and multipliers are designed with low power techniques.

II. SUBSYSTEM DESIGNS FOR DWT ARCHITECTURE

An adder is the most commonly used arithmetic block in the Central Processing Unit (CPU) of a microprocessor, a Digital Signal Processor (DSP), and even in a variety of ASICs. In a DWT processor, adder is one of the important building blocks, required to compute the DWT coefficients of input signal. Multiplier used in a DWT processor also requires adder to add the partial products. Hence, design and analysis of adder is considered in this section. Speed and optimization of power of an adder is significant, to improve the overall performance of the system. But an adder also experiences the power-delay trade off. That is, its power dissipation increases with reduction in delay and vice versa. There are various architectures for adder design. 4-bit adders can be of different types. Some of those are Carry look Ahead Adder, Ripple Carry Adder, Carry Save Adder, Carry Select Adder. In many digital signal processing operations-such as correlations, convolutions, filtering, and frequency analysis-one needs to perform multiplication. Multiplication algorithms will be used to illustrate methods of designing different cells so that they fit into a larger structure. In order to introduce these designs, simple and serial and parallel multipliers will be introduced. High-speed parallel multipliers are becoming one of the keys in RISCs (Reduced Instruction Set Computers), DSPs (Digital Signal Processors), and graphics accelerators and so on. Parallel multipliers are used in data processor as well as in digital signal processors. There are various multiplier architectures reported in literature, Wallace tree, booths multiplier, BZ-FAD multiplier, Shift and Add multiplier and Array multiplier are most popular for DSP applications. In this work, the adders and multipliers are modeled using HDL and is synthesized using TSMC 65nm CMOS libraries using Synopsys DC. The synthesis results generate reports that provide information on area, delay and power dissipation. The results obtained are presented in table 1 and table 2 is without low power techniques. Multipliers are designed using carry save adders.

Table 1 : Full Adder Design Comparisons

Type of adder (16-bit)	No. of transistors	Power - μ W	Delay -ps
Ripple carry adders	286	40.5505	600
Carry save adder	92	18.9241	74
Carry select adder	102	16.897	65
Carry look ahead adder	621	55.1482	62

Table 2 : Power comparison of multipliers

Multipliers	Total Dynamic power (uW)	Cell Leakage power(uW)
BZ-FAD Multiplier	161.27	5.32
Shift and Add Multiplier	241.14	4.71
Booth Multiplier	468.02	12.69
Array Multiplier	298.83	10.24
Wallace Tree Multiplier	341.62	13.81

In order to reduce power dissipation of adder and multiplier, multi VDD technique is adopted. Reducing VDD supply voltage, reduce the power consumption, there will be no effect on area. From the results obtained it is found that power consumption is a quadratic function of voltage ($\text{Power} = f(V_{DD}^2)$). Decrease in supply voltage increases the overall delay ($\text{Delay} = (KV_{DD}/V_{DD} - V_t)^{\alpha}$).

The synthesis results generate reports that provide information on area, delay and power dissipation. The results obtained are presented in table 1 and table 2 is without low power techniques. Multipliers are designed using carry save adders.

Table 3 : Reduction in dynamic power with voltage scaling

Voltage	Dynamic Power (uW)	Delay (ns)
1.8	341.62	1.76
1.5	156.12	1.934
1.2	82.61	2.34
1	41.29	3.99

Forward DWT and inverse DWT architecture are realized using carry save adder and Wallace tree multiplier due to its delay. Voltage scaling significantly

reduce power dissipation, however, delay increases. Thus in this work, a trade-off between power and delay is considered and thus the power supply voltage is chosen to 1.2V, thus the multiplier constitutes a delay of 2.34ns and carry save adder has a delay of 112 ps. The multipliers and adders with scaled operating voltages are adopted in design of a modified DWT architecture, to demonstrate the importance of architectural modifications leading to low power. Next section discusses low power techniques addressed at architectural level.

a) Modified lifting based DWT architecture for low power

Lifting equations presented in (1) – (6) when realized using HDL model is a sequential process, as the scaling factors and are dependent on previous samples, thus introducing latency. In order to increase throughput and latency modified equation are derived. The modified lifting equations eliminate dependency of outputs on previous samples. We have obtained the equations for a_i and d_i by substituting (4) in (3), (3) in (2) and so on. The lifting coefficients were substituted and the results were scaled by multiplying with 256 to avoid decimal and to round off the values. The modified lifting scheme equations are:

- $$a_i = 294 * (8(6 * x_{2i} + 4 * x_{2i-2} + x_{2i} + 4 * x_{2i+4} + x_{2i-4} + 4 * x_{2i+2}) - 5 * (3 * x_{2i+1} + x_{2i+3} + x_{2i+3} + 3 * x_{2i-1}) + 100 * (2 * x_{2i} + x_{2i+2} + x_{2i+2}) - 180 * (2 * x_{2i} + x_{2i+2} + x_{2i+2}) + 113 * (x_{2i+1} + x_{2i+1}) + 21 * (2 * x_{2i} + x_{2i+2} + x_{2i+2}) - 13 * (x_{2i+1} + x_{2i+1} + x_{2i-1}))$$
- $$d_i = 19 * (3 * x_{2i+3} * x_{2i+2} + x_{2i+4} + x_{2i-2}) + (-12) * (2 * x_{2i+1} + x_{2i-1} + x_{2i+3}) + 226 * (x_{2i} + x_{2i+2}) - 406 * (x_{2i} + x_{2i+2}) + x_{2i+1}$$

These equations are obtained by taking coefficients as common. The equations have initial latency, as the input samples need to be stored before DWT a_i and d_i coefficients computations.

The design of low power architecture to reduce dynamic power dissipation is based on equations (7) and (8). From the equation the following are the observations made:

- a_i and d_i coefficients are computed based on input samples and lifting coefficients. Every output sample depends upon x_0 to x_4 input samples. Input samples are multiplied by coefficients as per the equations.
- Common factors are identified between a_i and d_i equations and these common functions are realized once and are reused to reduce the circuit complexity.
- Lifting coefficients are stored in memory and are retrieved only once and used for computation of a_i and d_i components.
- Pipelined architecture is developed to realize a_i and d_i equations.

The proposed architecture shown in Figure 4 takes two inputs and gives two outputs per cycle. Data1 and Data2 are the odd and even input samples given to hardware in single clock for 100 % hardware utilization. This architecture is very simple design as compared to

other architectures suggested in [20] which have complex control path to achieve 100% hardware utilization. The row processor and column processor shown in figure 4 are realized using modified lifting scheme based equations.

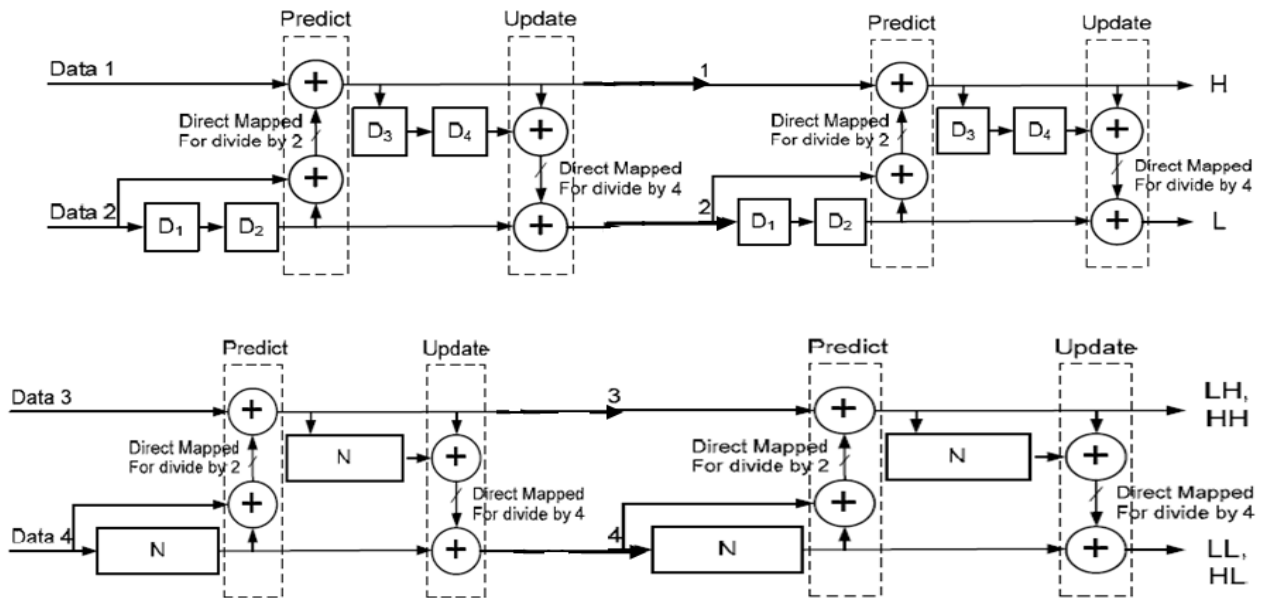


Figure 3 : Row processor and column processor for modified lifting DWT

Based on the architecture shown in figure 3 and equations presented in (7) and (8), the top level model for the architecture is shown in figure 4. A detailed data flow for the proposed architecture is presented in the figure 4.

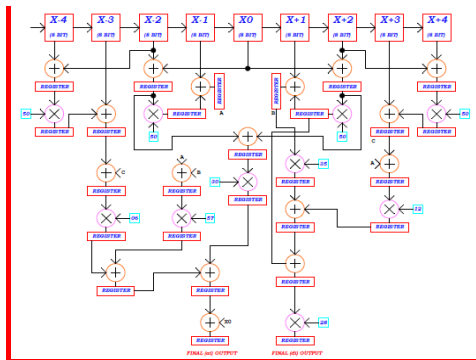


Figure 4 : Modified lifting scheme architecture to reduce dynamic power

The modified architecture derived consists of the following blocks: parallel input and serial output register, serial input and parallel output register, Multiplier and adders and control unit. The HDL model is developed and the design is verified for its functionality using test bench in ModelSim. The functionally correct HDL code is synthesized using Synopsys DC targeting TSMC 65 nm library and technology files. The reports obtained are compiled and presented in table 4.

Table 4 : ASIC synthesis results of modified lifting based DWT

Parameters	Reference [19]	Modified lifting based DWT
Area (sq.mm)	21984.657462	29542.89061
Power (μ W)	962.9536	604.712
Operating frequency (max) MHz	212	278

From the results obtained and tabulated in Table 4, it is found that due to changes in architecture that reduces number of stages in DWT computation, the dynamic power dissipation is reduced by 37%. However, the area is increased due to increase in registers and intermediate storage units, the design is synthesized to obtain minimum delay and zero slack requirement. Due to architectural changes it is demonstrated that dynamic power is reduced by 37%. In order to further reduce power dissipation various other dynamic low power techniques are introduced for optimization.

b) Dynamic low power reduction techniques

There is various dynamic low power techniques that have been recommend by synthesis tools like Design Compiler. In this work, Synopsys DC supporting low power design library is chosen for low power implementation. The low power techniques adopted for ASIC implementation of modified lifting based DWT architecture are: clock gating techniques, power gating technique, device sizing, logic restructuring, balanced delay paths to reduce glitch and Dynamic Voltage and Frequency Scaling (DVS, DFS).

i. Dynamic power reduction techniques for modified lifting based DWT

The simplest, general (or automatic) clock gating inserts a single clock gate for each register bank. Most tools permit the user "split" register banks or to prevent clock gate "sharing" across unrelated register banks. To save even more dynamic power, advanced clock gating styles such as multi-stage and hierarchical can be used, depending on design architecture and design requirements. The modified lifting DWT have common coefficients and thus need to be enabling at different instants of time and hence multi-stage clock gating technique is implemented. The 2D DWT architecture is realized using sub systems (multipliers, adders and registers), 1D DWT and finally 2D DWT, in order to reduce power dissipation hierarchical clock

gating technique is adopted. Figure 5 shows the multi-stage clock gating technique introduced into the row processor. Enable adder enables all adders together, similarly the enable reg enables all intermediate registers, thus saving power.

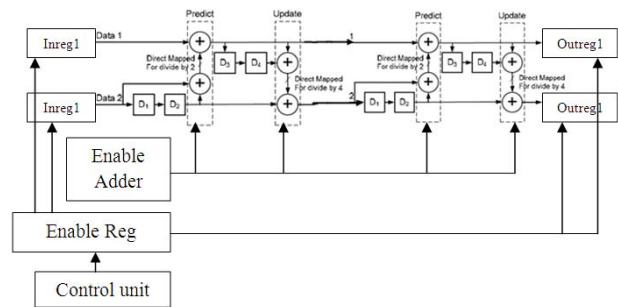


Figure 5 : Multi-stage clock gating technique on modified DWT

Figure 6 shows the block diagram of 2D DWT based on modified lifting scheme. 1D DWT is used in the first stage as well as the second stage. The first stage performs DWT on row and second level performs DWT on column data. Every 1D DWT have internal control logic that executes multi-gate clock gating technique. In the top module, hierarchical clock gating technique is adopted to reduce dynamic power dissipation.

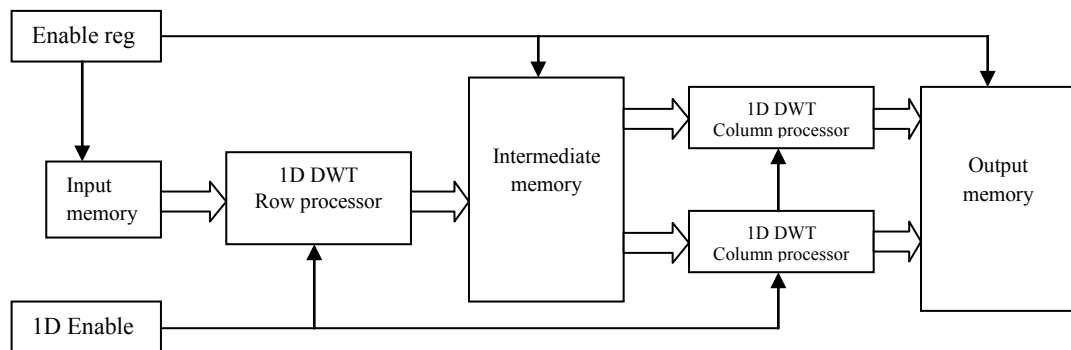


Figure 6 : Hierarchical clock gating for 2D DWT

In order to implement power gating technique power gates and state retention register required. Power gating cells are required for turning blocks on and off. State retention registers in their turn are useful because, if the state of a shut down or "sleeping" block needs to be retained the most automated method to retain the state is the use of retention registers. These registers have a backup power supply connection that remains always on to hold the state of the register via a high voltage threshold latch built into the register. An isolation cell is required to ensure electrical and logical isolation

of logic that is shut down from active logic in a design. The reason this is required is because when a block is shut down the internal signal level will transition to an unknown, floating state. Also always on cells are required between switched and steady state blocks to ensuring interoperability. Figure 7 shows the power gating logic for dynamic power reduction. Multiple voltages are used to drive the cells that are active or in standby. In the hierarchical design shown in Figure 6, 1D DWT are active during computation and inactive during data storage, thus power gating techniques are

inserted. The most common approach to provide state retention during power gating is to replace a standard register with a retention register.

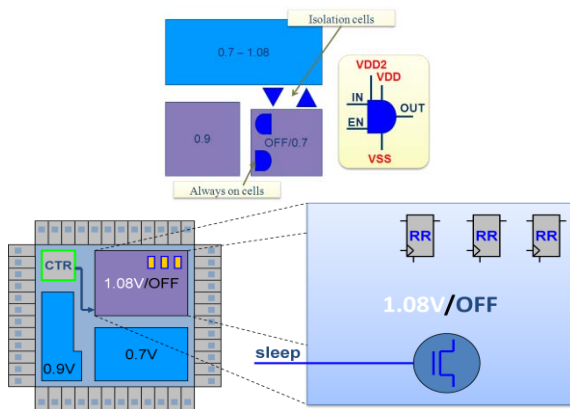


Figure 7 : Power gating techniques for modified DWT

As the modified lifting is hierarchical in nature and consists of multiple parallel data paths, power gating is easily implemented. Glitching is due to a mismatch in the path lengths in the logic network. If all input signals of a gate change simultaneously, no glitching occurs. Critical path is estimated based on synthesis report, the critical paths identified are manually observed, if they introduce any glitches. Based on the observations made, multiple critical paths that are in parallel are identified having mismatch in path lengths, thus intermediate registers are introduced at eh inputs and outputs of DWT architecture to introduce equal delay, thus reducing glitches. The fan-out out constrain is set to 4 to obtain reduced number of critical paths.

To achieve further improvements in power reduction without resorting to custom circuit techniques, Dynamic Voltage and Frequency Scaling can be used. Dynamic Voltage and Frequency Scaling is effective because of the following two facts:

- The amount of energy required to complete a task is proportional to the square of the supply voltage.
- The maximum frequency of any CMOS circuit is proportional to the supply voltage.

So if the supply voltage is decreased there is a square-law reduction in energy to complete a given task. However the task takes longer to complete because of the linear reduction in frequency. Therefore, the principle gain with Dynamic Voltage and Frequency Scaling is with respect to dynamic power consumption.

Dynamic voltage and frequency scaling adjusts performance and energy consumption levels while the logic circuit is active. It is required to reduce processor frequency and voltage to obtain quadratic energy savings. DVFS is an effective way of reducing the CPU energy consumption by providing computation power.

DVFS technique has been proven to be a highly effective technique for power minimization subject to a performance constraint. DVFS should consider not only the CPU power, but also the total system power dissipation. In this work, to realize 2D DWT, multiple 1D DWT architecture is realized using modified lifting scheme logic. Thus DVFS is adopted to minimize power dissipation.

DVFS computation for modified lifting DWT: Workload of a task, W_{task} , is defined as the total number of clock cycles required to compute 1D DWT.

$$W_{task} = \sum_{i=1}^n CPI_i$$

n: total number of iterations in DWT, CPI: clock cycles per DWT coefficient computation. The maximum value of n is 7 as there are 7 different partial factors to be added in computing a_i . Each computation of partial product requires 4 clocks, as there are multipliers and adders. The task execution time, T_{task} , is a function of DWT processor frequency, f_{DWTpf}

$$T_{task} = \frac{W_{task}}{f_{DWTpf}}$$

To save DWTpf energy using DVFS for a given deadline D, choosing a f_{DWTpf} , at which T_{task} can be closest to D.

$$T_{task} = D, \quad f_{DWTpf} = \frac{W_{task}}{D}$$

From the first cut synthesis results obtained, f_{DWTpf} is 290MHz. All the above discussed dynamic low power techniques have been included in the constrains file to minimize power dissipation.

III. ASIC IMPLEMENTATION AND RESULT ANALYSIS

The simulation results for modified DWT are presented in this section. There are sixty four inputs, each having bit width of twenty bits. These inputs are serially sent to the DWT architecture. The DWT consists of registers, multiplexer, adder and multiplier. Whenever the inputs are sent through SIPO (serial input parallel output), the data has been divided into even data and odd data. The even data and odd data are stored in the temporary registers. When the reset is high, the temporary register value consists of zero, whenever the reset is low, the input data is split into the even data and odd data. The input data is read up to sixty four clock cycles, after that the data read according to the lifting scheme. The output data consists of low pass and high pass elements. This is the 1-D discrete wavelet

transform. The two level discrete wavelet transform is that the low pass and the high pass filter outputs are again divided into LL, LH and HH, HL. The output is verified in the VCS. Figure 8 shows the VCS simulation results of DWT.

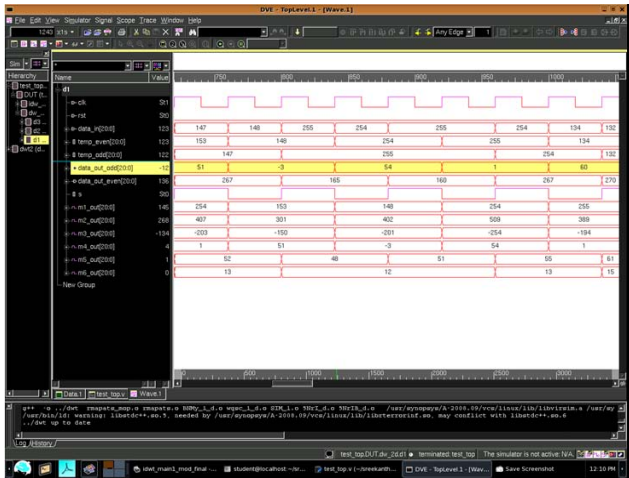


Figure 8 : 1-D Discrete Wavelet Transform output waveform in VCS

From the simulation results obtained the logic correctness is verified and the HDL model is synthesized for low power optimization. The low power design flow adopted in this work is shown in figure 9. Low Power design techniques have their impact on libraries, because in order to implement these techniques special cells (high-Vth MTCMOS power switches, isolation cells, level shifters, retention registers and Always-On buffers) are required in addition to the basic cells already included in digital standard cell libraries.

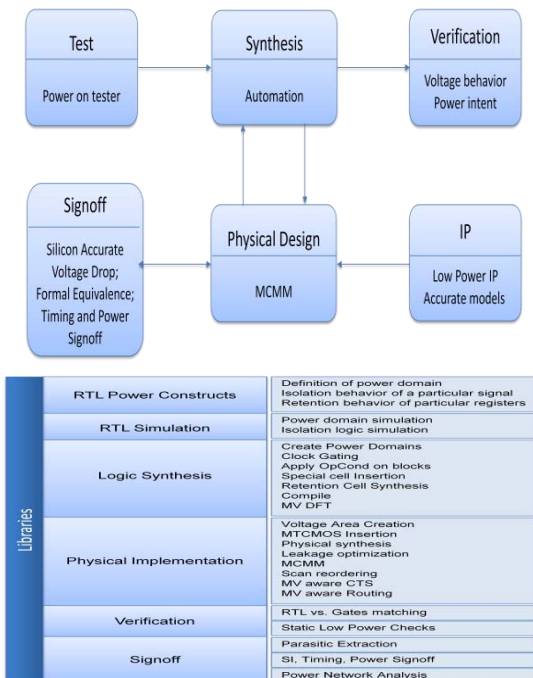


Figure 9 : Low power design flow

IV. IMPLEMENTATION RESULTS AND DISCUSSION

In this work, ASIC design flow is restricted to synthesis only for the modified lifting DWT, thus low power libraries and low power IPS from Synopsys design ware are adopted for synthesis. The synthesis constraint file is set for low power synthesis, the Synopsys DC constraints are:

```
create_power_domain TOP
create_power_domain GPRS -elements GPRS
create_supply_port VDD
create_supply_net VDD -domain TOP
create_supply_net VDD -domain GPRS -reuse
connect_supply_net VDD -ports VDD
create_supply_port VSS
create_supply_net VSS -domain TOP
create_supply_net VSS -domain GPRS -reuse
connect_supply_net VSS -ports VSS
create_supply_net VDDGS -domain GPRS
set_domain_supply_net TOP \
    -primary_power_net VDD \
    -primary_ground_net VSS
set_domain_supply_net GPRS \
    -primary_power_net VDDGS \
    -primary_ground_net VSS
create_power_switch gprs_sw \
    -domain GPRS \
    -input_supply_port {in VDD} \
    -output_supply_port {out VDDGS} \
    -control_port {gprs_sd}
    -applies_to outputs
```

```
set_isolation_control gprs_iso_out \
    -domain GPRS \
    -isolation_signal PwrCtrl/gprs_iso \
    -isolation_sense low \
    -location parent
PwrCtrl/gprs_sd \
    -on_state {state2002 in {gprs_sd}}
set_isolation gprs_iso_out \
    -domain GPRS \
    -isolation_power_net VDD \
    -isolation_ground_net VSS \
    -clamp_value 1 \
set_retention gprs_ret -domain GPRS \
    -retention_power_net VDDGS \
    -retention_ground_net VSS
set_retention_control gprs_ret \
    -domain GPRS \
    -save_signal {PwrCtrl/gprs_restore low} \
    -restore_signal {PwrCtrl/gprs_restore high}
map_retention_cell gprs_ret -domain GPRS -lib_cells
RDFFNX1
add_port_state VDD
    -state {HV 1.2}
add_pst_state sleep -pst chiptop_pst -state {HV OFF}
```

The constraints are set according to the command set in the file above. The low power constraints are supported only if the RTL is hierarchical and is parallel in nature. The constraints file is shown in below. The constraints for dynamic power reduction discussed earlier are set in a constraints file and are used for synthesis. The TCL scripts for DWT_TOP_MODULE are presented below and are used for synthesis.

#Reading design

```
analyze -library WORK -format verilog
{./RTL/top_DWTpf.v ./RTL/1ddwt.v
./RTL/power_controller.v}
read_file -format verilog {./RTL/top_DWTpf.v}
name_format \
```

```
-isolation_prefix "ISO_"
```

```
-level_shift_prefix "LS_"
```

#Reading UPF

```
source ./inputs/chiptop+.upf
```

#Setting voltages and options

```
set_voltage 1.2 -obj {VDD VDDGS}
```

```
set_voltage 0.000 -obj {VSS}
```

```
set auto_insert_level_shifters_on_clocks all
```

```
set_dont_touch [get_nets Ovfl]
```

```
set_dont_use saed65nm_typ_ht/AODFF*
```

```
set_dont_use saed65nm_max/AODFF*
```

```
set_dont_use saed65nm_min/AODFF*
```

#Reading constraints

```
source ./inputs/chiptop+_s0.sdc
```

#Compiling

```
compile
```

#Writing out results

```
change_names -rule verilog -hier
```

```
write -f verilog
```

```
-h -out ./results/compile.v
```

```
write -f ddc
```

```
-h -out ./results/compile.ddc
```

```
save_upf ./results/compile.upf
```

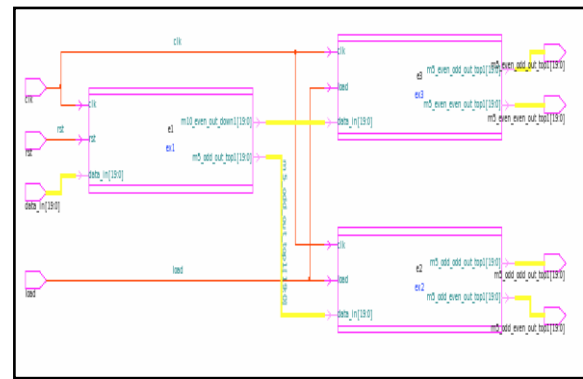


Figure 10 : Modified DWT synthesized netlist

Figure 10 shows the synthesis netlist obtained using 65nm technology and the interconnections used in the design along with clock tree network. Figure 11 shows the synthesized netlist along with clock tree network.

RTL model developed for the modified lifting scheme based DWT architecture is remodeled for ASIC implementation. The design is synthesized using Design Compiler and timing analysis is carried out using Prime Time. The design requires 42 input-output ports and requires 550 cells. The total combinational area is 21527.410 sq umm and non-combinational area is 10256.23 sq umm. Total dynamic power is 498.3µW. Due to the low power techniques adopted the dynamic power dissipation is reduced by 19%. From the results obtained, design of architecture achieves 37% power reduction; low power techniques presented in this section reduces power dissipation by 17%. Thus maximum power dissipation is achieved at the architecture abstract level.

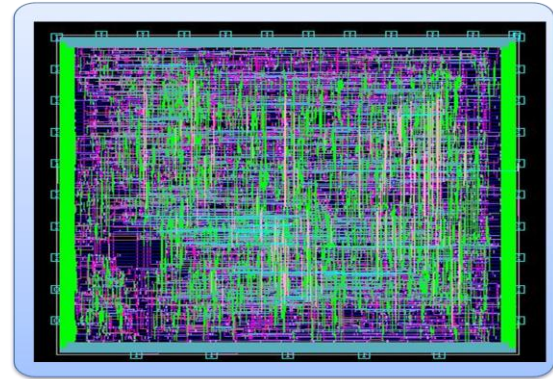
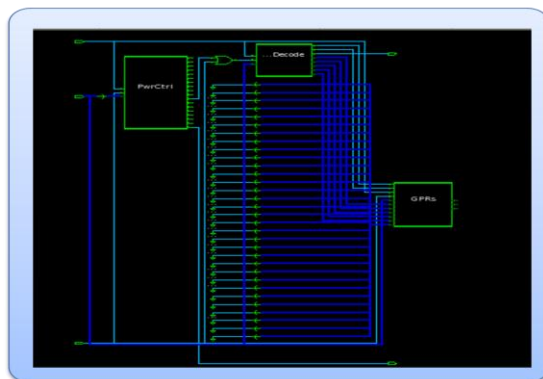


Figure 11 : Synthesized netlist of modified DWT and clock tree network

Table 5 : Dynamic power reduction comparison

Parameters	Modified lifting based DWT	Modified lifting based DWT with low power
Area (sq.mm)	29542.89061	31783.64
Power (μ W)	604.712	489.36
Operating frequency (max) MHz	278	290

DWT architecture is considered as a case study to analyze the power dissipation factor in VLSI circuits. Power saving achieved at various levels of hierarchy is proven in this work. Starting from architecture level to circuit level, power reduction need to be performed and is illustrated in this work.

V. CONCLUSION

In this work, a modified lifting based DWT is proposed, designed and implemented using 64nm TSMC low power design library. Lifting based DWT is considered to illustrate the techniques that can be adopted to reduce dynamic power. Modification in the architecture level as well as at different abstraction levels are considered for power reduction. Low power library cells from Synopsys design ware are considered for synthesis. TCL scripts for constraining the design for various dynamic power dissipation are developed. The RTL model developed is synthesized and performances are estimated. From the results obtained it is found that there is a total of 50% power reduction as compared with direct implementation. The developed low power techniques can be adopted to other complex designs. Further power dissipation can be reduced at the physical design stage.

VI. ACKNOWLEDGEMENT

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Design, Development and Performance Study of L³- Home Security System

By B V Sumangala & K Bhargava Ram

Dr. Ambedkar Institute of Technology

Abstract - All over the world, security has been a major concern in every home. Here, a security system has been developed that uses sensors to detect any security violation and sends out the alert signal by high intensity Buzzer. The system mainly consists of LDR, Laser, Logic Gates, Microcontroller IC, LCD, Keypad and Relay Circuit. L³ stands for LDR, Laser and Logic Gates as these 3 components form the core idea of the system. This system is mainly implemented on the present doors with lock-key method. Thus providing Double Authentication i.e. the door can only be opened with the right password and right key. Another feature of the system being that, using different logic gates combination the system is designed in such a way that the buzzer won't be switched off even though the intruder cuts the wires connecting the Buzzer and main control circuit. The system is designed and developed using simple locally available components and by considering every tiny factor it is made both reliable and affordable. Performance and cost analysis studies are also carried and also a glance into the future upgradations such as SMS service, PIR sensors and IR sensors that be introduced in the system.

Keywords : Microcontroller, Sensors, LCD, Logic Gates, Laser.

GJRE-F Classification : FOR Code : 020502, 090601



Strictly as per the compliance and regulations of:



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I. INTRODUCTION

a) Home Automation

In simple terms home automation is defined as the automatic control of all appliances at home. It's something like this: when you get up from bed, the pressure sensor kept under your bed mat sends the signal to the coffee maker which makes the coffee and heater in your bathroom switches on simultaneously^[1]. Lights and fans switch ON and OFF based on the humans presence in the room all by itself. These technologies are no more the dream but are now becoming the reality around us.

Home Security Automation: Non-Automated security systems were found non-reliable. Doors were fitted with lock and key system which can be opened easily. Even the human presence of security guard may not be completely trustworthy. Every system from the past has been found to be very much vulnerable. Home is a place where security is must, to keep all the valuables and appliances safe. The owner should have the confidence to step out of the house with the feel that

nothing can happen to the Home. This feel will only arise when the home is equipped with a reliable security system.

How: This reliable home security system can be made possible with Home Security Automations. Over the years many systems are being designed for this purpose. Password Authentications like the ATMs, which are equipped with RFID or Biometric System and Cameras with image processing, Zigbee based security system, PIC based security system, SMS based security system etc. has been designed and implemented^[2].

But the cost of the systems is relatively high, thus making it available to the only to the rich.

With this issue in focus, we tried to design a home security system which will be of low cost and provide adequate security levels for the home, thus making it reliable and affordable to every class of families.

II. BLOCK DIAGRAM

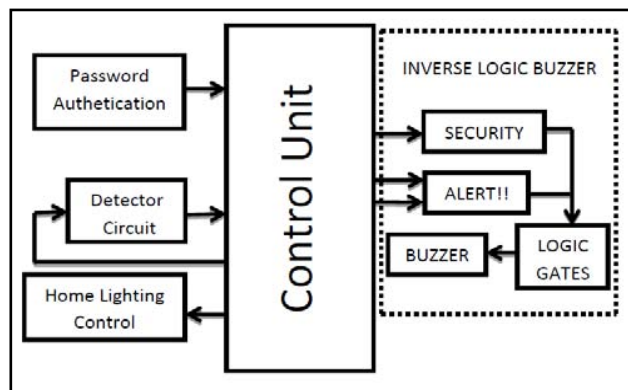


Figure 1 : Block Diagram Representation of the Security System

III. SYSTEM OVERVIEW

a) Control Unit

32 pins AT89V51RD2 Microcontroller is the control unit in the security system with a crystal oscillator to set accurate 12 MHz frequency. The microcontroller is programmed using C language.

b) Password Authentication

i. Components Description

- 1) **LCD – KEYPAD:** LM016 2 lines LCD (Liquid Crystal Display) in combination with 4X3 Keypad

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is used to enter password and verifications^[3]. LCD is used mainly to provide better user interfacing, such as to display "Enter Password:", "Home Lighting (Y/N)", "ALARM ON" etc.

- 2) **EEPROM:** A Parallel 16K (2Kx8) EEPROM^[4] (Electrically Erasable Programmable Read Only Memory) is provided as an external memory. EEPROM is used to store the password and is again accessed when a password has to be changed.

[Note: A series EEPROM can also be used in this application. To decrease the programming complexity Parallel EEPROM is selected]

The Password Authentication provides a secured gateway to enter the home. The owner activates/deactivates the security system by entering the password. When security system is switched ON, simultaneously the Detector Circuit, Inverse Logic Buzzer and Home Lighting Control inputs varies based on its mode of operation.

c) Detector Circuit

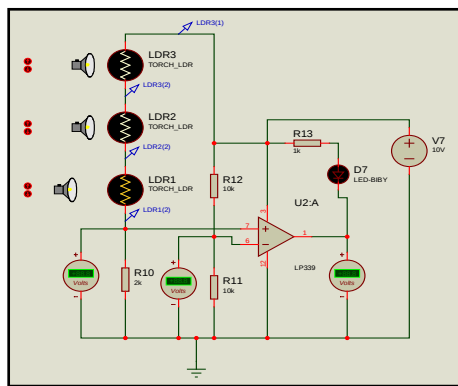


Figure 2 : Circuit Connection of Detector Circuit

Detector Circuit is placed behind the main door whereas the Password Authentication system is at the front as shown in the figure 2. The detector circuit is a combination of LDR (Light Dependent Resistor) and Laser. The LDR has the property of possessing a high resistance in the range of Kilo to Mega ohms in normal condition^[5]. When a high intensity light is incident on the LDR, the resistance drops to 300-400 ohms. In the circuit, there is a 10V DC supply along with two potential dividers (R11, R12) and R10, LDR resistance. Due to the R11 and R12 potential divider, the voltage drop across R11 is 5 volts providing 5 volts to the negative terminal of the LP339 comparator^[6]. Once the home security is switched ON, the LDR LASER circuit will get activated. This means that the laser light will be incident on the light dependent resistor. As the laser light is incident on the LDR, its resistance is lower than R10 creating a drop such that the voltage available at the positive terminal of the comparator is higher than the voltage at the negative terminal. Hence the comparator output will be high and

LED will not glow. If the laser light is switched off or cut due to some obstruction, the LDR resistance will increase. Hence the drop across it will increase producing a lower voltage at the positive terminal. As a result, the comparator output will be low and the LED starts glowing indicating that someone has disturbed the sensor system. The output of comparator is connected to port of the microcontroller (feedback loop).

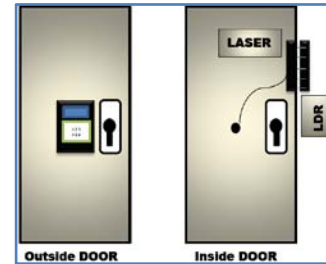


Figure 3 : Pictorial representation of how Password Authentication and Detector Circuit are implemented

Double Authentication: Thus it is observed that the door can only be opened with the right password and right key to the lock. Even the present doors need not be replaced but just a small hole (approx 1cm radius) on the door is sufficient to install this system. Thus the security system is reliable and also easy to implement.

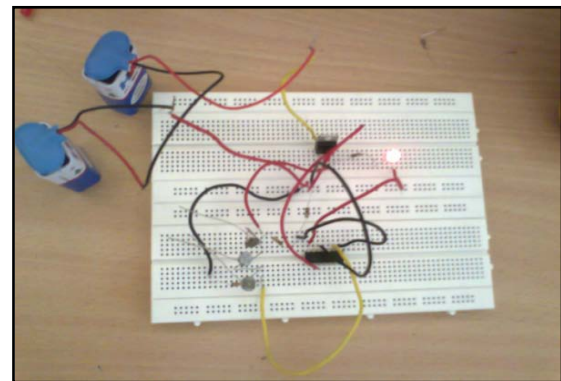


Figure 4 : Real Time working of Detector Circuit

d) Inverse Logic Buzzer

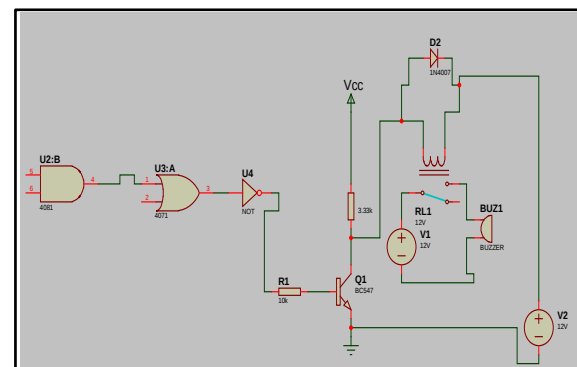


Figure 5 : Circuit Connections of Inverse Logic Buzzer

[Note: The inputs of "AND Gate" and "OR Gate" are connected to the port pin of microcontroller]

When wiring was used to switch ON the Buzzer, questions would be raised about what will happen if someone enters the home illegally and cuts the wire that connects main system to Buzzer.

For that reason using logic gates and applying inverse logic concept, a system is designed in such a way that even though the intruder cuts the wires the Buzzer doesn't switch OFF.

[Note: In real time connections the 74LS08 QUAD input AND Gate and 74LS32 Quad Input OR Gate will be used^[7]]

1) Working

The Inverse Logic Buzzer has 3 logic gates: AND, OR and NOT with a Buzzer.

OR Gate input changes based on the status of security system, 0- activated and 1-deactivated.

The 2 Inputs of AND gate signify the state of Detector Circuit and Password Authentication.

Initially when security is switched ON the inputs of AND is HIGH and OR Gates LOW, thus the output of OR is HIGH and the NOT gate inverses the signal from HIGH to LOW and the relay is not energized, Buzzer is OFF.

When an intruder breaks into the house, the detector circuit is disturbed and input of the AND gate changes from HIGH to LOW. Thus the output of OR gate will be LOW and the NOT gates inverses signal to HIGH, thus relay is energized and the Buzzer switches ON. The same principle discussed above is followed when a Wrong Password is entered (multiple times).

So the intruder should search for the main location of the buzzer, running along the wire. For best efficient working of buzzer, it is preferable to use multiple buzzers placed in different places, i.e. rooms. So that by the time the intruder finds and stops all the buzzers the entire surrounding neighbourhood area would have been alerted.

2) Relay Circuit Working

- ✓ OFF Condition: When the transistor (BC 547 npn) is OFF, the two voltage supplies Vcc and V6 tend to flow through the same path, opposing one another. Hence the relay coil is not energized properly and the contact switch remains open. The Buzzer is OFF.
- ✓ ON Condition: When the transistor is ON, the supply from Vcc gets grounded. The V6 energizes the coil, enabling the closing of the contact switch and Buzzer is switched ON.

is activated by entering the right password using the Keypad. The right password is verified by checking the entered password with the password stored in the EEPROM. Activating the system means that the Buzzer and Detector Circuit are energized.

Then an option to switch ON/OFF the Home Lighting is requested. At times when parents are leaving home with their kids at home doesn't prefer to cut OFF the power supply, so for that an option is provided to keep the lightings ON or OFF and the power is monitored through higher withstanding capacity relay.

Once the option is provided and the owner left the home, the security system gets activated. System is deactivated only when the right password is entered with the right key to the door lock, thus providing Double Authentication to the home.

If an intruder attempts to break into home by either forcibly opening the door or by placing a duplicate key, the detector circuit is disturbed (as the right password is not entered) and the Buzzer is switched ON.

Few other details that have been taken care are:

- ✓ Once the Buzzers gets activated it switches OFF the Laser Circuit, so that even if the intruder closes the door after breaking in, it doesn't deactivate the alarm as the Laser won't fall on LDR anymore.
- ✓ By giving a delay loop in such a way that the detector circuit gets disturbed only when Laser stops falling on the LDR for around 1sec. Thus if any minute dust particle passes through gap between the LDR-Laser doesn't trigger the buzzer.
- ✓ Even if the intruder tries to break the password system placed on the door to disable the security system, the outputs of the logic gates goes LOW and Buzzer turns ON automatically.
- ✓ As observed the system is divided into different sections and each section is supplied with a secondary supply unit (Batteries), so that even if the main supply is cut off the system will shift on to the backup power provided. As the sections are divided it will be easy to add separate power supply.

IV. COMPLETE WORKING OF L³

The system is placed on the door as explained before. When the owner is leaving the home, the system

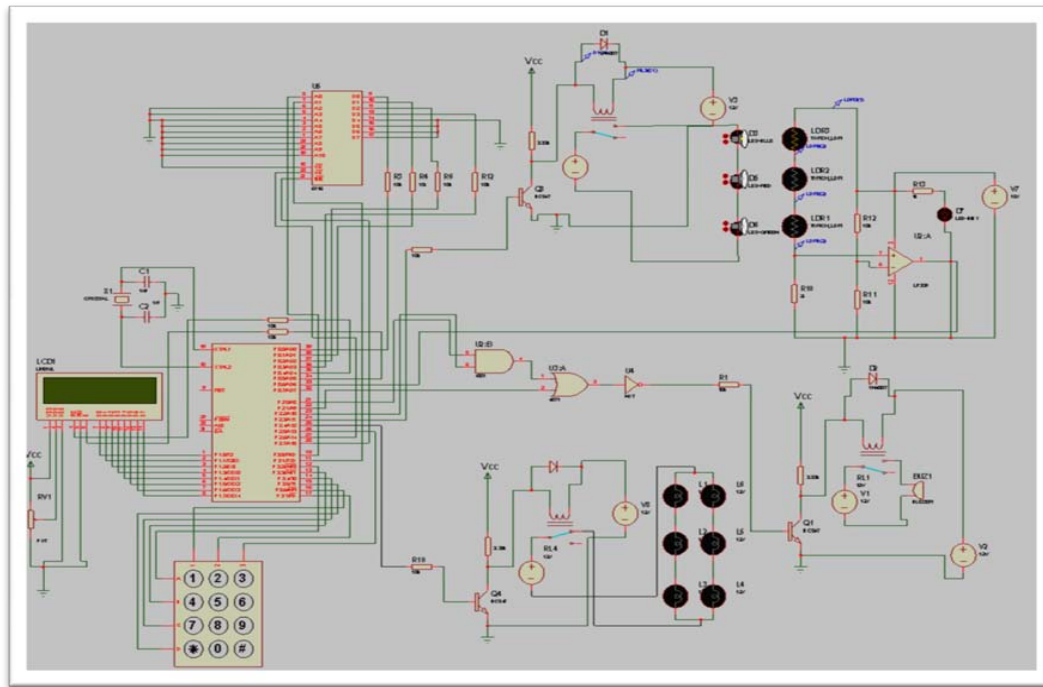


Figure 6 : Complete circuit connection of the prototype design of L³ Home Security System

FLOW CHART

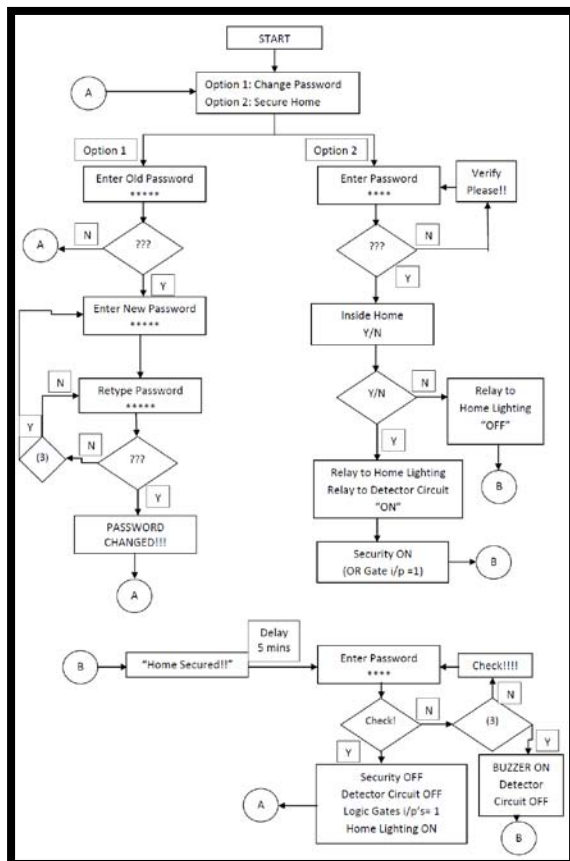


Figure 7 : Program Algorithm for L³ Security System. The program was framed using C Language in Kiel μ Vision Software [8].

V. COST ANALYSIS

For the proposed system, components of the system are available in local market. The recent cost for entire the system is given below.

Table 1 : Production Cost of L³ Security System ^[#]

Sl.no	Component Name	Cost (INR)
1	AT89V51RD2 Microcontroller	100
2	Crystal Oscillator	20
3	Electromagnetic Relay – 4	40
3	Detector Circuit (Laser + LDR + LP339)	200
4	Password Authentication (LCD LM016 + 4X3 Keypad + EEPROM)	200
5	Logic Gate IC's (74LS08 AND + 74LS32 OR)	30
6	Power Supply (Batteries + Step Down Transformer)	250
7	Design Accessories (PCB + Resistors + Capacitors, etc.)	150
	TOTAL =	990 /-

[#] – According to cost estimation made in May 2012, in Bangalore, India

a) Low Cost

The L³ Home Security System is a security system designed especially for existing homes and also its application to shops, banks etc. The system is

developed to make very affordable to reliable security system. Although there are existing security systems for that price, the L³ differ from them in many ways. The system was designed using locally available components and it is very cheap. The double authentication system with the inverse logic alert signal makes L³ different from the existing systems. The home security is low cost, reliable and can be easily implemented.

VI. FUTURE UPGRADATIONS

a) SMS Service

At times if the home is at an isolated locality, a buzzer won't alert the neighbors. In such conditions, another alert signal can be generated by sending alert SMS using GSM device to the owners or to nearby police station.

b) Other Sensors



Figure 8 : PIR and IR sensor

- 1) PIR Sensors: PIR ^[9] i.e. Passive Infrared Sensor is used as a motion and fire detection sensor. In the home it is mounted at height of about 3m at a corner of a room. 12V DC is given to the PIR to power the sensor. The circuit switch is normally closed when the motion is not activated. As soon as the PIR senses considerable temperature change, which can be due to motion or fire, the circuit switch opens. 5V DC is given to the normally closed switch. Thus at the start it sends high signal to the AND gate (as per explanation from section III). When motion is detected, circuit switch is open thus LOW signal is send to AND which switches ON the buzzer as per Inverse Logic concept (refer section 3.4).
- 2) IR Sensors: IR (Infra Red) sensors are used for motion detection. IR working concept is similar to that of Detector Circuit. When the transmitter signal is being received by Receiver, output signal is HIGH. Then the signal is disturbed, i.e. someone interferes in between the receiver stops receiving signal from transmitter. At thus condition the output signal will be LOW. The output signal is generated based on the closing and opening of switch at the Relay Circuit. Thus IR sensors can be used for

detection at doors, windows etc, to restrict the entry of intruder through doors or windows other than the main entry door.

VII. SIMULATION RESULT

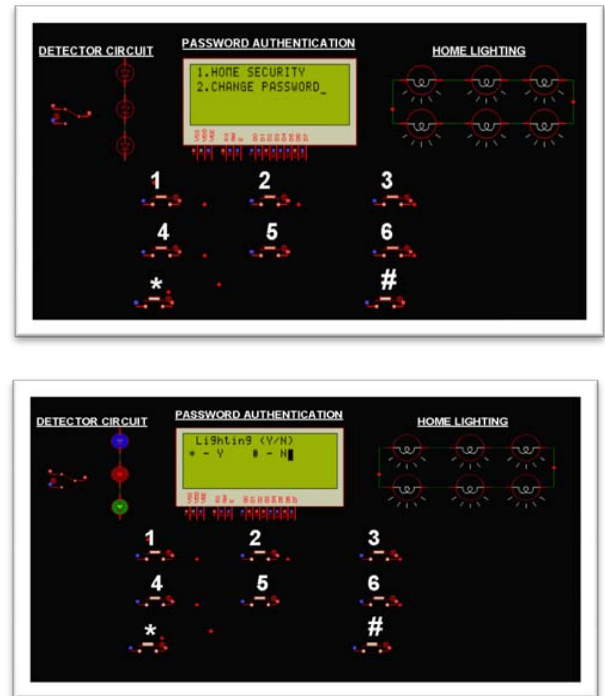


Figure 9 : Snapshots of running simulation of home security system using Proteus ISIS 7 Professional

VIII. CONCLUSION

The present technology for Home Security Automation at entry level involves systems like RFID cards, Biometrics Access System, ZIGBEE based etc. These systems provide a very high level of security to home, but comes with high price thus limiting the security system accessible only to wealthy families. These features also come with great complexity in designing, working and implementation.

Thus we attempted to design a system which can be affordable to every home within a feasible price which is less than 5000 INR, i.e. approximately **100 USD** (includes the installment and future upgradations). Also the working of the system is simple and easily can be implemented on existing doors without the need of replacing or modifying the door.

IX. ACKNOWLEDGEMENT

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Comparative Analysis and Security Issues in Broadband Wireless Networks

By Dr. Gurjeet Singh

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Abstract - Broadband wireless networks are considered to be enterprise-level networks providing more capacity and coverage. Wireless networking has offered an alternative solution to the problem of information access in remote inaccessible areas where wired networks are not cost effective. They have changed the way people communicate and share information by eliminating worrisome factors of distance and location. This paper provides a technical analysis of alternatives for implementing last-mile wireless broadband services. It provides detailed technical differences between 802.11 (Wi-Fi) wireless networks with 802.16 (WiMAX), a new technology that solves many of the difficulties in last-mile implementations.

Keywords : Broadband wireless, Last mile access, Rural connectivity, WiMAX, Wi-Fi, Digital divide, Network Security.

GJRE-F Classification : FOR Code : 100510



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I. INTRODUCTION

Broadband in the general term also referred as high-speed network connections. Broadband describes a medium that can carry signals from multiple independent network carriers on a single coaxial or fiber optic cable. While the benefits are compelling, there are still a number of challenges with moving to broadband Internet. Spotty geographic coverage and installation challenges are a significant impediment. As cable and DSL providers accelerate their deployment plans, this situation is improving, but there are still significant challenges. Network security is another very significant issue, and one that is becoming increasingly visible as hacker attacks on home PCs [1].

There are so many profits when we adapt a broadband network, this broadband network can spread through different geographic but installation is the major problem. Internet connections via cable modem and Digital Subscriber Line (DSL) are frequently known as broadband Internet connections. Cable and DSL providers speed up their operations plan and the conditions are improving, but network security is the major concern.

Security problems are increasing rapidly as hacker attacks on home PCs and major company websites such as government organizations. One of the most compelling uses of broadband connections is to allow enterprises to Connect branch offices and telecommuters into the corporate network with high speed remote access[2].

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II. OVERVIEW OF WI-FI AND WIMAX

a) The IEEE 802.11 (Wi-Fi)

The Wireless Fidelity (Wi-Fi) devices made possible the discovery of the wireless network world. In the WLAN field, the only major competition comes from HIPERLAN II. The Wi-Fi standard family allows wireless network over short distances. These standards are sometimes associated with directional antennas to establish point-to-point connections. WLANs based on the IEEE 802.11 standard are expected to be a major component to enable an integrated office, hospital, home networks and for campus buildings. The 802.11 WLANs operate in the ISM (industrial scientific and medical) bands, with several flavors of physical layer available. The first 802.11 wireless network standards were developed in 1997 as an extension to the Local Area Network. It was known as wireless Ethernet that only supported a maximum speed up to 2 Mbps. Frequency Hopping Spread Spectrum (FHSS) and Direct Sequence Spread Spectrum (DSSS) were the modulation techniques supported. There are three well known 802.11 wireless family standard widely used today.

b) The IEEE 802.11b

A refined standard for the original 802.11 and was successful due to its high data rates of 11 Mb/s - range of 100 m to a maximum of a few hundreds meters, operates on 2.4 GHz unlicensed band. 802.11b is the most widely deployed wireless network within the 802.11 wireless families [4, 5]. It uses the DSSS modulation technique that is more reliable than the FHSS.

c) The IEEE 802.11g

The IEEE 802.11g wireless standard also operates on the 2.4 GHz band and has similar range and characteristics as the 802.11b. It has a data rate of 54Mbps. The 802.11g has backward compatibility with 802.11b and differs only on the modulation technique; it uses Orthogonal Frequency Division Multiplexing (OFDM). This then makes the 802.11b devices not able to pick the signal from the 802.11g devices.

d) The IEEE 802.11a

Operates in the 5 GHz band with a maximum data rate of 54Mbps. The major disadvantage in deploying 802.11a with the other 802.11 standards b

and g is that, they cannot co-exist, as they operate on different frequency bands. 802.11b/g operates on the 2.4 GHz spectrum. There are some wireless card and access points which are compatible to all the three standards thereby supporting the 2.4GHz and 5GHz frequencies. The benefits of using Wi-Fi for last-mile solutions are:

1. Off-the-shelf 802.11 standard products are currently available
2. Initial investment is cost effective for small deployments
3. Flexibility over wired installations can be achieved

e) *The IEEE 802.16 (WiMAX)*

Wireless networks adapted for covering cities and villages, arrived a few years after the Wi-Fi type WLAN. The IEEE 802.16 WiMAX (World Interoperability for Microwave Access) standard is based on global interoperability including ETSI HIPERMAN, IEEE 802.16d-2004 for fixed, and 802.16e for mobile high-speed data. It is an emerging technology that delivers carrier-class, high speed wireless broadband at a much lower cost than the cellular services while covering large distances than Wi-Fi. It has been designed to be a cost-effective way to deliver broadband over a wide area. It is intended to handle high-quality voice, data and video services while offering a high QoS. WiMAX is classified as the Wireless Metropolitan Area Network (WMAN) that operates in between 10 and 66 GHz Line of Sight (LOS) at a range up to 50 km (30 miles) and 2 to 11GHz non Line-of-Sight (NLOS) typically up to 6 - 10 km (4 - 6 miles) for fixed customer premises equipment (CPE) [11]. Both the fixed and mobile standards include the licensed (2.5, 3.5, and 10.5 GHz) and unlicensed (2.4 and 5.8 GHz) frequency spectrum. However, the frequency range for the fixed standard covers 2 to 11 GHz while the mobile standard covers below 6 GHz. Depending on the frequency band, it can be Frequency Division Duplex (FDD) or Time Division Duplex (TDD) configuration. The data rates for the fixed standard will support up to 75 Mbps per subscriber in 20 MHz of spectrum, but typical data rates will be 20 to 30 Mbps. The mobile applications will support 30 Mbps per subscriber, in 10 MHz of spectrum, but typical data rates will be 3 - 5 Mbps.

f) *PHY (Physical) Layer*

Apart from the usual functions such as randomization, forward error correction (FEC), interleaving, and mapping to QPSK and QAM symbols, the standard also specifies optional multiple antenna techniques. This includes space time coding (STC), beam forming using adaptive antennas schemes, and multiple input multiple output (MIMO) techniques which achieve higher data rates. The OFDM modulation/demodulation is usually implemented by

performing fast Fourier transform (FFT) and inverse FFT on the data signal.

The MAC layer used by WiMAX is based on a time division multiple access (TDMA) mechanism to allow a homogeneous distribution of the bandwidth between all the devices which is more effective and support several channels compared to the mechanism used by Wi-Fi (CSMA-CA). This makes it possible to obtain a better optimization of the radio spectrum with better efficiency (bits/seconds/Hertz). Thus, WiMAX has an efficiency of 5 Bps/Hz compared to the 2.7Bps/Hz of Wi-Fi that makes it possible to transmit 100 Mb/s on 20 MHz channel.

g) *Comparison of Wi-Fi and WiMAX*

From the technical overview of the two wireless technologies given in previous section, it can be seen that they are not addressed to the same market but are very complementary. Wi-Fi allows the implementation of wireless local area network for a house or a small building. It can also be used to carry out a public hot spot allowing mobile points to connect in a hotel, an airport, etc. WiMAX is a metropolitan technology whose objective is to interconnect houses, buildings or even hot spots to allow communication between them and with other networks (Internet, etc).

Although not being targeted on the same use, more recently WiMAX technology has several advantages compared to Wi-Fi. Such as: a better reflection tolerance; a better penetration of obstacles; and an increased in the number of interconnections (a few hundreds of equipment rather than some tens of equipment for Wi-Fi). It's obvious that the WiMAX standard goal is not to replace Wi-Fi in its applications but rather to supplement it in order to form a wireless network web. Despite the similarity in equipment cost, WiMAX technology requires a costly infrastructure while Wi-Fi can be easily install using low cost access points. These two wireless technologies have common components in their operations with a major difference in the communication range. Table 1 below gives the detailed comparative analysis of the two broadband wireless access networks (WiFi and WiMAX) suitable for rural connectivity.

Table 1 : Comparison between 802.11 & 802.16

Properties	802.11(Wi-Fi)	802.16(WiMax)
Frequency Band	5GHz	2GHz to 11GHz
Range	100m	50km
Coverage	Optimized for indoor performance	Optimized for outdoor performance
Security	WAP+WEP	DES & RSA
Radio Technology	OFDM(64 channels)	OFDM(256 channels)

Modulation	QPSK-802.11b	QPSK 14, 64, 256-QAM
Data Rate	802.11a-54Mbps 802.11b-11Mbps	802.16a-75Mbps 802.16b-15Mbps

III. SECURITY ISSUES AND SOLUTIONS

a) DOS (Denial of Service)/ Reply attack

Denial of Service (DoS) is one of the major issues of all types of wireless networks especially broadband wireless networks. When authorized users are not provided a requested service within a defined maximum waiting time, it means that a DoS violation has occurred. It is the most harmful and dangerous attack which can be launched on any layer of broadband Wireless Network. DoS attacks target availability by preventing communication between network devices or by preventing a single device from sending or receiving traffic, where availability ensures that authorized users can access the data, services and network resources from anywhere anytime.

Physical Layer Vulnerabilities WMN and IEEE 802.11 uses 2.4 GHz frequency band while IEEE 802.16 uses 10-66 GHz and 2-11 GHz bands at physical layers. DoS attack can be launched against physical layer by using radio jamming device or a source of strong noise to interfere the physical channels and may compromise the service availability. However this kind of attack is not common as it need specialized hardware equipment to be launched, furthermore jamming attacks can be detected using radio analyzers. It can create great problems during exchange of sensitive information or during warfare. For jamming attack in

- IEEE 802.11, the attacker needs to be close to the target AP
- IEEE 802.16, the attacker needs to be close to the Base Station (BS)
- WMN, the attacker can launch the attack from anywhere. Due to the vast coverage area and dense deployment of wireless mesh routers in WMN, it is more vulnerable to physical layer DoS attacks

Currently, IEEE 802.11 uses Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spread Spectrum (FHSS), IEEE 802.16 is using Orthogonal Frequency Division Multiple Access (OFDM) and Scalable OFDM access (SOFDMA), while WMN uses OFDM and Ultra wide band (UWB) mechanisms for radio transmission. None of the mechanism is capable enough to handle the jamming attack on these broadband wireless networks.

b) Distributed Flooding DoS

A distributed flooding DoS attack is a huge challenge for all the wireless broadband networks, as this attack can bring down an entire network or

consume the network bandwidth to a great extent. This kind of attack is launched by first compromising large number of innocent nodes in the wireless network termed as Zombies, which are programmed by highly skilled programmer. These zombies send data to selected attack targets such that the aggregate traffic congests the network. In most of the cases, the DDoS is impossible to prevent and it has the ability to flood and overflow the network. In IEEE 802.11 the target of distributed flooding would be Access Point (AP), in WMN the target is wireless mesh router while in IEEE 802.16 it is base station.

c) Rogue and selfish backbone devices

The attacker can seriously disrupt the broadband wireless networks by compromising the core network devices. In WMN and IEEE 802.11, a selfish mesh router or selfish AP can degrade the network performance either causing congestion or unavailability. IEEE 802.16, a rogue BS is an attacker station which is used to confuse the mobile stations of the network; as such kind of BS seems and acts like a legitimate BS. Mesh routers or APs are compromised by the attackers using sniffers. A sniffer is an application which is used for passive traffic analysis attack to analyze the network traffic. In IEEE 802.16, the BS is compromised by reprogramming a device with the hardware address of another legitimate device with hardware address can be detected by intercepting the management messages of IEEE 802.1 using sniffers. The same mechanism can be applied on mesh routers and APs to compromise using hardware address of another network device.

Authorization flooding on backbone devices WMN and IEEE 802.11 nodes use Probe request frames to discover a wireless network, if a wireless network exist then the AP respond with Probe response frame. The clients select that AP which provides the strongest signal to it. Here the attacker can spoof a flood of probe request frames presenting a lot of nodes searching for wireless network, can seriously overload the AP or wireless mesh router. If the load exceeds the threshold value will cause the AP or wireless mesh router to stop responding and may create service unavailability. In IEEE 802.16 the client stations use certificate to authenticate and register with the BS. The client station can send a bulk of registration requests to the BS may result in DoS.

d) Node deprivation attack

In node deprivation attack, the attackers target a single node and isolate it from taking part in the normal network operations. In WMN and IEEE 802.11, the nodes first authenticate itself with the mesh router or AP, and needs to de-authenticate it if the node has no more desire to use the network resources. The attacker can spoof the de-authentication message on behalf of the target node so that to stop it from using the network resources. The same vulnerability exist in IEEE 802.16,

where the adversary eavesdrop the authentication message exchange between the node and the BS, and then replays this message many times to BS, creating DoS for the target node.

IV. RESULTS OF DOS ATTACKS AND POSSIBLE COUNTERMEASURES

The results of different DoS attacks on broadband wireless networks vary with the nature and type of DoS attack.

- DoS attack is of low intensity, if launched against a single node either to exhaust its battery or to isolate it from the network operations.
- DoS attack is of high intensity if it is launched to make services unavailable for a target area in wireless broadband networks. Selfish mesh router attack in WMN and rogue BS attack is used for this purpose.
- Dos attack will be of highest intensity if it is launched to cripple down the entire broadband wireless network by distributive flooding.

Distributed flooding is normally used for this purpose to exhaust the bandwidth of the network or to overflow the resources of the gateways. DoS in any form against any network is regarded as a severe attack. Some possible countermeasure needs to be investigated to overcome to some extent against DoS and related issues in broadband networks.

Message 1. SS → BS : Cert (SS, Manufacturer)
 Message 2. SS → BS : T_S | Cert (SS) | Capabilities | SAID | SIG_{SS} (2)
 Message 3. BS → SS : T_S | T_B | KU_{SS} (AK) | Lifetime | SeqNo | SAIDList | Cert (BS) | SIG_{BS} (3)

'Cert' stands for the X.509 certificates used. KU_{SS} (AK)' is the Authentication Key encrypted by SS's public key. T_S and T_B are timestamps of respectively the SS and BS. SeqNo and Lifetime are a sequence number and lifetime for the AK. SIG_{SS} and SIG_{BS} are signatures for respectively the SS and BS. The SAID List defines the security associations ID's to be used for communication. By adding the timestamps and signatures, freshness can be guaranteed for both messages. This way both SS and BS know that the message is fresh and not intercepted and replayed. The key management protocol is also vulnerable for these attacks. Both the message from BS to SS and vice versa can be replayed to cause DoS or other unwanted behaviour.

HMAC stands for Hash Message Authentication Code, is a type of message authentication code (MAC)

calculated using a cryptographic hash function in combination with a secret key. As with any MAC, it may be used to simultaneously verify both the data integrity and the authenticity of a message. What happens is that SS requests (or BS forces him to, using message 1) a new TEK in message 2. HMAC (1) can be used by SS to detect forgery attacks. HMAC (2) assures BS that the message is authentic. HMAC (3) assures SS that message 3 is from BS and has not been modified.

Message 1. BS → SS: SeqNo | SAID | HMAC (1)
 Message 2. SS → BS: SeqNo | SAID | HMAC (2)
 Message 3. BS → SS: SeqNo | SAID | OldTEK | NewTEK | HMAC (3)

Because message 1 is optional, T_{B2} will be set to 0 in message 2 by SS when it initiates re-keying. T_{B2} in message 3 is generated by BS in responding to SS's request to assure SS the freshness and aliveness. When BS starts the rekeying, T_{B2} is generated in message 1 by BS and SS should include it in message 2 to assure BS the freshness and aliveness, but BS can omit it in message 3 by setting it to 0.

Message 1. BS → SS: T_{B2} | SeqNo | SAID | HMAC (1)
 Message 2. SS → BS: T_{B2} | T_{S2} | SeqNo | SAID | HMAC (2)
 Message 3. BS → SS: T_{S2} | T_{B2} | SeqNo | SAID | OldTEK | NewTEK | HMAC (3)

V. ANALYSIS

We will seem, per problem, at all answers by means of the principles stated over. For every explanation there is a table showing how they score on each criterion. A '+' means it scores well on that criterion, a '+/-' that it is doubtful and a '-' means a bad score. A '?' means no information was available for that criterion, for example no performance information because no simulations were ran.

a) DoS/Reply attack

[XMH06] depicts good quality development for authentication and authorization beside rerun assaults. Adding together the timestamp and signatures needs a sensible alteration to the normal. No data is obtainable concerning presentation but our anticipation would be a minute plunge in presentation. Even though the answer is deconcentrated, the argument in communication dimension is not radically. Yet, owing to the forward of timestamps and signatures, measurability might be exaggerated[9].

VI. CONCLUSION

From the above analysis, we are able to consider different issues pertaining to security aspect of broadband technology. When discussing the security of wireless technologies, there are several possible Perspectives. Different authentication, access control and encryption technologies all fall under the umbrella of security. Although relevant and important building blocks for overall security, these are not the focus of this paper. Instead, it will explore the problems at the implementation level of the current wireless access technologies and their Real world implications. As future technology of broadband is wireless communication, in that WiMAX plays a major role. In other way, in this research paper we would be discussing issues of security feature of WiMax and analyse one of the security features to work on it.

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References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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