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- Controlling Voltage and Frequency
- Presence of Static Transfer Switch
- Wireless Communication Channel
- FPGA Arithmetic Processor

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Controlling Voltage and Frequency of a Power Network with Microgrid Using Droop Method

By Yasser Rahmati Kukandeh, Hassan Rahmati Kukandeh , Mohammad Hossein Kazemi

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Abstract - Microgrids (MG) are new concept of electric power networks consisting of distributed generation (DG), renewable energy resources and sensitive loads. The goal of microgrid operation is to provide reliable and high-quality electric power regardless of faults or abnormal operating conditions. Many control methods have been employed to regulate the output power of DGs used in MGs. This paper presents a control scheme for DGs of a power system, especially with voltage source inverter (VSI) interface, for both grid connected and islanded modes. A comprehensive study has been performed through PSCAD simulations of the inverter-fed MG behavior under both islanding and connected operation for different load conditions. The simulation results prove the droop method efficiency in controlling the voltage and frequency of the inverter output which is connected to the loads.

Keywords : DG; Microgrid; Droop Method; Connected Mode; Islanding Mode.

GJRE-F Classification: FOR Code: 090607

CONTROLLING VOLTAGE AND FREQUENCY OF A POWER NETWORK WITH MICROGRID USING DROOP METHOD

Strictly as per the compliance and regulations of:

Controlling Voltage and Frequency of a Power Network with Microgrid Using Droop Method

Yasser Rahmati Kukandeh[α], Hassan Rahmati Kukandeh[Ω] ,Mohammad Hossein Kazemi[β]

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Keywords : DG; Microgrid; Droop Method; Connected Mode; Islanding Mode.

I. Introduction

Renewable energy emerges as an alternative way of generating clean energy. As a result, increasing the use of green energy benefits the global environment. This topic relies on a variety of manufacturing and installation industries for its development. As a solution, continuously small and smart grid energy systems appeared, including renewable energy resources, micro-generators, small energy storage systems and critical and non-critical loads have formed among them a special type of distributed generation system called the Microgrid (MG) [1, 5].

Advantages of MGs can be cited as: i) MG can operate independently without any support from the upper stream of the network. It is one of the advantageous as the MG would not be affected, but rather separated from the upper stream where the fault occurs, and thus in islanding mode [1]. ii) MG has "plug-and-play" feature. This means that it can always be connected or disconnected to the medium-voltage network [3]. iii) They are clean sources of energy that have very little environmental impact on the community compared to those conventional energy technologies [5].

The high penetration of DGs like fuel cell, photovoltaic, wind turbine, micro turbine and etc, along with different types of loads, always raises concern about coordinated control and power quality issues.

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In microgrid, DGs are connected through VSIs as an interface to deliver the sinusoidal voltage to the network and loads. parallel DGs are controlled to deliver the desired active and reactive power to the system while local signals are used as feedback to control the inverters. The power sharing among the DGs can be achieved by controlling two independent quantities of frequency and fundamental voltage magnitude [9, 10].

A MG can operate in grid-connected mode or islanding mode, hence increases the reliability of energy supplies by disconnecting from the grid in the case of network faults. When the MG is connected to the main grid, if the produced power of the MG is lower than the power demand level, main grid provides this difference in power. On the other hand, MG can send the excessive generated power to the main grid [6].

If the grid has to go in islanding mode due to fault or low-voltage, the network controllers must keep the system frequency and voltage in a desirable area leads to sending the qualified power to consumers. The MG should also recover the frequency and voltage in islanding mode rapidly. When MG goes to islanding mode, its last situation should be considered: if it was importing energy then after entering to the islanding mode, it has to increase the generation level to compensate the lost power; therefore in this mode the MG frequency will be decreased. On the other hand, if MG was exporting energy and afterwards it has gone to islanding mode, it should decrease the generation level so the grid frequency will rise [2, 4].

Now a considerable research has been undertaken on the control strategy of the MG. Flexible and fast controls of active and reactive power are important requirements during transient and steady-state operation of a MG system in both grid-connected and islanding modes.

A MG when subjected to disturbances can experience angle instability and poor voltage quality due to the presence of DGs with slow response rotating machines and DGs with power electronic converters as the interface to the utility system. To ensure stable operation during network disturbances while maintaining power quality in the islanded mode of operation, a more sophisticated control strategy for MG needs to be developed, in order to warranty both quality of supply and ensuring power management supervising critical and non-critical loads [8]. Also, the basic issue on small grids is the control of the number of micro-sources. MG concept allows larger distribution generation by placing many micro-sources behind singles interfaces to the utility grid. Some key power system concepts based on power against. Frequency droop methodology, voltage control and can be applied to improve system stability, enhance active and reactive support. Flexible and fast controls of active and reactive power are important requirements during transient and steady-state operation of a MG system in both grid-connected and islanding modes [11, 13].

This paper is organized as follows. In Section II, the structure of the MG has been described. Section III explains the droop method to control the DGs in a power network with MG. To prove the efficiency of droop method some simulations have been done in different situations with connected and islanding modes and the results are discussed in section IV. The simulation results show that droop method can regulate the voltage and frequency of the PCC (point of common coupling) where inverter has been attached to the load or network both in connected and islanding modes.

II. Study System

Figure 1 shows a single-line diagram of the system used to investigate typical MG operational scenarios. The basic system's configuration and parameters were extracted from the benchmark system of the IEEE Standard 399-1997, with some modifications to allow for autonomous MG operation. The system is composed of a 13.8 KV, three-feeder distribution subsystem which is connected to a large network through a 69 KV radial line. The 13.8 KV distribution substation is equipped with a three-phase 1.5 MVAr, fixed shunt capacitor bank. The 13.8 KV substation busbar is radially connected to the main grid through the substation transformer and a 69 KV line. The network at the end of the 69 KV line is represented by a 69 KV, 1000 MVA short-circuit capacity bus. Combinations of linear and nonlinear loads (L_1 to L_5) are supplied through three radial feeders of the subsystem. Loads L_2 to L_5 are composed of linear RL branches. Load L_1 is a three-phase diode rectifier load. The aggregate of L_1 and L_2 constitutes a sensitive load within the distribution subsystem.

The system also includes two DG units, i.e., DG_1 (2.5 MVA) and DG_2 (5 MVA) on feeders F_1 and F_3 respectively. DG_1 utilizes a voltage-sourced converter (VSC) as the interface medium between its source and the power system. DG_1 Represents a dispatchable source with adequate capacity to meet the active/reactive power commands, within pre-specified limits, subsequent to disturbances. Such a dispatchable source may also include energy storage interfaced at the converter dc bus. DG_1 provides control on its output active and reactive power components independently. DG_2 is a synchronous rotating machine equipped with excitation and governor control systems. It may represent either a diesel-generator or a gas-turbine-generator unit [7].

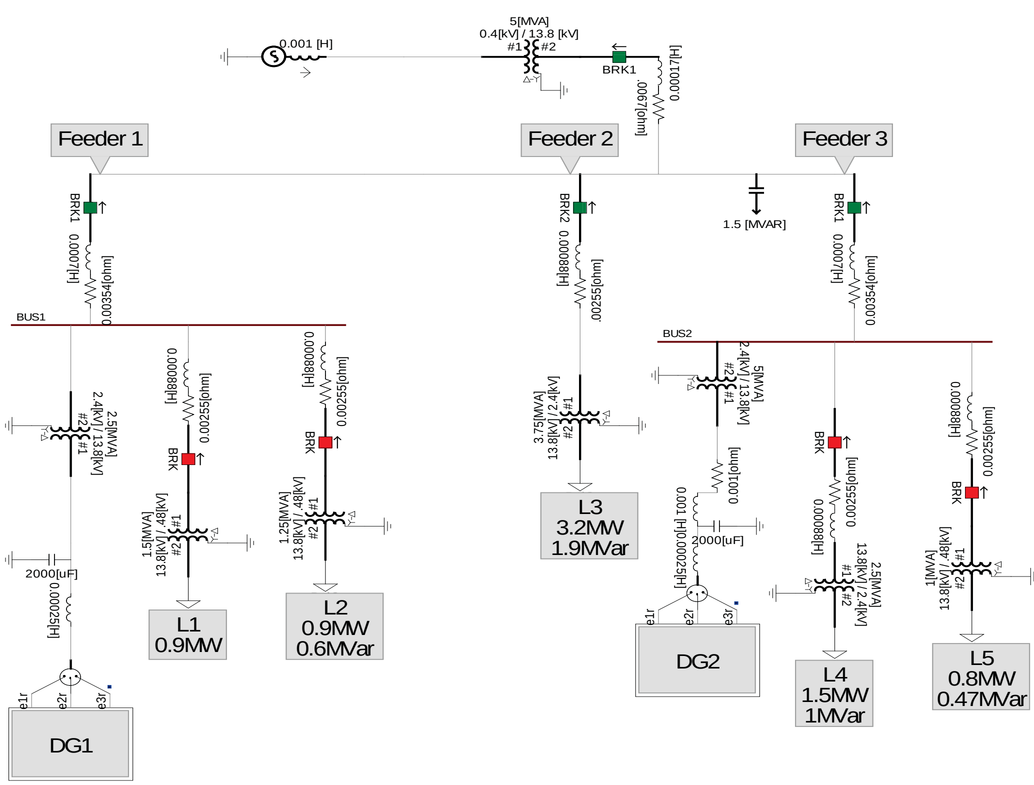

Figure 1 : Studied System

III. Microgrid Control

In a MG, the DG supply can be connected to a network using an inverter. An inverter can be tuned by frequency and voltage control.

For controlling the inverters usually the drop method is used. The active and reactive power of inverter can be controlled by means of this method in order to control the frequency and to produce voltage in a specific level. Active and reactive power has influence on voltage frequency and amplitude, so the control method can be described as follows:

a) Active power control versus frequency

In this mode, a frequency change is affected by changing in active power. Figure 2 shows the droop of power versus frequency changes.

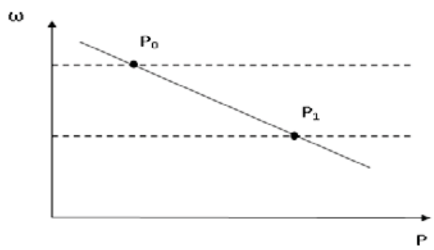

Figure 2 : Droop active power versus frequency

According to figure 2 it can be deduced that whenever frequency decreases in a network, controllers make the supplies to increase their production and it means the production level changes from P_0 to P_1.

This state will happen to a MG when a fault occurs and it changes the status into islanding mode. The MG reconnects to main grid meanwhile the frequency increases then controllers make the DG to decrease the production level.

Equation 1 represents this controlling structure"

$$\omega = \omega^{*} - m.(P - P^{*}) \tag{1}$$

b) Reactive power control versus voltage

In this mode, changes in voltage have an interaction with changes in reactive power. According to figure 3, this controlling mode is represented by Eq. 2:

$$E = E^{*} - n.(Q - Q^{*}) \tag{2}$$

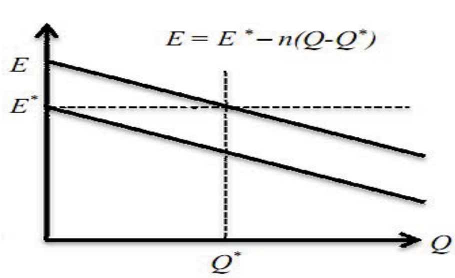

Figure 3 : Droop reactive power versus voltage

Where E is the amplitude of the inverter output voltage; Q is the reactive power of the inverter output, $Q^{*}$and E^{*} are the reactive power and voltage amplitude at no-load, respectively; and n is the proportional droop coefficient.

IV. Simulation And Results

To verify the proposed method some simulations have been done in PSCAD. To cases have been considered and explained as follows:

Case study1 : In this state the load of L3 in 0.5 seconds is disconnected. Then Micro Grid in the second 1 turns into the island state and the system acts as two separate Micro Grids. As in Figure 4 is observed, in the 0.5 seconds, DG1, in addition to producing the amount of MG1, exports the excess energy to L3, while MG2 only produces the which meets its own need. After the segregation of load L3 at 0.5 seconds due to the reduction in the amount of demand, the rate of the production of the units is decreased. In a run-time between 0.5 and 1 second DG1 supplies some portions of. MG1`s energy need, but since the production in MG1 occurs in the first 0.5 second, its frequency is decreased. It is worth noting that since MG1 is importing, its frequency remains more than nominal amount. On the other hand, since the MG2 is importing energy, the frequency of it drops below the nominal value. In second 1, both Micro Grids are in an island state. According to the state before going into an island state, in which MG1 was importing and MG2 was exporting energy,, after going to a new state, (islanded mode), MG1 production levels set frequency to provide for themselves and 1.8 MW to reduce their production levels and MG2 increases to 2.3 MW.

As in the Figure 5 is shown, when the Micro Grids at second 1 go to an island state, due to the reduction in the amount of required reactive capacity in the network, the voltage is increased. Therefore, the unit which controls voltage for increasing the capacity of the reactive, issues an order for the reduction of voltage. After adjusting for this transient condition, the voltage returns to its stable value and is set.

Case study 2 : in this case the Microgrid issues energy to the main grid until 0.5^{th} second and afterwards, the loads L3 and L5 are disconnected simultaneously. MG1 is also in this island state. As it is shown in figure 6, Since the power required in MG1 is 1.8 MW, DG1 reduces its production level to this amount. In other part of system, DG2 and L4 are responsible for the 0.8 MW by DG2 and 0.7 MW by the main supply network. At second 1, L3 and L5 are also disconnected mode. DG1 and DG2 at this time to meet the demands, they change their production levels. Production levels for DG1 and DG2 reach to 1.7 MW and 1.6 MW respectively.

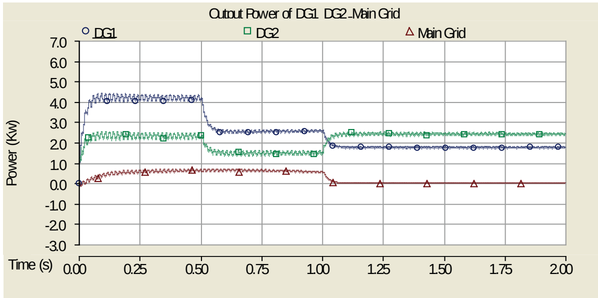

Figure 4 : power generation in case study 1

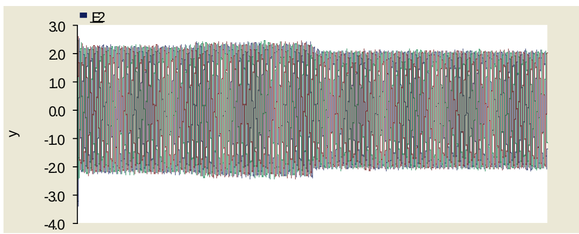

Figure 5 : voltage variation in case study 1

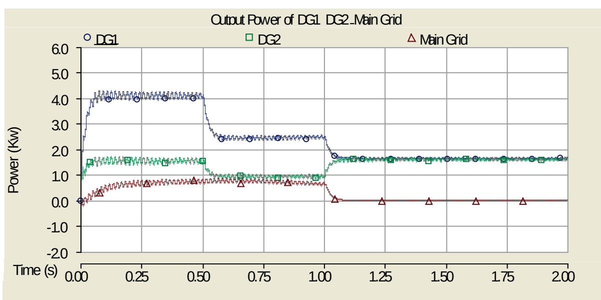

Figure 6 : power generation in case study 2

These results show that the droop method could fix the main grid generation, thus to supply the load changes, it orders the Microgrid to produce the amount of power that is required due to islanding mode and load variations.

V. Conclusion

In this paper the effect of drop method in voltage and frequency control has been discussed. As shown in Section III .in result of disconnection between network and microgrid, the active power generation level increases, if microgrid received energy before disconnection. If microgrid sends power to the network then active power generation level will reduce.

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On the Investigation of Stacked Sierpinski 'S Gasket Antenna with Enhanced Bandwidth

By S.B.Kumar, Dr.P K Singhal

Abstract - The broadband behavior of the fractal Sierpinski's gasket antenna is described in this paper. A stacked microstrip gasket antenna at iterations level three for C-band application is designed and simulated on IE3D software. The feeding technique used is transformer feed. Simulated results shows that this antenna has three resonant frequencies of gain of order 5dBi with a bandwidth of 1.64GHz and percentage bandwidth of 48.2 which empower it as a broadband antenna.

Keywords : Stacked Antenna, Gasket Antenna, Transformer Feed,VSWR,RL.

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Index terms : Stacked Antenna, Gasket Antenna, Transformer Feed, VSWR, RL.

I. Introduction

The Sierpinski gasket is named after the Polish mathematician Sierpinski who described some of the main properties of this fractal shape in 1916. In recent years, the current trend in commercial and government communication system has been to develop low cost, minimal weight, low profile antennas that are capable of maintaining high performance over a large spectrum of frequencies. This technological trend has focused much effort in to the design of microstrip antennas. Most fractal objects have self-similar shapes, which mean that some of their parts have the same shape as the whole object but at a different scale[1]. In multiple reduction copy machine (MRCM) algorithm, an initial structure called generator is replicated many times at different scales, positions and directions, to grow the final fractal structure. With the ever-increasing need for mobile communication and the emergence of many systems, it is important to design broadband antennas to cover a wide frequency range. Microstrip antenna suffers a major drawback of narrow bandwidth. This problem can be handled by three ways like lower the impedance of antenna, use of impedance matching and implementation of multiple resonances [2]. For lowering the impedance, mainly shape of radiator can be changed or thickness of substrate with lower dielectric constant and higher losses has to be chosen. As the shape of antenna is decided as per its requirements so a thick substrate with lower dielectric constant is a better option for reducing Q. Transformer feed provides impedance matching of antenna and microstrip line.

The matching network can be a quarter-wavelength impedance transformer, tuning stubs, active components or their variations,The advantage of this is that the radiator need not to be changed, which simplifies the design by allowing the impedance matching and radiation performance to be controlled independently.

Some of the major antenna properties discussed in this paper are

a) Bandwidth[2]

The term bandwidth simply defines the frequency range over which an antenna meets a certain set of specification performance criteria. The important issue to consider regarding bandwidth is the performance tradeoffs between all of the performance properties described above. There are two methods for computing an antenna bandwidth. An antenna is considered broadband if $fH/fL \geq 2$.

Narrowband by %

$$BWp = \frac{fh - fl}{fo} \times 100$$

Broadband by ratio

$$BWp = \frac{fh}{fl}$$

where $f_o \equiv$ operating frequency
$f_H \equiv$ higher cut-off frequency
$f_L \equiv$ lower cut-off frequency

b) Gain

The gain of an antenna is essentially a measure of the antenna's overall efficiency. If an antenna is 100% efficient, it would have a gain equal to its directivity. There are many factors that affect and reduce at the overall efficiency of an antenna. Some of the most significant factors that impact antenna gain include impedance, matching network losses, material losses and random losses.

$$Gain = \frac{|S12|\left(\frac{4\pi d}{\lambda o}\right)}{\sqrt{(1 - |S11|^2)(1 - |S22|^2)}}$$

where d is distance between the transmitting and receiving antenna. Gain also can be simply defined as the product of the directivity and efficiency given by

$$G = \eta D$$

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II. Antenna Design And Specifications

The original gasket is constructed by subtracting a central inverted triangle from a main triangle shape (Fig. 2.1). After the subtraction, three equal triangles remain on the structure, each one being half of the size of the original one. One can iterate the same subtraction procedure on the remaining triangles and if the iteration is carried out an infinite number of times, the ideal fractal Sierpinski gasket is obtained. In such an ideal structure, each one of its three main parts is exactly equal to the whole object, but scaled by a factor of two and so each of the three gaskets that compose any of those parts. Due to this particular similarity properties, shared with many other fractal shapes, it is said that the Sierpinski gasket is a self-similar structure.

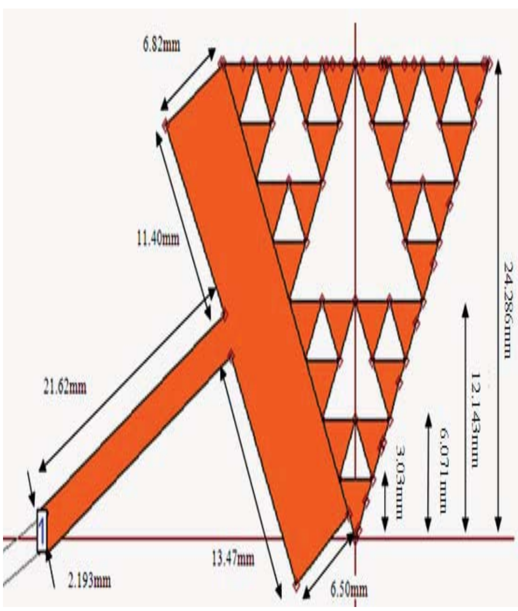

Figure 2.1 : Design of Antenna

The Sierpinski gasket (also Sierpinski triangle) was chosen as the first candidate for a fractal antenna due to its resemblance to the triangular or bow-tie antenna. As shown in Fig. 1, the height of gasket is 24.286mm. Stacking of two substrates of thicknesses 1.588mm and dielectric constant of 4.4 is done for the design. The antenna design starts with frequency is 3.4GHz and proposed antenna has got three resonance frequency at 6.18 GHz,6.942 GHz & 7.442 GHz with enhanced band width up to 1 GHz. Which indicates that this antenna is a broadband antenna.

The formulae for determining the length of each side of gasket is

$$a = \frac{2c}{3fr\sqrt{\varepsilon r}}$$

The 3D view of antenna (fig. 2.2) clearly shows the stacking and feed structure.

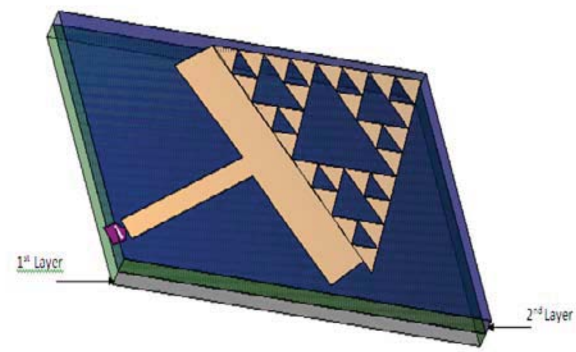

Figure 2.2 : 3D view of Design

III. Simulation Results

The proposed antenna is simulated on IE3D software and the results are shown below.

a) Return Loss

Return loss is the difference, in dB, between forward and reflected power measured at any given point in an RF system. It is a convenient way to characterize the output of signal sources. The return loss of antenna is displayed in fig 3.1.1 and its values are displayed in table 3.1.1.

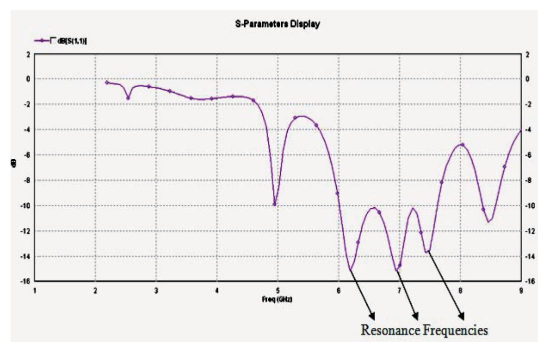

Figure 3.1.1 : Return Loss

Frequencies(GHz)	Return Loss(dB)
6.18	-15.104
6.942	-15.142
7.442	-13.682

Table 3.1.1 : Return Loss

The overall bandwidth of antenna is 1.64 GHz from 5.997GHz to 7.637 GHz with a bandwidth percentage of 48.2.

b) VSWR Result

Simulated results show that the antenna has VSWR of approximately 1 at three working frequencies. The VSWR of the antenna is shown in the figure 3.2.1.

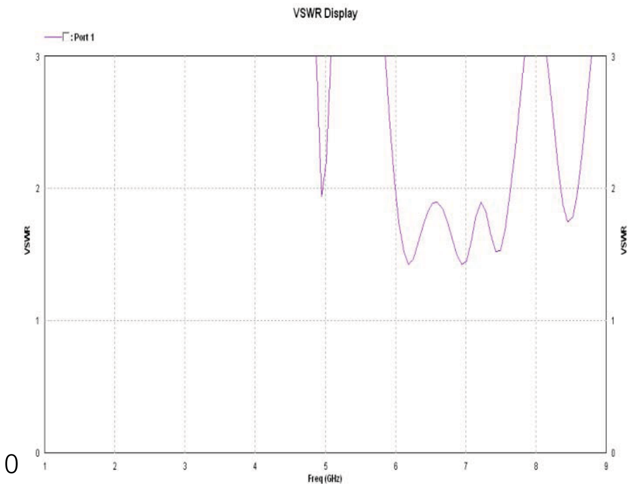

Figure 3.2.1 : VSWR

c) Radiation Pattern

The 3D radiation pattern of the antenna at the frequency of 6.52GHz is shown in the figure 3.3.1.The 2D radiation pattern(polar plot) of antenna for phi=0°,90°,170° is shown in the figure 3.3.2. It can be observed from the 3D radiation pattern that the antenna has a gain of 6.64dbi at the above frequency.

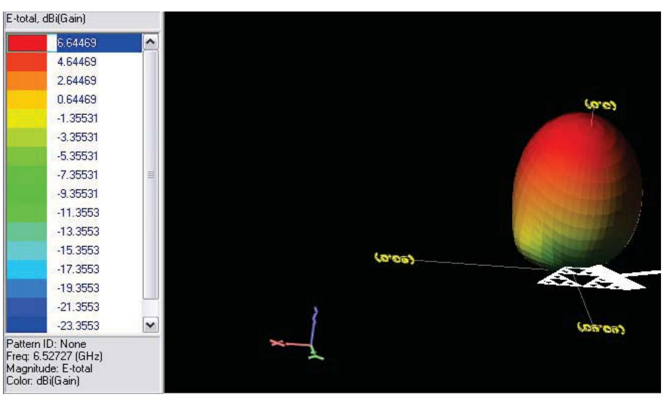

Figure 3.3.1 : 3D gain

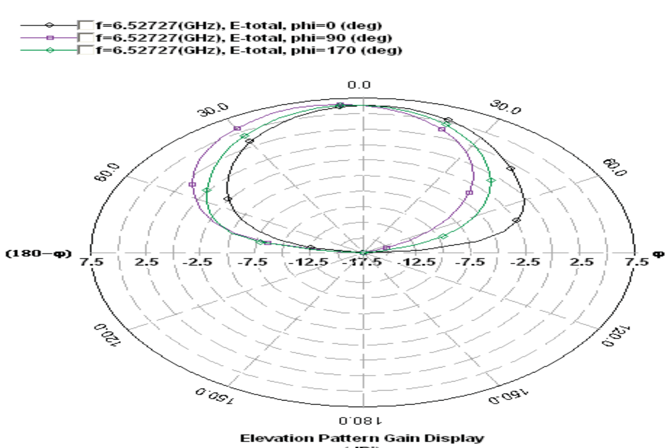

Figure 3.3.2 : Polar plot at 6.52 GHz

IV. Conclusion

From the simulated results, it can be inferred that the designed antenna can operate at three resonance frequencies and has bandwidth of 1.64 GHz and enhancement in bandwidth is 42.8% with a gain of 6dBi.Result shows that designed antenna has broadband behaviour. This is the overcome of the narrow banding behaviour of microstrip antenna. .

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Steady State Stability Analysis of Power System under Various Fault Conditions

By Md Multan Biswas , Kamol Kanto Das

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Abstract - Stability is an important constraint in power system operation and control. Power system stability is understood as the ability to regain an equilibrium state after being subjected to a physical disturbance. This paper presents steady state stability analysis of power system and its behavior in accordance with the locations of fault. Principal among these are the determination of system stability on the consideration of Eigen values in steady state condition. This provides appropriate strategy to have a quick decision on the system's steady state behavior. The simulation results show the severity of fault and help to make a quick decision that whether it is possible to get the system in normal operation or not.

Keywords : Power system, stability, infinite bus, Eigen value, power system stabilizer (PSS), MATLAB.

GJRE-F Classification: FOR Code: 090607

STEADY STATE STABILITY ANALYSIS OF POWER SYSTEM UNDER VARIOUS FAULT CONDITIONS

Strictly as per the compliance and regulations of :

Steady State Stability Analysis of Power System under Various Fault Conditions

Md Multan Biswas[α] , Kamol Kanto Das[Ω]

Abstract - Stability is an important constraint in power system operation and control. Power system stability is understood as the ability to regain an equilibrium state after being subjected to a physical disturbance. This paper presents steady state stability analysis of power system and its behavior in accordance with the locations of fault. Principal among these are the determination of system stability on the consideration of Eigen values in steady state condition. This provides appropriate strategy to have a quick decision on the system's steady state behavior. The simulation results show the severity of fault and provide information to make a quick decision that whether it is possible to get the system in normal operation or not.

Keywords : Power system, stability, infinite bus, Eigen value, power system stabilizer (PSS), MATLAB.

I. Introduction

The steady state stability of power systems has been and continues to be of major concern in system operation. Modern electrical power systems have grown to a large complexity due to increasing of interconnections, installation of large generating units, and extra-high voltage tie-lines etc. Steady state stability refers to the ability of the power system to regain synchronism after small and slow disturbance, such as gradual power changes [1].

Economic and operational factors make power systems to utilize utmost percentage of their transmission capacity and consequently operate close to stability limit with small margins. In such environment voltage instability is emerged as a major threat for power system security. At present most of electric utilities use the fast response excitation systems, faster relays and stabilizing devices to improve the system security margin. Power systems have become increasingly concerned world-wide with voltage stability and collapse problems [2]. A number of major voltage collapse phenomena have been experienced by utilities resulted in widespread blackouts [3]. In spite of dynamic nature of voltage instability, static approaches are used for its analysis based on the fact that the system dynamics influencing voltage stability are usually slow [4]-[6].

Again, fault may occur at various locations of a power system network such as (a) near the generator, (b) middle of the transmission line, and (c) near the infinite bus etc. Steady state stability problems use a very simple generator model which treats the generator as a constant voltage source. The solution technique of steady state stability problems is to examine the stability of the system under incremental variations about an equilibrium point. The methods of linear analysis can be used to determine whether the system will remain in synchronism following small changes from the operating point or not [7]. It is convenient to assume that the disturbances causing the changes disappear. The motion of the system is free; stability is assured if the system returns to its original state. Such a behavior can be determined in a linear system by examining the characteristic equation the system.

In all stability studies, the principle objective is to determine whether or not the rotors of the machines being perturbed return to constant speed operation. Obviously this means that the rotor speeds must depart at least temporarily from synchronous speed. In the past three decades, power system stabilizers (PSSs) have been extensively used to increase the system damping for low frequency oscillations. Worldwide the power utilities are currently implementing PSSs as effective excitation controllers to improve the system stability under various faults conditions [8]–[12].

The objective of this work is to analysis a simple and effective method for stability analysis of power system under different faulty conditions by considering Eigen values in steady state condition under MATLAB environment. This research paper is organized as follows. A brief description of the system is presented in Section 2. Section 3 discusses the synchronous generator model of the considered system while the excitation system is described in Section 4. Section 5 highlights some important issues for modern prime-mover governing system. Effect of small load changes of the system and associated state variables have been summarized in Section 6. System Eigen values which play important role in determining the power system stability have been discussed in Section 7. In section 8, computer simulations are performed using the MATLAB environment under different operating conditions. Finally, some concluding remarks have been highlighted in Section 9.

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II. Description of the System

The system consists of a synchronous generator connected to the infinite bus through the parallel transmission line as shown in Fig. 1. The synchronous generator is connected to a large interconnected electric power system networks. These networks have important characteristic that the system voltage at the point of connection is constant in magnitude, phase angle, and frequency. Such a point in a power system is referred to as an infinite bus. That is, the voltage at the generator bus will not be altered by changes in the generator's operating condition [1].

Faults at different sections of the power system are considered for small disturbances and the system behavior is observed. The faults may occur (a) at the generator bus, (b) middle of the transmission line, and (c) at the infinite bus. The system is sensitive to large disturbance and may not regain synchronism.

III. Synchronous Generator Model

In the two axis model, the transient effects are accounted while the sub-transient effects are neglected. The transient effects are dominated by the rotor circuits, which are the field circuit in the d-axis and an equivalent circuit in the q-axis formed by the solid rotor. An additional assumption is made in this model is that the stator voltage equations in terms of flux linkages derivatives are negligible compared to the speed voltage terms. The machine will thus have two stator circuits and two rotor axis. However, the number of differential equations describing these circuits is reduced by two since flux linkages derivatives are neglected in stator voltage equations [13].

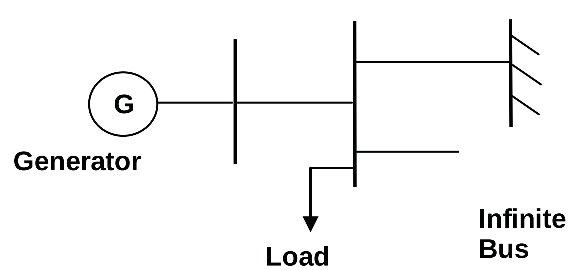


Fig. 1 : Connection of synchronous generator with an interconnected electric power system networks.

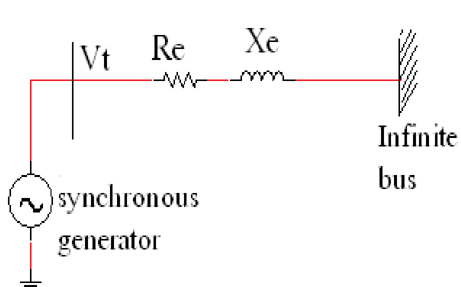


Fig. 2 : The equivalent circuit of the system.

The transient equivalent circuit of the generator is presented in Fig. 3. The following state equations have been considered:

Swing equation:-

$$\dot{\omega} = \frac{1}{M_g}\left(P_m - D_g\omega - P_e\right) \qquad (1)$$

Rotor angle equations:-

$$\dot{\partial} = \omega - \omega_0 \qquad (2)$$

IV. Excitation System

Each and every alternator in a power system is provided with an automatic voltage regulator. The primary function of automatic voltage regulator is to adjust the field current of the synchronous machine in an automatic way to maintain the terminal voltage at a desired value as the output of the machine varies.

Usually a high loop gain K_A renders the system unstable. Again with a small amplifier gain, automatic voltage regulator step response is not satisfactory. Thus, in order to improve the relative stability and steady state response, a stabilizing transformer is used. The input of the transformer is connected to the output of the exciter and the output is subtracted from the amplifier input. The output of the transformer is V_S. The required equations are:

$$\dot{E}_{FD} = \frac{1}{T_A}\left[-E_{FD} + \left(V_{ref} - V_t - V_s\right)K_A\right] \qquad (3)$$

$$\dot{V}_s = \frac{1}{T_F}\left[-V_s + E_{FD}\right] \qquad (4)$$

The armature transient voltage of direct axis and quadrature axis are expressed as,

$$\dot{E}_d' = \frac{1}{T_{qo}'}\left[-E_d' - \left(X_q - X_d'\right)I_q\right] \qquad (5)$$

$$\dot{E}_q' = \frac{1}{T_{do}'}\left[E_{FD} - E_d' + \left(X_d - X_d'\right)I_d\right] \qquad (6)$$

Here, E_{FD} is the field excitation voltage, T_{qo} is the d-axis transient time constant, and T_{do} is the q-axis transient time constant [3].

V. Prime-Mover Governing System

When the generator electrical load suddenly increases, the electrical power exceeds the mechanical power input. The power deficiency is supplied by the

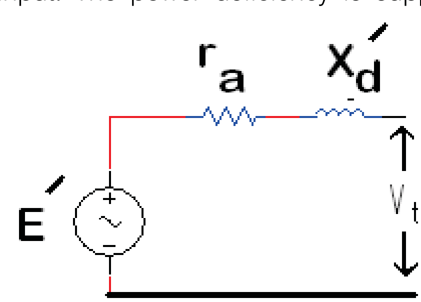


Fig. 3 : Transient equivalent circuit of the generator.

kinetic energy of the rotating system. The reduction in kinetic energy causes the turbine speed and consequently it causes the generator frequency to fall. The change in speed is sensed by the turbine governor which acts to adjust the turbine input valve to change the mechanical power output to bring the speed to a new steady state. The block diagram of modern speed governing system is shown in Fig. 4.

Here, the governor consists of two delays. Time constants of speed regulator T_{sr} = 0.1 sec. The other delay is control valve and other speed mechanism where the time constant T_{sm} = 0.2 sec. And T_{ch} is the time constant which usually lies in the range of 0.2 to 0.5 sec [3]. The equations that express the prime-mover governing system are given as,

$$\dot{P_R} = \frac{1}{T_{sr}}[-P_R + K_g(\omega_{ref} - \omega)] \quad (7)$$

$$\dot{P_h} = \frac{1}{T_{sh}}[-P_h + P_R] \quad (8)$$

$$\dot{P_{ch}} = \frac{1}{T_{ch}}[-P_{ch} + P_h + P_{m0}] \quad (9)$$

$$P_m = \frac{1}{T_{rh}}[-P_m + P_{ch} + \frac{K_{rh}T_{rh}}{T_{ch}}(-P_{ch} + P_h + P_{m0})] \quad (10)$$

VI. Effect Of Small Load Changes (Steady State Analysis)

Steady state studies use a very simple generator model which treats the generator as a constant voltage source. Steady state stability studies are less extensive in scope and involve one or just few machines undergoing slow or gradual changes in operating conditions. The criterion of small disturbance is simply that the perturbed system can be linearized about a quiescent operating point . In general , the response of a power system to impacts current oscillatory. If the oscillations are damped, so that after sufficient time has been elapsed the deviation or the change in the state of the system due to the small impact is small, the system is stable. On the other hand if the oscillations grow in magnitude or are sustained indefinitely, the system is unstable.

When the load changes on a power system with a little amount, the system state variables are expressed as:

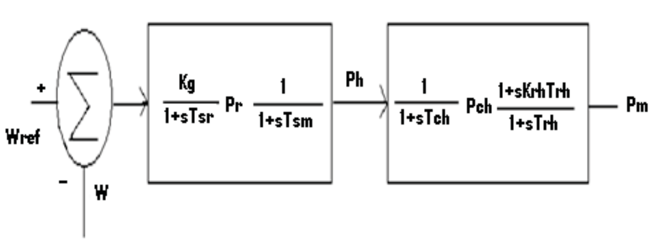


Fig. 4 : Block diagram of modern speed governing system.

$M_g \Delta\dot{\omega} = \Delta P_m - D_g \Delta\omega - I'_{do}\Delta E'_d - I'_{qo}\Delta E'_q - E'_{do}\Delta I_d - E'_{qo}\Delta I_q$

$\Delta\dot{\partial} = \omega_0 \Delta\omega$

$T_A \Delta\dot{E}_{FD} = -\Delta E_{FD} + K_A(-\Delta V_s - f_1\Delta E'_d - f_2\Delta E'_q + f_3\Delta I_d + f_4\Delta I_d)$

$-K_F\Delta\dot{E}_{FD} + T_F\Delta\dot{V}s = -\Delta V_s$

$T'_{qo}\Delta\dot{E}'_d = -\Delta E'_d - (X_q - X'_d)\Delta I_q$

$T'_{qo}\Delta\dot{E}'_q = \Delta E_{FD} - \Delta E'_q + (X_d - X'_d)\Delta I_d$

$T_{sr}\Delta\dot{P}_R = -\Delta P_R - K_g\Delta\omega$

$T_{sm}\Delta\dot{P}_h = -\Delta P_h + \Delta P_R$

$T_{ch}\Delta\dot{P}_c = -\Delta P_c + \Delta P_h$

$-K_{rh}T_m\Delta\dot{P}_c + T_m\Delta\dot{P}_m = -\Delta P_m + \Delta P_c$

Where $f_1 = \frac{V_{do}}{V_{to}}$, $f_2 = \frac{V_{qo}}{V_{to}}$, $f_3 = f_2X'_d - f_1r_a$, $f_4 = -f_1X'_d - f_2r_a$

Consideration:

$V_{ref} = 1\,p.u.$, $\omega_0 = 1\,p.u.$, and $V_s = 0$, because under steady state no stabilizing signal is required. the above equations can be expressed in matrix form as,

$$[F][\dot{x}] = [B][X] + [D][I_{dq}]$$
$$I_{dq} = G\;L\;X$$
$$\therefore F\dot{x} = (B + D\;G\;L)X$$
$$\therefore \dot{x} = F^{-1}((B + D\;G\;L)X)$$
$$\therefore \dot{x} = A\;X$$

Finally, Eigen values are determined using MATLAB.

VII. Eigen Value Sensitivity

Eigen values play important role in determining the power system stability. Table 1 shows the system Eigen values for two initial operating conditions for reheat steam turbine gain of K_{rh} = 0.3 and K_{rh} = 2.4. Electromechanical modes are denoted in bold. The value of K_{rh} may be changed to get the electromechanical mode of oscillation and K_{rh} varies from 0.3 to 0.4. For both P_0 = 1.0 p.u. and P_0 =1.2 p.u., the system real part of the oscillatory mode is small compared to the imaginary part. On the other hand, For P_0 = 1.2 p.u. and K_{rh} = 2.4, the system has positive real part. Because of positive real part, the system will be unstable.

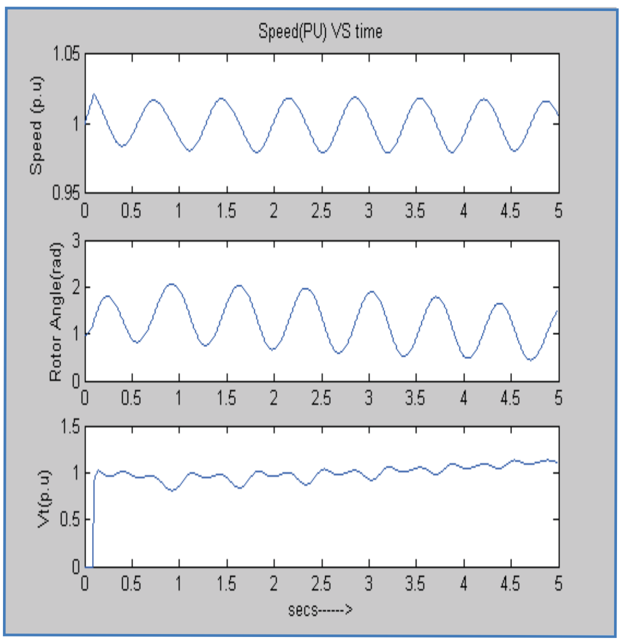
VIII. Computer Simulation

These computer simulations have been performed using the MATLAB environment under different operating conditions. The system performance is observed for different locations of the transmission line. Three case studies have been conducted.

Table 1 : System Eigen values

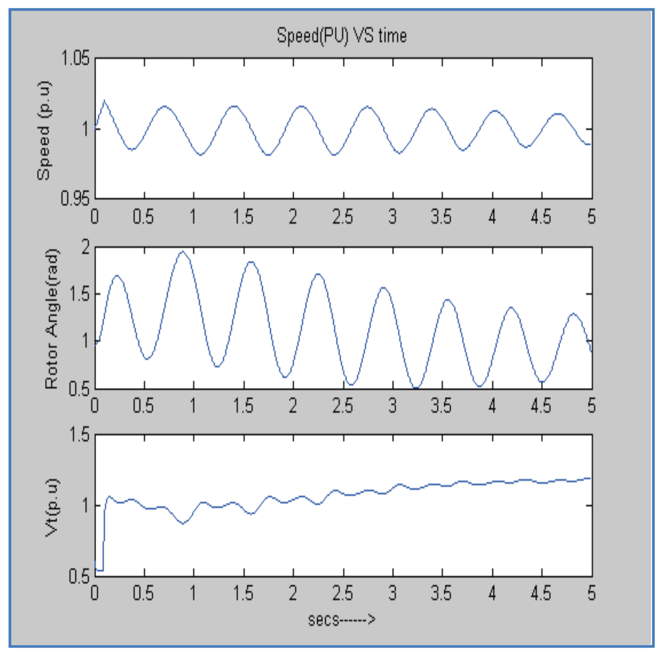
$P_0 = 1.0$ p.u. $K_{rh} = 0.3$	$P_0 = 1.2$ p.u. $K_{rh} = 0.3$	$P_0 = 1.0$ p.u. $K_{rh} = 2.4$	$P_0 = 1.2$ p.u. $K_{rh} = 2.4$
-217.8	-217.89	-217.8	-217.89
-41.55	-41.7	-41.55	-41.7
-19.94	-19.94	-19.45	-19.47
$-0.25 \pm 10.07j$	$-0.10 \pm 10.32j$	$+0.09 \pm 10.23j$	$+0.05 \pm 10.46j$
-10.22	-10.21	-11.63	-10.59
-4.9	-4.9	-4.32	-4.3
-2.3	-2.37	-2.25	-2.35
-1.49	-1.49	-1.51	-1.59
-0.12	-0.12	-0.13	-0.13

Case 1: Fault occurs at the generator bus



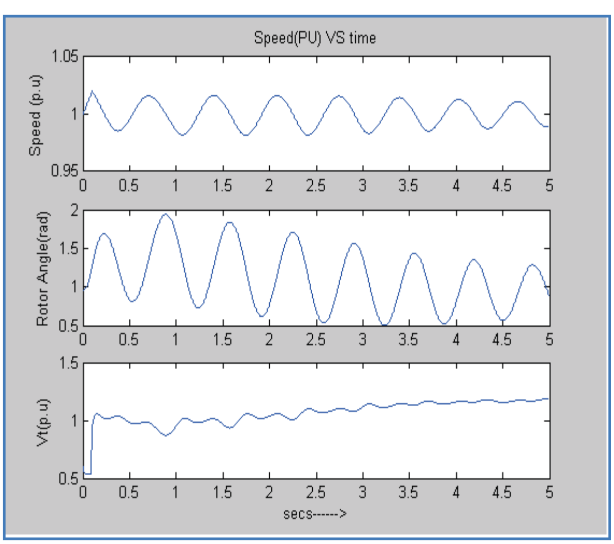
(a)

Case 2 : Fault occurs at the middle of the transmission line



(b)

Case 3 : Fault occurs at the infinite bus



(c)

Fig. 5 : System performances for different locations of faults.

IX. Conclusion

Two axis model of synchronous machine taking into account the effect of saliency is considered for steady state stability analysis. For small disturbance, it is possible to regain the stability of the system. This is observed by varying the air gap power P_e. If the forces tending to hold the machines in synchronism with one another are sufficient to overcome the disturbing forces, the system is said to remain stable. The gradual increase of the generator power output is possible until the maximum electrical power is transferred. This maximum power is referred to as the steady state stability limit. The most common boundary conditions are the terminal voltage and either the current I_a and the power factor or the generated power and the reactive power. In either case V_a, I_a and Φ (Power factor angle) are assumed to be known. In this paper, the steady state analysis is performed. The ten equations in section VI would be changed for small load changes. The initial values as well as Eigen values are calculated and finally computer simulation of the system is performed. For all cases, the initial power $P_e = 1.03$ is considered as the air gap power. It is observed from Fig. 5 (a) that fault at the generator bus is very much severe. It is impossible to regain the system into stable, because the speed of the rotor and the rotor angle is continuously oscillatory. Fig. 5 (b) demonstrates that fault at the middle of the transmission line is not much severe. In this case, the oscillation of the rotor angle and the speed reduces with respect to time. The system may come back into stable state. From Fig. 5 (c), it is seen that it is possible to regain synchronism. In a short time the system comes back into stable state.

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Appendix: System Data and Initial Conditions

All parameters are expressed in per unit (p.u) unless stated otherwise.

Generator and Transmission line:

Base: 160 MVA; 15 kV

Generator: 160 MVA, 15kV, 0.85 p.f.

Exciter: 375 V, 926 A

R_a=0.001096	X_d=1.7	X_d'=0.245
T_{q0}=0.075	T_{d0}=5.9	D_g=0
M_g=4.74	X_q'=.380	X_q=1.64

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FPGA Implementation of QMF for Equalizer Application of Wireless Communication Channel

By P.Harika , A.pravin
BVC Engineering College, Odalarevu, Amalapuram,India

Abstract - In this paper a Quadrature Mirror Filter is implemented in VHDL, for wireless communication applications. The Quadrature Mirror Filter (QMF) basically is a parallel combination of a High Pass Filter (HPF) and Low Pass Filter (LPF), which performs the action of frequency subdivision by splitting the signal spectrum into two spectra. The QMF implementation is carried out on FPGA platform. The Xilinx IP Core generator will be used for instantiating the standard Xilinx parts. Xilinx ISE will be used to carry out the synthesis and bit file generation. The obtained Synthesis Report for implemented QMF will be used to analyze the occupied area and power dissipation. The study and implementation will be aimed to realize the equalizer for wireless communication system. Modelsim Xilinx Edition (MXE) will be used for simulation and functional verification. Xilinx ISE will be used for synthesis and bit file generation. The Xilinx Chip scope will be used to test the results on Spartan 3E 500K FPGA board.

Keywords : *QMF bank, ISE, MXE, Adaptive Equalizer, FPGA, Analysis Bank, Synthesis Bank .*

GJRE-F Classification: *FOR Code: 090604*

FPGA IMPLEMENTATION OF QMF FOR EQUALIZER APPLICATION OF WIRELESS COMMUNICATION CHANNEL

FPGA Implementation of QMF for Equalizer Application of Wireless Communication Channel

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Keywords : QMF bank, ISE, MXE, Adaptive Equalizer, FPGA, Analysis Bank, Synthesis Bank .

I. Introduction

The importance of quadrature mirror filter banks in subband coding has been widely recognized and various analysis, design, and implementation issues pertaining to these filters have been intensively studied since the mid-1970. In this decade the wireless communication technologies are expected to grow multifold and spreading its usage in all communication segments. The latest processing techniques are enabling the communication system to work with longer distances, with less energy per bit. The channel equalization is an important step in all most all wireless communication receiver designs. Normal equalization techniques take long time for converging which can't be used for mobile technologies.

By virtue of the excellent coding and error propagation control capabilities of the sub band coding technique it has been used successfully in speech coding and image and video compression .A practical and efficient implementation platform for the sub band coding process is the quadrature mirror filter (QMF) bank. The QMF (quadrature mirror filter) based solution with sub band adaptive equalization can result less area solution, converges very fast, hence can meet the new generation mobile requirements. The FPGA based implementation can result in high speed processing hence the proposed architecture can work for wideband signals.

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II. Adaptive Equalization

An adaptive equalizer is an equalizer that automatically adapts to time-varying properties of the communication channel.It is frequently used for eliminating mitigating the effects of multipath propagation and Doppler spreading in adaptive equalization, the filters adapt themselves to the dispersive effects of the channel. That is the coefficients of the filters are changed continuously according to the received data. The filter coefficients are changed in such a way that the distortion in the data is reduced. The adaptive equalizer shown in fig.

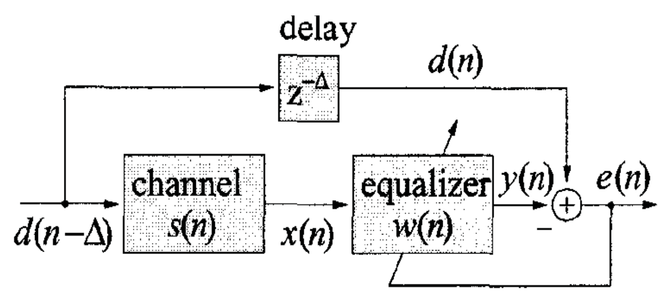

Fig.1 : Structure of Adaptive equalizer.

In this case ,the equalizer is placed after the receiving filter in the receiver. The Sequence x(n) is applied to the input of the adaptive filter.The output y(n) of the adaptive filter will be,

$$Y(n)= \sum_{i=0}^{m} w_i x(n-i)$$

The weights wi on the taps are basically adaptive filter coefficients.A known sequence d(n-Δ)is transmitted first.This sequence is known to the receiver.The response sequencey(n) is observed.The error sequence between the two sequences is calculated

$$e(n)=d(n)-y(n) \quad n=0,1,\ldots N-1$$

if there is no distortion in the channel,then d(n)and y(n)will be exactly same producing zero error sequence.

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III. Basic Principle

The basic principle for the sub band Adaptive filters is,adaptive equalization operating in the fullband, adaptive algorithms even with medium computational complexity take long time to converge.The filter lengths for fullband operation is very high which consumes high area.If the channel exhibits large spectral dynamics .which is likely in mobile applications then convergence time is even more. Adaptive filters working in sub bands the convergence time is less, hence update rate is high.The filter length is less for sub band equalizer approach. Further, the subband decomposition allows implementing QMF like high speed architectures.

(a) *Sub band adaptive equalizer*

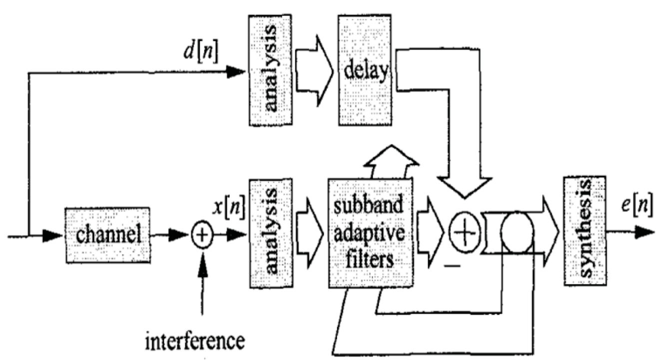


Fig.2 : Sub band adaptive equalizer.

(b) *Sub band filter section*

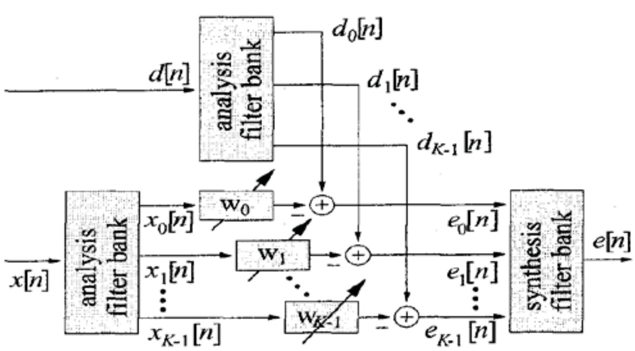


Fig .3 : Sub band filter section.

IV. Quadrature Mirror

The Quadrature Mirror Filter (QMF) basically is a parallel combination of a High Pass Filter (HPF) and Low Pass Filter (LPF), which performs the action of frequency subdivision by splitting the signal spectrum into two spectra. The general structure of a critically subsampled two-channel QMFbank is shown in Fig. 4.

It is a two channel sub band coding filter bank with complementary frequency responses. It consists of two sections.

1. Analysis section.
2. Synthesis section.

The analysis sub band filters have the transfer functions H0(z) and H1(z), and the synthesis filters are represented by G0(z) and G1(z). The input-output relation in the z-domain is given by

$$Y(z) = X(z)Tlin(z) + X(-z)Ealias(z) \qquad (1)$$

With linear (distortion) transfer function

$$Tlin(z) = \frac{1}{2}[H0(z)G0(z) + H1(z)G1(z)] \qquad (2)$$

and aliasing (distortion) transfer function

$$Ealias(z) = \frac{1}{2}[H0(-z)G0(z) + H1(-z)G1(z)] \qquad (3)$$

Aliasing distortions are completely eliminated by the choice

$$G0(z) = H1(-z) \wedge G1(z) = -H0(-z) \qquad (4)$$

If the analysis filters fulfill the requirement H0(z) = H1(−z), they are referred to as quadrature-mirror filters.

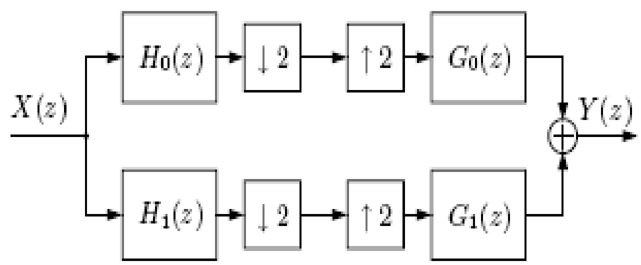


Fig.4 : General structure of a two-channel QMF bank.

The block diagram of two channel QMF is as shown in above Fig.. Here in this figure at the transmission end, the input signal x(n) is splitted into two subband signals using Analysis filters having equal bandwidth using the lowpass and highpass analysis filter HoCz) and HI Cz) respectively. Then these subband signals are decimated by factor of two. At the receiver end the decimated signal is first interpolated by factor of two and then passed through corresponding synthesis filters FoCz) and F I Cz) respectively. The outputs of the synthesis filters are combined to obtain the reconstructed signal y(n). This y(n) may not be perfect replica of x(n), due to; aliasing error or amplitude error or phase error. The elimination of aliasing effect or amplitude distortion or phase error can be achieved thereby resulting a perfect reconstruction of input signal at the output of QMF if the following conditions are satisfied by analysis filters HkCz) and synthesis filters FkCz)

1. The length L, of the window, wCn), is an integer multiple of the number of sub-bands.
2. The synthesis filters fkCn), is related to the analysis filters by a time-reversal.
3. FIR lowpass and highpass has linear phase.
4. The filter components satisfy the pairwise power complementary requirement .i.e the magnitude response of the filters satisfy the following .

Condition:-

Amplitude distortion can be elliminated completely, if above mentioned condition is satisfied. The normalized frequency response of this filter is as shown in Fig. Here the normalization is done with the total Bandwidth of our interest. From this it is clear that with two sub-bands as mentioned above the flat response can be obtained for the frequency band of interest i.e. almost flat response can be obtained for the entire frequency range of interest. In particular, perfect reconstruction is guaranteed for a filter bank with analysis filters, hkCn), and synthesis filters,

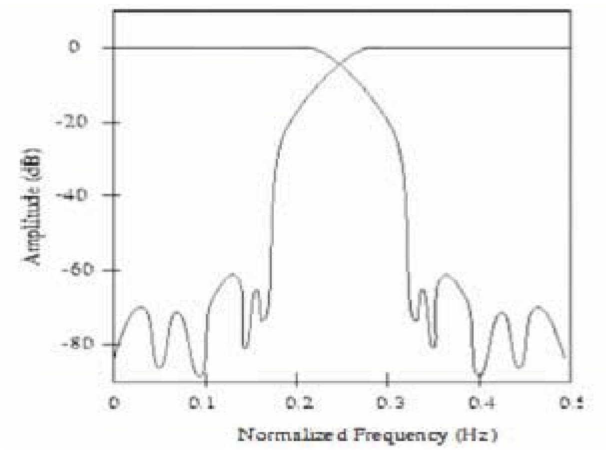


Fig.5 : Normalized Frequency Response of QMF Filter.

V. Applications

QMF finds wide applications in many signal processing tasks such as trans-multiplexing, equalizing wireless communication channels, sub-band coding of speech and image signals, sub-band acoustic echo cancellation.

VI. Results

a) Simulation Results

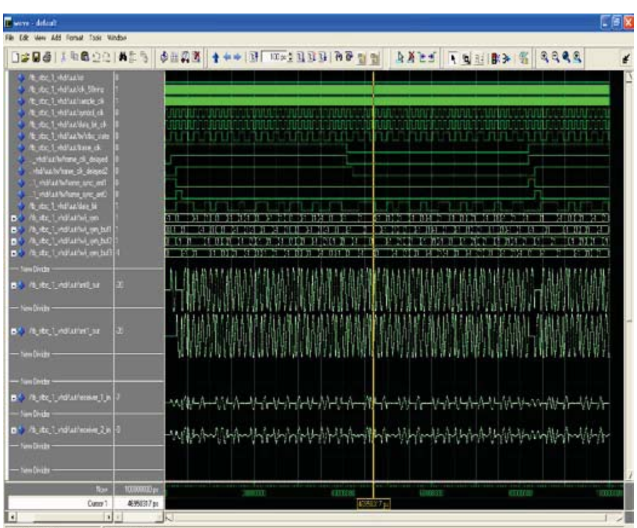


Fig .6 : Analysis bank

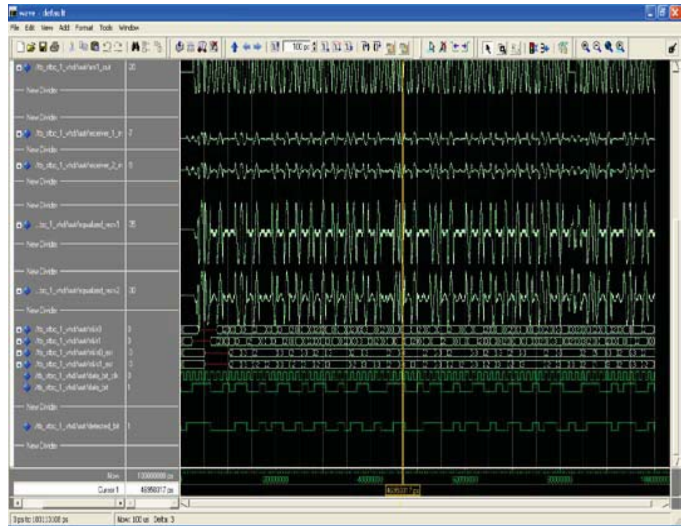
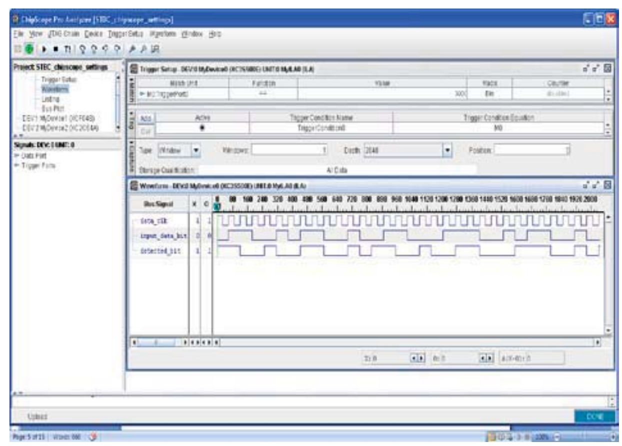
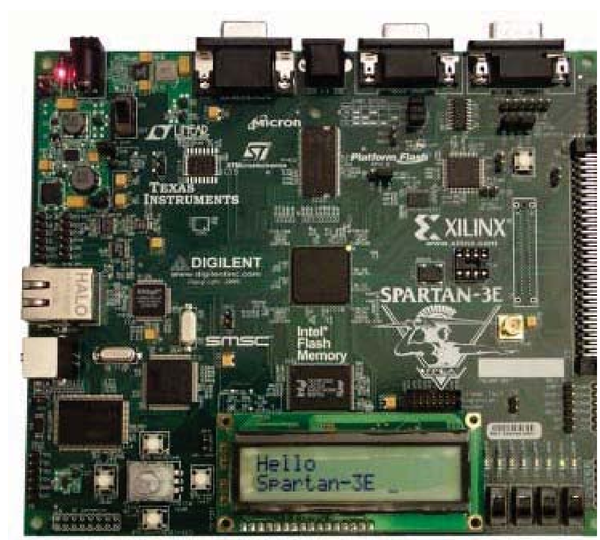


Fig.7 : Synthesis bank

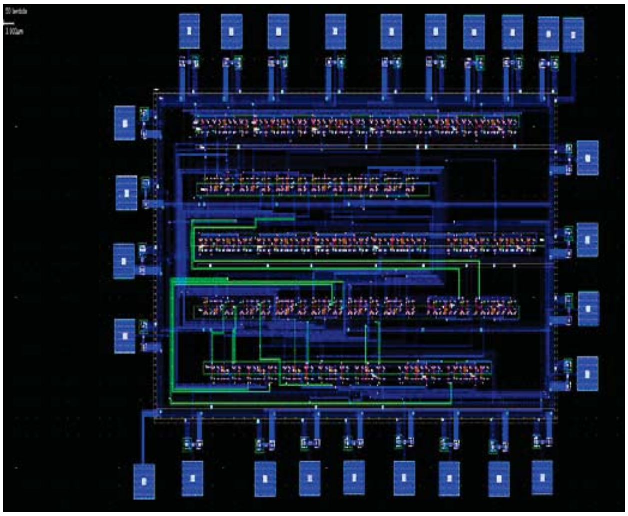
b) Chip scope Result



c) Spartan_3e



d) Floor Planning



VII. Conclusions

Here the QMF implementation for equalizer application of wireless communication channel is done and Modelsim Xilinx Edition (MXE) will be used for simulation and functional verification. Xilinx ISE will be used for synthesis and bit file generation. The Xilinx Chip scope will be used to test the results on Spartan 3E 500K FPGA board.

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Wideband Inverted-F Double-L Antenna for 5 GHz Applications

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Abstract - An Inverted-F Double-L (IFDL) antenna with Omni- directional radiation pattern in the azimuth plane is proposed. It provides an impedance bandwidth of 2.55 GHz (5000-7550 MHz) below 10dB, which easily covers the required universal 5GHz bandwidth for wireless local area network (WLAN), and worldwide interoperability for microwave access (WiMAX).Furthermore, the antenna has a simple structure and it occupies a small size of about 19×21. mm2. This antenna also provides lower gain variation with peak return loss of -35.14, -25.795 and - 22.37 dB at 5.2, 5.5 and 5.8 GHz respectively.

Keywords : IFA, low cost, wideband antenna, WLAN,WiMAX.

GJRE-F Classification: FOR Code: 291701

WIDEBAND INVERTED-F DOUBLE-L ANTENNA FOR 5 GHZAPPLICATIONS

Strictly as per the compliance and regulations of :

Wideband Inverted-F Double-L Antenna for 5 GHz Applications

Abu Naim Rakib Ahmed [α], Al-Ahsan Talukder [Ω], Debabrata Kumar Karmokar [β]

Abstract - An Inverted-F Double-L (IFDL) antenna with Omni-directional radiation pattern in the azimuth plane is proposed. It provides an impedance bandwidth of 2.55 GHz (5000-7550 MHz) below 10dB, which easily covers the required universal 5GHz bandwidth for wireless local area network (WLAN), and worldwide interoperability for microwave access (WiMAX).Furthermore, the antenna has a simple structure and it occupies a small size of about 19×21. mm2. This antenna also provides lower gain variation with peak return loss of -35.14, -25.795 and - 22.37 dB at 5.2, 5.5 and 5.8 GHz respectively.

Keywords : IFA, low cost, wideband antenna, WLAN, WiMAX.

I. Introduction

In recent years due to fabulous development of mobile wireless communication, systems such as digital notepad, notebook and so on required broadband connections with large transmission and receiver speeds through wireless local area network (WLAN).Generally, the 2.4 GHZ ISM band utilized by the IEEE 802.11b and 802.11g standards but in this case the WLAN equipment will suffer interference from baby monitors, wireless keyboards, microwave oven, Bluetooth devices and other appliances that use the same band. On the other hand, the other frequency spectrum allowed for WLAN (5 GHz) have much wide band width with fewer disturbances from other services. Moreover, 5 GHz network can carry more data than the 2.4 GHz.

So, to meet the condition of less interference the design of the antenna become more sophisticated which required having some special properties such as, small size, higher gain, Omni-directional radiationpattern and so on. In order to satisfy the above condition for 5 GHz band antenna, several antennas are proposed. a monopole antenna with a folded ground strips [1] has been proposed for WLAN application is capable to satisfy the whole 5GHz band but it is not small in size.

Some of the antennas are also provide full coverage of 5 GHz but they are in large size [2-6] or require a big ground plane [7-10].Although small size is achieved by antenna presented in the literature but they suffered by inadequate coverage in 5 GHz band [1,4,5,7,10] .

Therefore, in this article, we propose a compact wideband antenna for 5GHz Universal WLAN and WiMAX operations. From the simulation results, it provides a wider impedance bandwidth of 2.55 GHz (5000-7550MHz) which fully covers the 5.2/5.5/5.8 GHz bands. Moreover it also gives an omnidirectional radiation patterns with maximum measured peak antenna gains of 7.6, 7.14 and 6.53 dBi across the operating bands, respectively. Details of the proposed antenna design are described in this study, and the related results for the obtained performance operated across the 5.2/5.5/5.8 GHz bands are presented and discussed.

II. Antenna Geometry & Design

The design variables for this antenna are the height, width, and length of the top plate, the width and the location of the feed wire.In designing the broadband low profile antenna for 5 GHz WLAN/WiMAX applications, we examine the possibility of increasing antenna bandwidth, gain and maintaining the input impedance near about 50 Ω throughout the application bands with simplifying its structure. Method of moments (MoM's) in Numerical Electromagnetic Code (NEC) [11] is used for conducting parameter studies to ascertain the effect of different loading on the antenna performance to find out the optimal design where finest segmentation of each geometrical parameter are used. The antenna is assumed to feed by 50 Ω coaxial connector. In our analysis we assume the copper conductor and the antenna was intended to be matched to 50 Ω system impedance. Fig. 1 represents the basic geometry of the different antenna. For the simulation we consider printed circuit board (PCB) with permittivity of $\varepsilon_r = 2.2$, substrate thickness of 1.58 mm and the dimensions of the ground plane considered as 60 × 60 mm2. Fig. 1(a) represents the general IFA where one leg of IFA directly connected to the feeding and another leg spaced *s* from the ground plane. An additional L branch is added in structure 2 which shown in Fig. 1(b).In Fig 1(c) the limbs of L branch of structure 2 is extended and an additional L branch is coupled. Therefore structure 3 is termed as inverted-F Double-L antenna (IFDL antenna).

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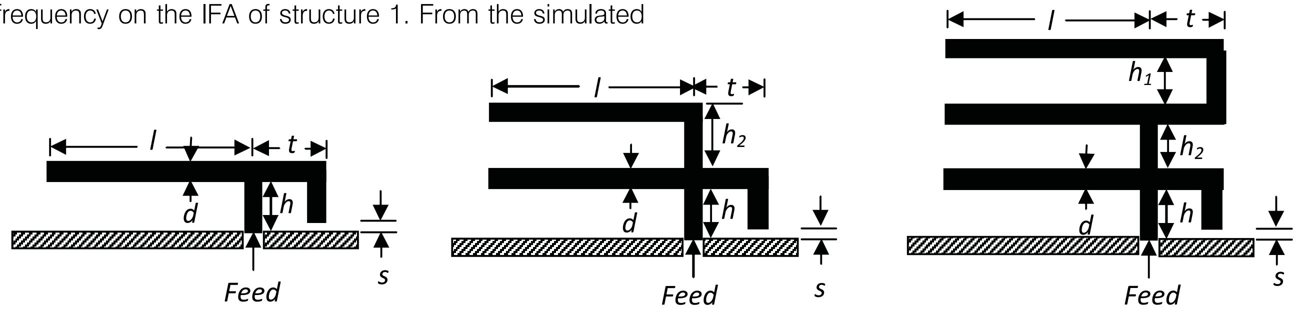
With the help of resonant frequency theory of IFA and impedance matching concept, we consider the dimension of the IFA *l=16 mm, t=5 mm, h=4 mm, h1=3 mm, d=2 mm* and *s=1 mm.* Fig. 2 shows the effects of length *l* on the return loss as a function of frequency on the IFA of structure 1. From the simulated results when *l=16 mm, t=5 mm, h=4 mm, h1=3 mm, d=2 mm* and *s=1 mm* the variation of return loss with frequency is not covering the whole 5 GHz operating band (frequency ranges 5150 – 5850 MHz) moreover the return loss is not so desirable.



(a) Structure 1, (b) Structure 2 , (c) Structure 3

Fig.1 : Geometry of different antenna structure.

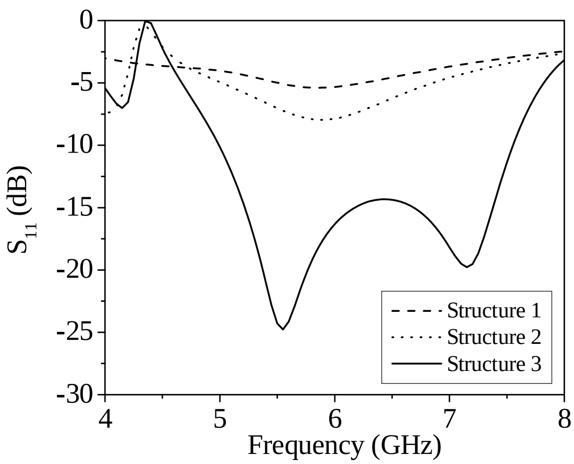


Fig.2 : Return loss as a function of frequency for different types of antennas.

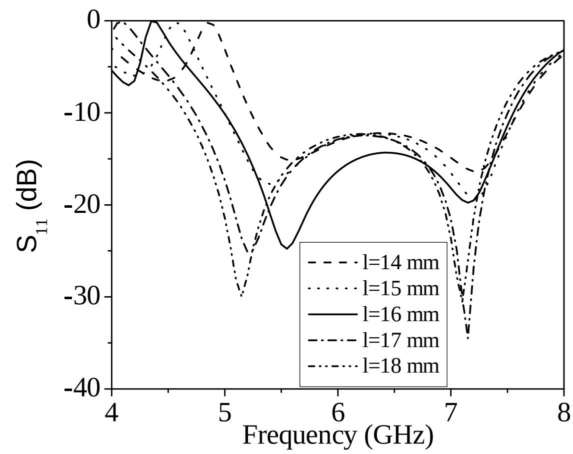


Fig.3 : Effects of length *l* on the return loss as a function of frequency on the antenna structure of Fig. 1(C).

After adding an additional L branch with the structure 1 the performance of the return loss improves slightly. However, when we added another L branch with structure 2, the performance of return loss improves dramatically. Fig. 3 shows the effects of *l* on the return loss of IFDL antenna, when *t=5 mm, h=4 mm, h1=4 mm, h2=4 mm, s=1 mm* and *d=2 mm*. From the figure we observed that, for considering return loss the best performance of the IFDL antenna is obtained when *l=16 mm although l=16 mm* and l=17 *mm* will cover the whole 5 GHz band, their return loss is not appreciable as *l=16 mm*. On the other hand, for *l=14 mm* and *l=15 mm* return loss is much higher than *l=16 mm.* Now maintaining *l=16 mm* we continue our advance analysis on the tap distance *t* as shown in Fig. 4 and we observe that when *t=5 mm* the IFDL antenna provides more negative return loss at the application bands than other values. Fig. 5 shows the effects of d on return loss when the tap distance *t=5 mm* and length *l=16 mm*. The best performance of return loss is obtained when *d=2 mm.*

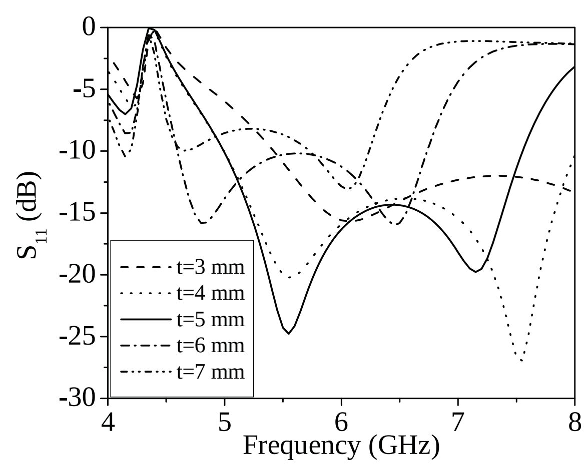


Fig.4 : Return loss as a function of frequency with the different tap distance *t* of the IFDL antenna of Fig.1(C) when *l=16 mm.*

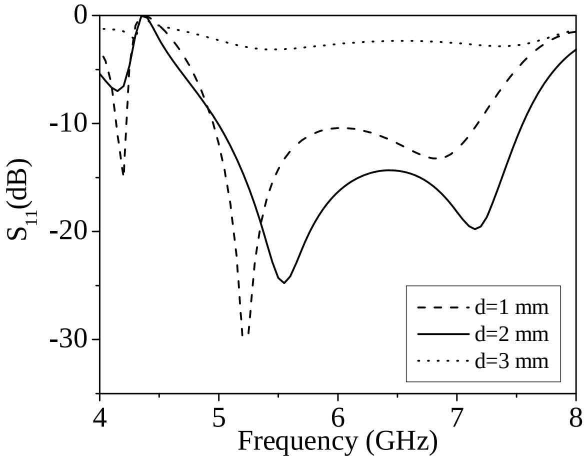


Fig.5 : Return loss as a function of frequency with different value of *d* of the IFDL antenna of Fig. 1(C) when *t=5 mm* and *l=16 mm.*

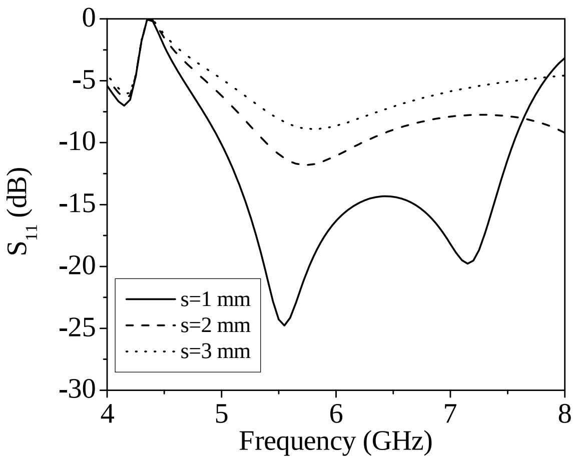


Fig.6 : Effects of spacing s on the return loss as a function of frequency on the antenna structure of Fig. 1(C)

From Fig. 6 we observe that the IFDL antenna provide best return loss performance when space from feed line s*=1 mm*. From overall analysis we see that IFDL antenna provides best performance for the desired applications. The optimized dimensions of the proposed IFDL antenna are listed in Table I.

Table 1 : Optimized dimensions of the proposed antenna

<table>
<tr><th>Antenna Name</th><th>Antenna Parameters</th><th>Values (mm)</th><th>Dimension (mm^2)</th></tr>
<tr><td rowspan="7">IFDLA</td><td>l</td><td>16</td><td rowspan="7">19×21</td></tr>
<tr><td>t</td><td>5</td></tr>
<tr><td>h</td><td>4</td></tr>
<tr><td>h_1</td><td>4</td></tr>
<tr><td>h_2</td><td>4</td></tr>
<tr><td>d</td><td>2</td></tr>
<tr><td>s</td><td>1</td></tr>
</table>

III. NUMERICAL SIMULATION RESULTS

The IFDL antenna provides a wide impedance bandwidth of 2.5 GHz (5000-7550 MHz) which fully covers the 5.2/5.5/5.8 GHz bands. Moreover, the IFDL antenna has the return loss appreciable than the commonly required 10 dB level. Fig. 7 and Fig. 8 show the variation of voltage standing wave ratio (VSWR) and return loss respectively. The Peak value of return loss is -14.5, -24.2 and -19.2 dB respectively. The value of VSWR of IFDL antenna varies from 1.12 to 1.55 within the operating band and obtained result indicates that the variation of VSWR is very low and it is near to 1 as shown in Fig. 7. Fig. 9 illustrates the gain of IFDL antenna. The peak gains of IFDL antenna is 7.6, 7.14, and 6.53 dBi with a very small gain variation within the 10 dB return loss bandwidth at 5.2, 5.5 and 5.8 GHz band respectively, which indicates that the antenna has stable gain within the every separate operating bandwidth.

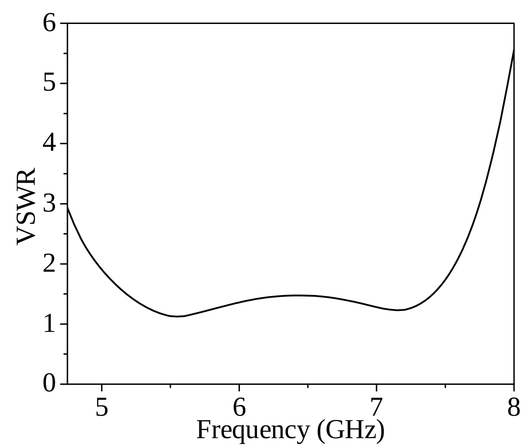


Fig.7 : VSWR variation of IFDL antenna with frequency.

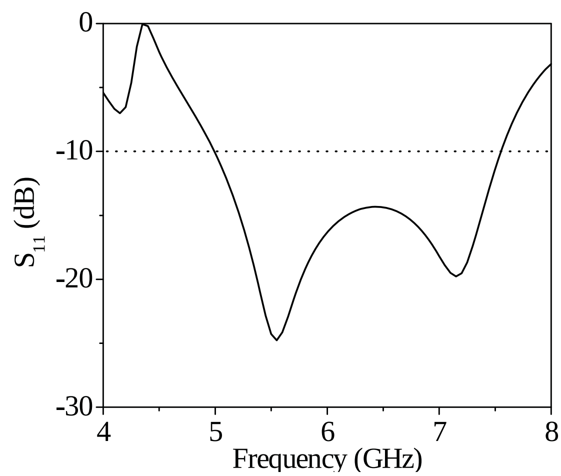


Fig.8 : Return loss variation of IFDL antenna with frequency.

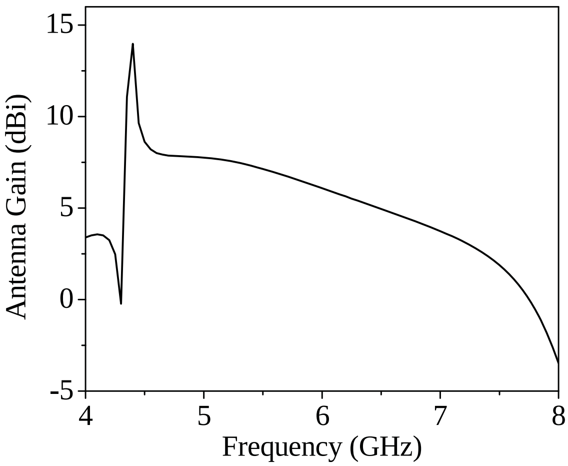


Fig.9 : Total gain variation of IFDL antenna with Frequency.

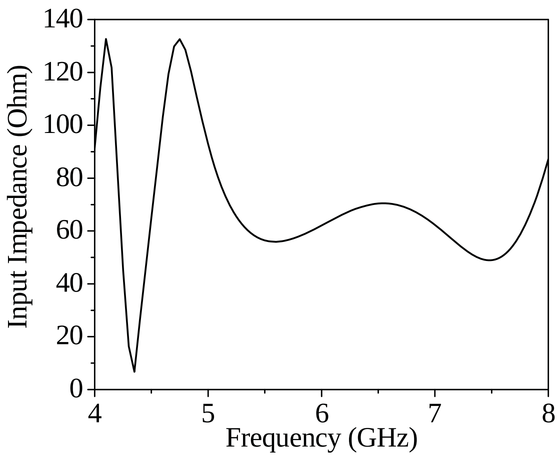


Fig.10 : Impedance variation of IFDL antenna with frequency.

Fig. 10 represents the antenna input impedance variation and Fig. 11 represents the antenna phase shift causes due the impedance mismatch as a function of frequency. From the obtained results, the input impedance of IFDL antenna is 69.05, 56.45 and 57.94Ω at 5.2, 5.5 and 5.8 GHz so the input impedance of the proposed antenna is near about 50 Ω. Also, from the simulation study, the antenna offers a phase shift of -11.2^0, -0.8^0 and 9.1^0 respectively. Therefore, phase shift of IFDL antenna closer to 0^0 all over the antenna bandwidth. A comparison in gains between the proposed (IFDL antenna) and reference antennas (Inverted-F antenna) are listed in Table II. From the table it has been observed that a significant amount of improvement resulted by IFDL antenna. A great progress experienced in return loss, VSWR, input impedance and phase.

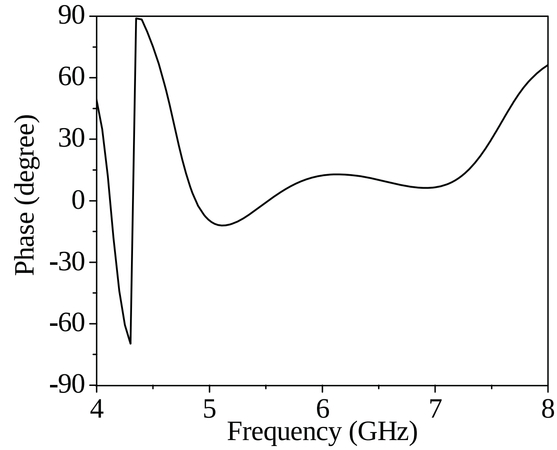


Fig.11 : Phase variation of IFDL antenna with frequency.

Figs. 12 to 14 show the normalized radiation patterns of IFDL ANTENNA at 5.2, 5.5 and 5.8 GHz bands respectively. Normalized radiation patterns for three resonant frequencies are shown as: total gain in Hplane and E-plane. The antenna's normalized total radiation in E and H-plane is almost omnidirectional at the 5 GHz WLAN and WiMAX applications. One of the significant advantages of symmetrical radiation pattern as seen from Figs. 12, 13, and 14 is that the maximum power direction is always at the broadside direction and does not shift to different directions at different frequencies.

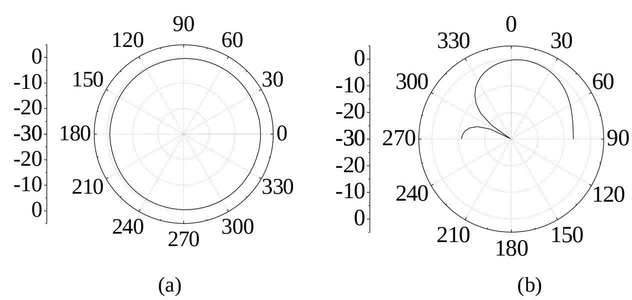


Fig.12 : Radiation pattern (normalized) (a) Total gain in E-plane and (b) total gain in H-plane of IFDL antenna at 5.2 GHz.

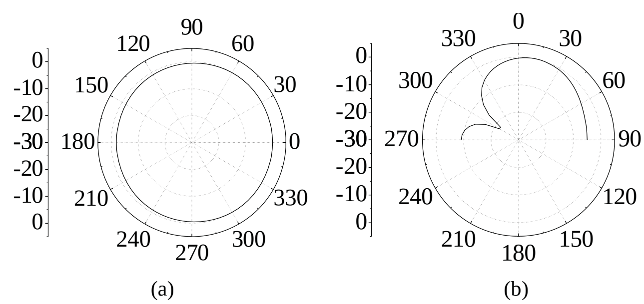


Fig.13 : Radiation pattern (normalized) (a) Total gain in E-plane and (b) total gain in H-plane of IFDL antenna at 5.5 GHz.

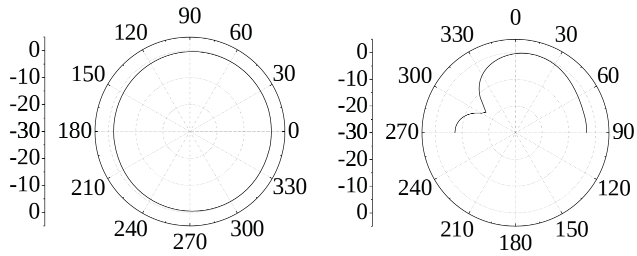


Fig.14 : Radiation pattern (normalized) (a) Total gain in E-plane and (b) total gain in H-plane of IFDL antenna at 5.8 GHz.

Table 2 : Comparison between the IFDL and IF Antenna

Antenna Parameter	IFA			IFDL		
	5.2 GHz	5.5 GHz	5.8 GHz	5.2 GHz	5.5 GHz	5.8 GHz
VSWR	4.08	3.57	3.33	1.46	1.12	1.24
Peak Gain (dBi)	7.26	7.06	6.78	7.62	7.14	6.50
Input Impedance (Ω)	45.46	20.2	15.2	69.0	56.4	57.9
Return Loss (dB)	-4.34	-5	-5.4	-14.5	-24.2	-19.2
Phase (Degree)	-57.9	-55	-26	-11.1	0.85	9.16

IV. Conclusion

In this paper we presented an Inverted-F Double-L (IFDL) antenna design. The antenna provides a sample structure with small area of 19×21 mm^2. In addition, it also ensures nearly omnidirectional radiation patterns with incredibly high gain 7.6, 7.14, and 6.53 dBi across the 5.2, 5.5 and 5.8 GHz operating bands respectively. The improvement of size, input impedance, bandwidth, gain and radiation is achieved by this structure which is suitable for WLAN and WiMAX applications.

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Method to Minimize Data Losses in Multi Stage Flip Flop

By N. Suresh Kumar, D.V. Ramakoti Reddy,Anil Patro,K.V. Ramana Rao,I. Krishnarao
GITAM University,Visakhapatnam, India

Abstract - In complex digital circuits the clock arrives at next stages before the data pulses arrives to the next stage. The clock pulse must be inserted to activate the digital circuits at any stage starting from first stage. But due to unsynchronization between clock pulse and data there is a chance of miss hitting in the next stages. This leads improper data transmissions in complex systems. It creates data losses in transmission. In the present work a gate controlled clock scheme is proposed to increase data hitting ratio.

Keywords : clock, Synchronization, data propagation, registers, flip flop.

GJRE-F Classification: FOR Code: 090604, 291703

METHOD TO MINIMIZE DATA LOSSES IN MULTI STAGE FLIP FLOP

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Method to Minimize Data Losses in Multi Stage Flip Flop

N. Suresh Kumar[α], D.V. Ramakoti Reddy[Ω], Anil Patro[β], K.V. Ramana Rao[ψ], I. Krishnarao[¥]

Abstract - **In complex digital circuits the clock arrives at next stages before the data pulses arrives to the next stage. The clock pulse must be inserted to activate the digital circuits at any stage starting from first stage. But due to un-synchronization between clock pulse and data there is a chance of miss hitting in the next stages. This leads improper data transmissions in complex systems. It creates data losses in transmission. In the present work a gate controlled clock scheme is proposed to increase data hitting ratio.**

Keywords : clock, Synchronization, data propagation, registers, flip flop.

I. Introduction

In light weighted circuits, contain fewer flip flops the problem may not arise. But the circuits with complex logic circuit with large number of flip-flops may face these types of problems. Because the complex logic circuits cause some delay to propagate the data from one flip flop to other flip flop or from one stage to other stage. In the present paper flip flops and delay logics are considered to describe the problem. Delay elements are often added to improve performance of a wave-pipelined circuit by reducing the delay difference of the longest and the shortest paths [1]. Unfortunately, precise delay elements that realize the exact delay needed is difficult to obtain. Instead simple logic gates are used for delay balancing, thereby providing more feasible and accurate circuit path delay control under the Min/Max delay model. A heuristic is developed to insert a sufficient number of latches into a combinational circuit to achieve a specified clock cycle time. There are already some existing methods effectively working to improve the data quality in terms of accuracy in propagation [2][3][4][5]. T. Feng proposed new wave pipeline design to achieve faster Clock Cycle Timing (CCT) [2] than the conventional pipeline methods. The author T Feng4drt wave pipeline can achieve at least a 48% performance enhancement on clock cycle time compared with the conventional wave pipeline.

This paper presents a new design method for combinational circuits with focus on circuit speed optimization. Today's high speed circuit and advanced fabrication technology facing seviour problem from delay uncertainty an extremely important issue in circuit design. The proposed method the speed optimization achieved with better Clock cycle scheme. By this intrinsic advantage of the proposed method over conventional methods, the proposed new scheme can achieve a better clock cycle than conventional methods.

The percentage of propagation error can be bringing to minimum level which is almost zero with the enhanced technology. In the conventional pipeline system it is facing problems due to improper synchronization of clock pulses. This is a universal problem in all the digital systems mostly called clock skew. The system clocking must be such that the output data is clocked after the latest data has arrived at the outputs and before the earliest data from the next clock cycle arrives at the outputs. In the present work a new system is proposed in the path of the clock to remove or reduce the clock skew. There are already few methods effectively working on clock skew such as wave-pipelining [5][6] and Me-synchronous pipeline [3] methods. The equalization of path delays comes as a new challenge for the design of wave-pipelined systems. Different clock signal paths can have different delays for a variety of reasons [7]. Differences in delays of any active buffers within the clock distribution network may cause un-synchronization of data and clock in double buffer method and wave pipeline method. And it is difficult to identify exact delay value without which the pipe line cannot perform 100% propagation.

II. Enhanced Method

In the present method simple logic gates are used in clock path to achieve higher data rates and accurate data propagation. In the present circuit the clock pulse applied to the next flip flop only when the first flip flop is ready to transmit the data wave to the next flip flop. In the present work an 8bit four stage circuit is built to test the data rates. In simple combinational circuits with little number of latches, the data propagation path is almost equal to the clock propagation path as shown in figure1. The output will follow 100% with the input. But when the stages increase in the combinational circuit with more logics and latches the propagation length of the data path will be long when compared with clock path as shown in figure2. In this crucial period it is difficult and highly impossible to get exact input data match with the output in conventional circuits.

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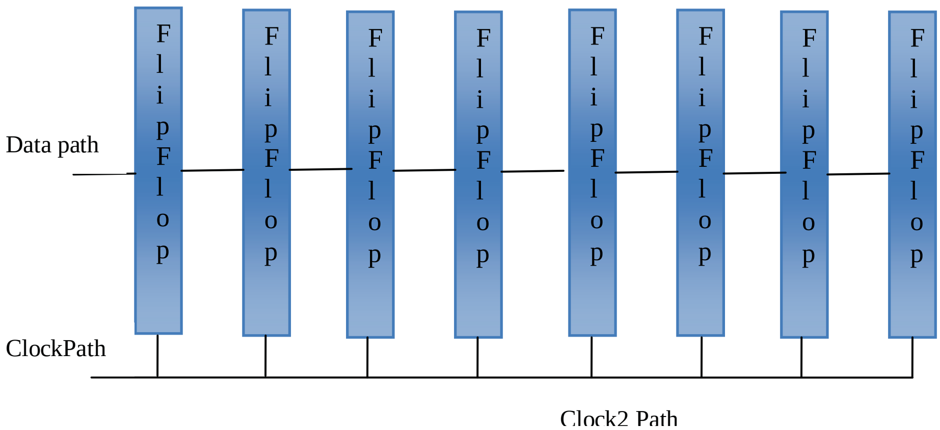

Figure 1 : Simple Combinational Circuit.

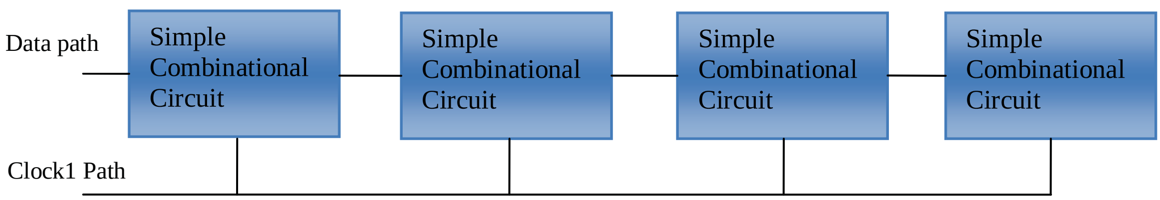

Figure 2 : Complex circuits having more logic.

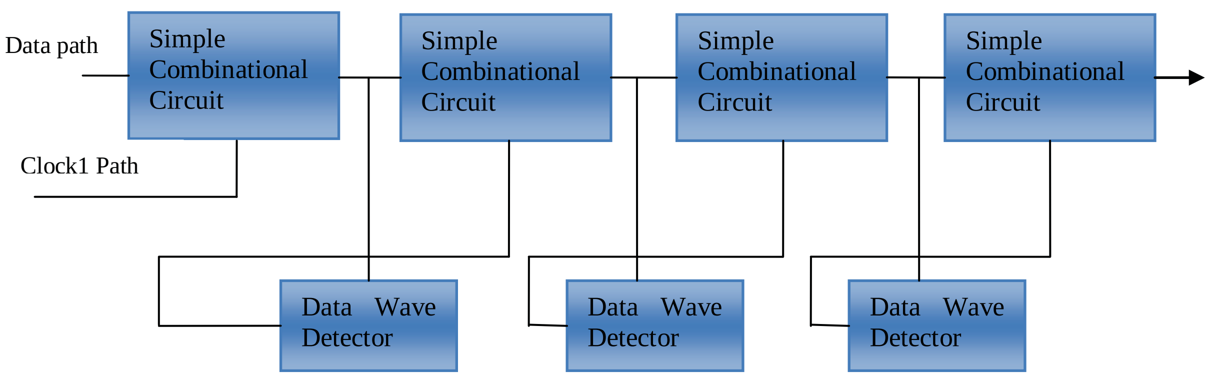

Figure 3 : The proposed Method with new clock Scheme.

The problem can be solved with new method as shown in figure 4. As the clock1 set the first stage of the circuit the data will be fed to the first stage. When the first stage data arrives at the output and ready to send to second stage the data wave detector detects the data pulse at output of the first stage and enables the second stage by clock2. Then only the first stage output will be forwarded to the next stage. Without clock2 the stage1 data cannot be transmitted to second stage, although it is arrived at output. The width of clock pulse maintained less when compared with data pulse to detect individual data pulse. The hardware connections for the same are shown in figure4 and the simulations results are shown in figure5. While the data passing from one stage to next stage, the second data travels through the internal logic of the circuit.

$$T_{wclk.n} \leq D_{wclk.n}$$

$$D_{prop.delay} \geq (T_{clk\_set.n} + D_{trav(n->n+1)})$$

$$D_{prop.delay} = D_s + D_h + \Delta_{clk}$$

s

Where, $T_{wclk.n}$ = The width of Clock signal applied at nth stage

$D_{wclk.n}$ = The width of Data wave

$D_{prop.delay}$ = The time delay taken to propagate data

$T_{clk\_set.n}$ = The clock signal used to set nth stage

$D_{trav(n->n+1)}$ = Delay produce in travelling data from nth stage to (n+1) stage

D_s = Data set time at each component of the individual stage

D_h = Data hold time in each component of the individual stage

Δ_{clk}= Clock skew

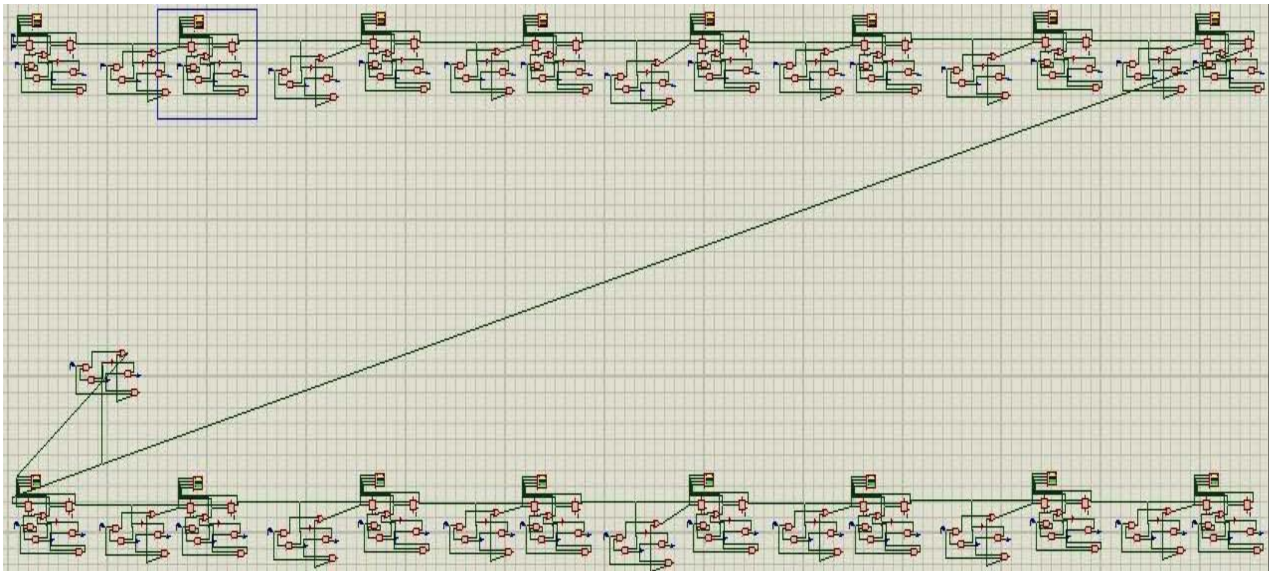

Figure 4 : Hardware Circuit Design of Eight bit Four Stage Circuit.

III. Results

The hardware is tested and simulations are verified in the software Proteus. In the figure 5 the yellow colour pulse represents clock1 and blue colour represents clock 2 applied at each stage. The input data is represented with green colour and output data is represented with pink colour at each stage of the designed circuit. In this diagram the first green and pink colour waves represent the input and output of the individual flip flop of first stage of the circuit. In the first stage the data input and output are in same phase. They appear at same clock pulse in the timing diagram. But in the second stage it is different. The second green and pink colours follow different clock phases unlike first green and pink colours. That means in the second phase the input and output appear in different phases of the clock. Because the data arrived at second stage input is after crossing logic circuit between two stages. So it took one clock pulse to come input pin of the second stage. And the clock pulse clock2 arrives after one clock pulse. So the output appears after one clock pulse after the input appears at second stage. That is the output will appear at second stage after two clock pulses after the first input appear at first stage. At the same time, while the second stage processing the first data wave the first stage receives the second data wave. That means while processing the one data wave the circuit can fetch second data wave. In the same way while the third stage processing the first data and second stage processing the second data wave the first stage will try to fetch the third wave.

Figure 5 : The Simulation results of Eight bit Four stage combinational Circuit.

IV. Conclusion

A new clock scheme is implemented for higher data rates. Parallel processing can be done with new clock system. High speed data can be read through the stages by simultaneous operations, fetching and processing through logic circuit. In the circuit the clock skew is almost minimized when compared to old methods. An eight bit four stage combinational circuit is designed to achieve accurate data.

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VHDL Design of FPGA Arithmetic Processor

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Abstract - This paper involves the design and development of a single chip VHDL FPGA processor which performs all arithmetic and logical functions and the output is displayed by means of LCD interface. This processor can perform 2n number of operations, where n is the number of control bits. In this design, a 5 bit control input is used so that the processor is capable of performing up to 32 operations. The chip is designed to execute 21 operations for different specified functions and 11 more operations can be worked on for improvements and future works. Two data with a size of 8 to 16 bits can be applied as input and the results are obtained on 4 to 8 hexadecimal digits carrying 32 bits in all. A status flag is also designed with the features such as indication of overflow, carry, borrow and zero value. To implement the above design, Very High Speed Description Language simulation is required which can be performed using Altera or Xilinx softwares. Once the program has been developed, the authors demonstrate the feasibility of the proposed design by incorporating it into a FPGA chip and the required hardware can be brought into effect. The state of each output bit is shown by using Light Emitting Diodes. Based on users needs, more features can be added to the designed hardware without hindering the implemented one.

Keywords : VHDL, FPGA, Processor, Chip, Arithmetic, LCD, Light Emitting Diodes, overflow, carry, borrow.

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I. Introduction

This paper deals with the design methodology of a FPGA Arithmetic Processor using VHDL to enhance the description, simulation and hardware realization. The design and implementation of FPGA based Arithmetic Logic Unit is of core significance in digital technologies as it is being an integral part of all microprocessors. As the name suggests, this is a system which is capable of performing not only arithmetic operations but also computes logic functions and provides the output through gating circuitry. All the modules described in the design are coded using VHDL which is a very useful tool with its degree of concurrency to cope with the parallelism of digital hardware. The top-level module connects all the stages into a higher level. Once identifying the individual approaches for input, output and other modules, the VHDL descriptions are run through a VHDL simulator, followed by the timing diagrams for the verification, working and performance of the above design along with the hardware implementation that shows the appropriateness of the design.

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II. Rationale

An early design involved in the computations of arithmetic and logical operations were complex and found to be time consuming. The circuitry needed to develop such an ALU of required specifications by conventional approach will lead to thousands of gates, transistors, resistors, capacitors, inductors and other digital components. The implementation of such a system raises major questions in the shape of its integration and optimization. These problems have been eliminated in this project by the use of Field Programmable Gate Array (FPGA) technology and by Hardware Descriptive Language (HDL). Since the feeding units are of binary nature and output of Hexadecimal, the complex and time consuming computations in the earlier methods are eliminated. The software interface along with the advanced options like graphical blocks, chip design and planner reduces the complexity and increases the ease of computations.

III. Technical Work Preparation

The organization and designing of this process is put forth by various tools. These tools and methods are significant in differentiating a successful one with the one carrying loop holes and discrepancies. In the present case, ALU is bricked up using synthesized operations in the form of objectives and broader aspects. The organization chart for the paper design that is needed to implement is shown in Fig. 1.

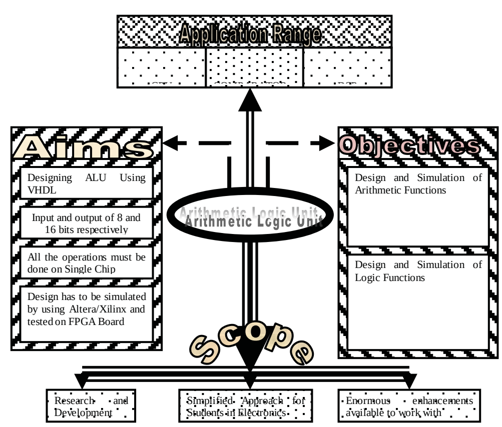

Fig.1 : Organization chart of the paper design with aims and objectives.

a) System Overview

This paper design has been embodied by many separate sub-systems. Amongst them operational design, Software design and Hardware design are of central emphasis.

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b) Operational overview

The operational overview deals with two kinds of operations which an ALU can perform. First part deals with arithmetic computations and is referred to as Arithmetic Unit. It is capable of addition, subtraction, multiplication, division, increment and decrement. The second part deals with the Gated results in the shape of AND, OR, XOR, inverter, rotate, left shift and right shift, which is referred to as Logic Unit. The functions are controlled and executed by selecting operation or control bits. A select input of 5 bit size that will accommodate up to 32 operations is sufficient to achieve the objectives. The operations selected by the Control Unit are shown in the Fig. 2. Arithmetic part is quite complex as compared to logic unit and involves an additional carry input. Multiplication and Division also increases the complexity of ALU. In the Logic Block, gates such as AND, OR, XOR and NOT operations are shown. Logic Block of ALU does not need as many gates as required in Arithmetic Unit and if done separately, the LOGIC unit can be implemented using Complex Programmable Logic Devices (CPLD) or other Programmable Logic Device (PLD) technologies instead of using FPGA.

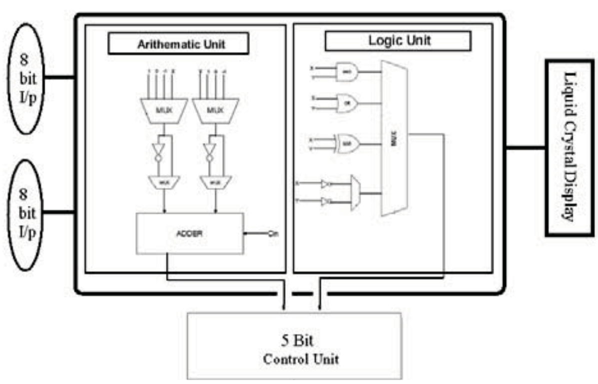

Fig.2 : General operation – ALU sub-blocks and control units using multiplexers

c) Software Overview

This paper capitalizes on the digital phenomenon; therefore software design draws most of the attention. The VHDL software interface used in this design reduces the complexity and also provides a graphic presentation of the system. The key advantage of VHDL when used for systems design is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires). This software not only compiles the given VHDL code but also produces waveform results. Graphical blocks, chip design and planner are the advanced options available and are used in the software mentioned. Altera's Quartus II and Xilinx webpack are few of the sophisticated Computer Aided Design (CAD) tools to perform the compilation and simulation of any logic circuit design.

d) Hardware Overview

The fundamental building block of ALU is shown in Fig. 3. Here bold dots (dip switches) indicate the inputs to an ALU which are selected by the user. The input can either be 1 or 0 indicating 5V and 0 V respectively. A LCD is used to display 16 bit output, whereas * indicates LEDs which are used to show the status of carry out, overflow, borrow and zero. The VHDL code which implies the hardware part of ALU is downloaded on FPGA processor using JTAG cable interfacing PC and the hardware element.

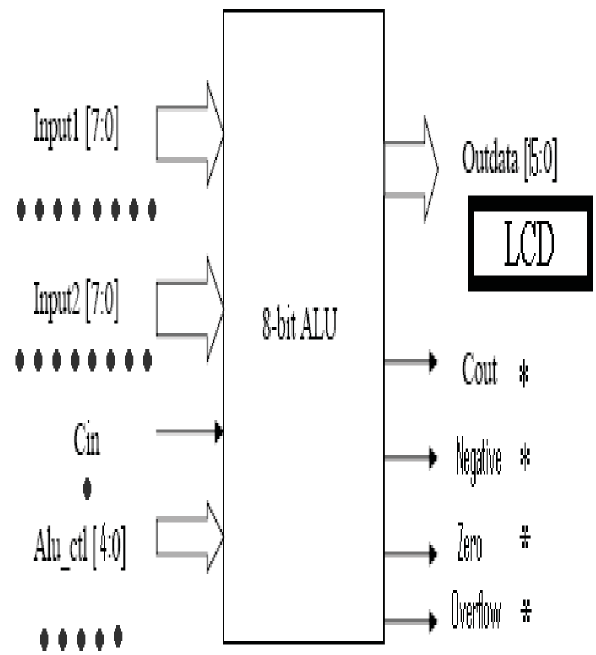

Fig.3 : Hardware representation of an 8-bit ALU.

A final point is that when a VHDL model is translated into the "gates and wires" that are mapped onto a programmable logic device such as a CPLD or FPGA, and then it is the actual hardware being configured, rather than the VHDL code being "executed" as if on some form of a processor chip.

IV. Methodology

Strategizing methods are designed by using part by part approach also known as "Divide and Conquer" or "Bit Slice". This approach provides a convenient method of operation and hence smaller blocks can be easily managed with ease as compared to the larger units.

a) *Graphical Splitting*

In this method, an ALU is chopped into several segments each incorporating its specific operations. A model of this technique containing Arithmetic, Logic, Multiplexer and Shift and Rotate Units are shown in Fig.4.

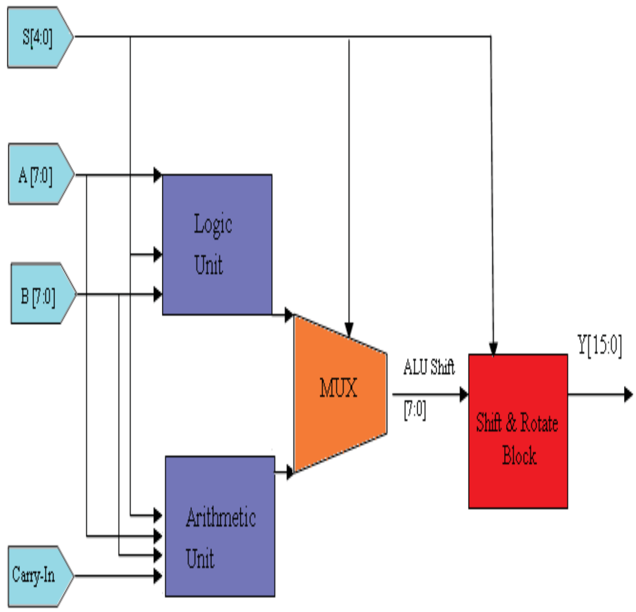

Fig.4 : Block diagram of 8-bit ALU.

b) *Truth Table Design*

Truth table design is an effective method compiling all those functions that are needed by the user on a single platform. Table 1 indicates the combination of five bit control input S[4 down to 0] with their operation and functions that are used in ALU. Arithmetic, Logic and Shifter units are separated in the table.

Table 1 : Combination of five bit control input S [4 down to 0] with their operation and functions that are used in ALU.

S4	S3	S2	S1	S0	Operation	Function	Implementation
0	0	0	0	0	Y<=a+b	Addition	Arithmetic Unit
0	0	0	0	1	Y<=a+ 2's C of b	Subtraction a-b	Arithmetic Unit
0	0	0	1	0	Y<=b+2's C of a	Subtraction b-a	Arithmetic Unit
0	0	0	1	1	Y<=a+1	Increment a	Arithmetic Unit
0	0	1	0	0	Y<=a-1	Decrement a	Arithmetic Unit
0	0	1	0	1	Y<=b+1	Increment b	Arithmetic Unit
0	0	1	1	0	Y<=b-1	Decrement b	Arithmetic Unit
0	0	1	1	1	Y<=a*b	Multiplication	Arithmetic Unit
0	1	0	0	0	Y<=a/b	Division a by b	Arithmetic Unit
0	1	0	0	1	Y<=b/a	Division b by a	Arithmetic Unit
0	1	0	1	0	Y<=a comp	Complement a	Logic Unit
0	1	0	1	1	Y<=b comp	Complement b	Logic Unit
0	1	1	0	0	Y<=a AND b	AND	Logic Unit
0	1	1	0	1	Y<=a OR b	OR	Logic Unit
0	1	1	1	0	Y<=a XOR b	XOR	Logic Unit
0	1	1	1	1	Y<=shl a	Shift left a	Shifter Unit
1	0	0	0	0	Y<=shl b	Shift left b	Shifter Unit
1	0	0	0	1	Y<=shr a	Shift right a	Shifter Unit
1	0	0	1	0	Y<=shr b	Shift right b	Shifter Unit
1	0	0	1	1	Y<=RAL a	Rotate left a	Rotate Unit
1	0	1	0	0	Y<=RAR a	Rotate right a	Rotate Unit

Global Journal of Researches in Engineering (F) Volume XI Issue VII Version I November 2011

V. Implementation

The VHDL coding of this paper design is compiled and simulated using Altera Quartus-II and has been downloaded in FPGA using Xilinx Spartan XC3S100E kit shown in Fig. 5. The data is updated to the kit using two separate select inputs A and B each carrying 8 bits. The function of FPGA is embedded on the kit along with PROM, LCD, LEDs and DIP switches. A Joint Test Action Group (JTAG) interface connects the FPGA chip with PROM and leads to PC through a serial interface. The structure of such a PROM assembly XC10S is shown in Fig. 6. Since FPGA is user programmable, therefore JTAG is of core significance. PROM has several postulates in the shape of data storage and debugging, permanent storage of data, consistency of operation, low cost, high speed and compactness. PROM used in this design of ALU is "XC10S", which is equipped with the inbuilt circuitry to support and store complex functions. It supports both mode of Master and Slave serial Field Programmable Gate Array.

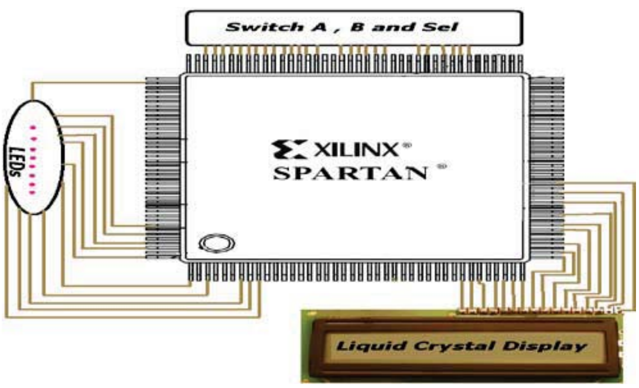

Fig.5 : Circuit design of FPGA kit.

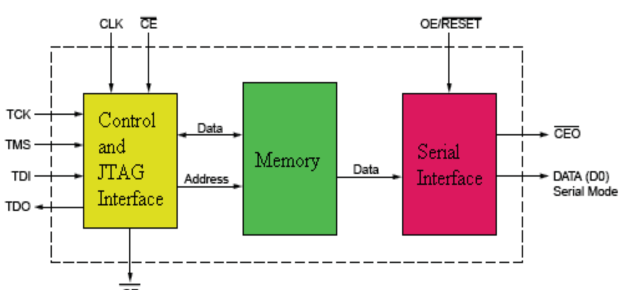

Fig.6 : Structure of XC10S PROM.

In real time application, after the process of compilation and simulation of the VHDL design, the hardware realization is constructed and tested as shown in Fig. 7. Here the 8-bit inputs are given by means of two sets of DIP switches and the 16-bit output can be displayed on a LCD panel and the result can be verified with the simulated output. The status of the flag register is indicated by a series of 8-bit LEDs. The provision of a select switch used in this hardware enables the user to perform the required operation on the FPGA processor.

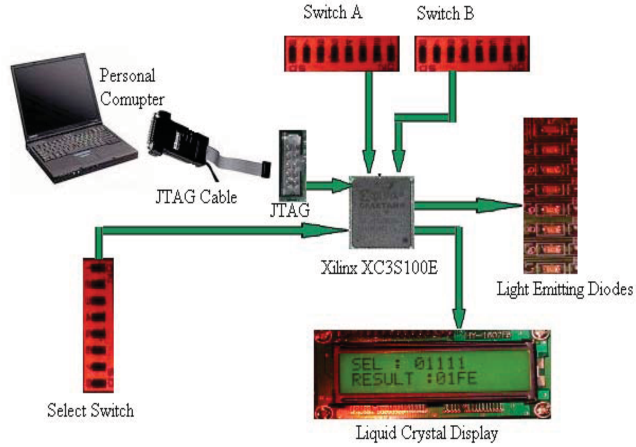

Fig.7 : Real time hardware implementation.

V. Achieved Results

This paper requires the building and simulation of the VHDL coding using Xilinx or Altera program. Once the program has been developed, it will be burnt on to a FPGA chip with which the required hardware is obtained. Designing and Testing of ALU is achieved by differentiating the system into four blocks, first deals with Arithmetic Aspects while second is concerned with Logical Unit, similarly third and fourth blocks are for Shifter and Rotate Operations respectively. Simulated output of a sample multiplication operation is shown in Fig. 8.

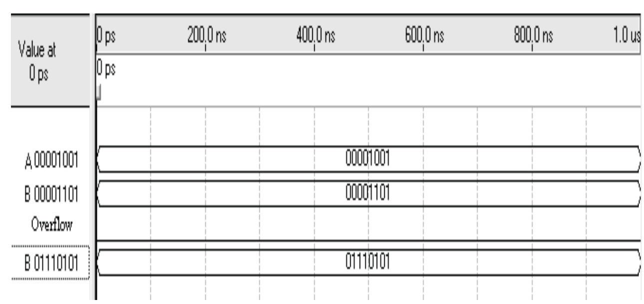

Fig.8 : Simulated output of 8-bit multiplication operation.

VI. Conclusion

In this project, Arithmetic Logic Unit was successfully designed and implemented using Very High Speed Hardware Descriptive Language and Xilinx Spatan-3E Field Programmable Gate Array. All the primary operations of Arithmetic Logic Unit are fabulously done alongside some extra features that provide status of output. Graphical Splitting and Truth Table formation provided a synthesizable system design by separating Arithmetic, Logic, Shifter and Rotator blocks which were integrated in later stages. Design methods involved follows a TOP-DOWN approach in which software design leads the physical and hardware construction. Software section has been realized using Behavioral Model of VHDL. The programming is done for 8 bit lanes of 2 inputs each but system can accommodate up to 6 input channels. The 5 bit control unit holds responsibility for shaping the output of specified operation. Further enhancements can be made on this system by adding more number of inputs with increased number of bit size. Digital Signal Processing (DSP) is being credited with lots of applications from VHDL designs. Advancement in floating point applications of ALU can mutually benefit the two fields.

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· Present your points in sound order

· Use present tense to report well accepted

· Use past tense to describe specific results

· Shun familiar wording, don't address the reviewer directly, and don't use slang, slang language, or superlatives

· Shun use of extra pictures - include only those figures essential to presenting results

Title Page:

Choose a revealing title. It should be short. It should not have non-standard acronyms or abbreviations. It should not exceed two printed lines. It should include the name(s) and address (es) of all authors.

Abstract:

The summary should be two hundred words or less. It should briefly and clearly explain the key findings reported in the manuscript--must have precise statistics. It should not have abnormal acronyms or abbreviations. It should be logical in itself. Shun citing references at this point.

An abstract is a brief distinct paragraph summary of finished work or work in development. In a minute or less a reviewer can be taught the foundation behind the study, common approach to the problem, relevant results, and significant conclusions or new questions.

Write your summary when your paper is completed because how can you write the summary of anything which is not yet written? Wealth of terminology is very essential in abstract. Yet, use comprehensive sentences and do not let go readability for briefness. You can maintain it succinct by phrasing sentences so that they provide more than lone rationale. The author can at this moment go straight to shortening the outcome. Sum up the study, with the subsequent elements in any summary. Try to maintain the initial two items to no more than one ruling each.

- Reason of the study - theory, overall issue, purpose
- Fundamental goal
- To the point depiction of the research
- Consequences, including definite statistics - if the consequences are quantitative in nature, account quantitative data; results of any numerical analysis should be reported
- Significant conclusions or questions that track from the research(es)

Approach:

- Single section, and succinct
- As a outline of job done, it is always written in past tense
- A conceptual should situate on its own, and not submit to any other part of the paper such as a form or table
- Center on shortening results - bound background information to a verdict or two, if completely necessary
- What you account in an conceptual must be regular with what you reported in the manuscript
- Exact spelling, clearness of sentences and phrases, and appropriate reporting of quantities (proper units, important statistics) are just as significant in an abstract as they are anywhere else

Introduction:

The **Introduction** should "introduce" the manuscript. The reviewer should be presented with sufficient background information to be capable to comprehend and calculate the purpose of your study without having to submit to other works. The basis for the study should be offered. Give most important references but shun difficult to make a comprehensive appraisal of the topic. In the introduction, describe the problem visibly. If the problem is not acknowledged in a logical, reasonable way, the reviewer will have no attention in your result. Speak in common terms about techniques used to explain the problem, if needed, but do not present any particulars about the protocols here. Following approach can create a valuable beginning:

- Explain the value (significance) of the study
- Shield the model - why did you employ this particular system or method? What is its compensation? You strength remark on its appropriateness from a abstract point of vision as well as point out sensible reasons for using it.
- Present a justification. Status your particular theory (es) or aim(s), and describe the logic that led you to choose them.
- Very for a short time explain the tentative propose and how it skilled the declared objectives.

Approach:

- Use past tense except for when referring to recognized facts. After all, the manuscript will be submitted after the entire job is done.
- Sort out your thoughts; manufacture one key point with every section. If you make the four points listed above, you will need a least of four paragraphs.
- Present surroundings information only as desirable in order hold up a situation. The reviewer does not desire to read the whole thing you know about a topic.
- Shape the theory/purpose specifically - do not take a broad view.
- As always, give awareness to spelling, simplicity and correctness of sentences and phrases.

Procedures (Methods and Materials):

This part is supposed to be the easiest to carve if you have good skills. A sound written Procedures segment allows a capable scientist to replacement your results. Present precise information about your supplies. The suppliers and clarity of reagents can be helpful bits of information. Present methods in sequential order but linked methodologies can be grouped as a segment. Be concise when relating the protocols. Attempt for the least amount of information that would permit another capable scientist to spare your outcome but be cautious that vital information is integrated. The use of subheadings is suggested and ought to be synchronized with the results section. When a technique is used that has been well described in another object, mention the specific item describing a way but draw the basic principle while stating the situation. The purpose is to text all particular resources and broad procedures, so that another person may use some or all of the methods in one more study or referee the scientific value of your work. It is not to be a step by step report of the whole thing you did, nor is a methods section a set of orders.

Materials:

- Explain materials individually only if the study is so complex that it saves liberty this way.
- Embrace particular materials, and any tools or provisions that are not frequently found in laboratories.
- Do not take in frequently found.
- If use of a definite type of tools.
- Materials may be reported in a part section or else they may be recognized along with your measures.

Methods:

- Report the method (not particulars of each process that engaged the same methodology)
- Describe the method entirely
- To be succinct, present methods under headings dedicated to specific dealings or groups of measures
- Simplify - details how procedures were completed not how they were exclusively performed on a particular day.
- If well known procedures were used, account the procedure by name, possibly with reference, and that's all.

Approach:

- It is embarrassed or not possible to use vigorous voice when documenting methods with no using first person, which would focus the reviewer's interest on the researcher rather than the job. As a result when script up the methods most authors use third person passive voice.
- Use standard style in this and in every other part of the paper - avoid familiar lists, and use full sentences.

What to keep away from

- Resources and methods are not a set of information.
- Skip all descriptive information and surroundings - save it for the argument.
- Leave out information that is immaterial to a third party.

Results:

The principle of a results segment is to present and demonstrate your conclusion. Create this part a entirely objective details of the outcome, and save all understanding for the discussion.

The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

Content

- Sum up your conclusion in text and demonstrate them, if suitable, with figures and tables.
- In manuscript, explain each of your consequences, point the reader to remarks that are most appropriate.
- Present a background, such as by describing the question that was addressed by creation an exacting study.
- Explain results of control experiments and comprise remarks that are not accessible in a prescribed figure or table, if appropriate.
- Examine your data, then prepare the analyzed (transformed) data in the form of a figure (graph), table, or in manuscript form.

What to stay away from

- Do not discuss or infer your outcome, report surroundings information, or try to explain anything.
- Not at all, take in raw data or intermediate calculations in a research manuscript.

- Do not present the similar data more than once.
- Manuscript should complement any figures or tables, not duplicate the identical information.
- Never confuse figures with tables - there is a difference.

Approach

- As forever, use past tense when you submit to your results, and put the whole thing in a reasonable order.
- Put figures and tables, appropriately numbered, in order at the end of the report
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Figures and tables

- If you put figures and tables at the end of the details, make certain that they are visibly distinguished from any attach appendix materials, such as raw facts
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- Make a decision if each premise is supported, discarded, or if you cannot make a conclusion with assurance. Do not just dismiss a study or part of a study as "uncertain."
- Research papers are not acknowledged if the work is imperfect. Draw what conclusions you can based upon the results that you have, and take care of the study as a finished work
- You may propose future guidelines, such as how the experiment might be personalized to accomplish a new idea.
- Give details all of your remarks as much as possible, focus on mechanisms.
- Make a decision if the tentative design sufficiently addressed the theory, and whether or not it was correctly restricted.
- Try to present substitute explanations if sensible alternatives be present.
- One research will not counter an overall question, so maintain the large picture in mind, where do you go next? The best studies unlock new avenues of study. What questions remain?
- Recommendations for detailed papers will offer supplementary suggestions.

Approach:

- When you refer to information, differentiate data generated by your own studies from available information
- Submit to work done by specific persons (including you) in past tense.
- Submit to generally acknowledged facts and main beliefs in present tense.

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Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
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Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

INDEX

O

P

Q

R

S

T

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