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Abstract - Proto-type Silicon Drift Detectors (SDDs) have been realized through a pilot stage fabrication run at the Micro-fabrication facility at Indian Institute of Technology - Bombay (IIT-B). Taking precedence from the fabrication run at IIT-B, commercial grade SDDs with on-chip low noise JFETs are being developed for low energy X-ray spectroscopy and position sensing applications using silicon bipolar technology available with Bharat Electronics Ltd (BEL), Bangalore. This paper presents a detailed illustrative view on the design; fabrication and characterization of the SDDs & in-built JFETs fabricated at BEL. Traditionally, detectors are fabricated over high resistivity silicon substrates whereas JFETs are fabricated over low-resistivity silicon. To design a process for fabrication of both SDD and JFET over high resistivity silicon posed a sufficient technological challenge. Simulations in Technology Computer Aided Design (TCAD) proved helpful in arriving at optimum process parameter values for fabrication of SDDs and on-chip JFETs over the same high resistivity silicon substrate. SDDs & low noise JFETs fabricated at BEL were characterized to extract dc (I-V) performance parameters like total leakage current at anode, transconductance etc. These results formed precursors to fine-tuning the process for the next run aimed at achieving an even lower leakage current level.

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I. Introduction

Silicon drift detector (SDD) is a device based on the principle of lateral charge transport within the bulk of a fully depleted detector, as proposed by Gatti and Rehak (Reference-1). SDD is essentially detector in which a high resistivity *n*-type silicon substrate is employed to fabricate *p-n* junctions on both sides of the substrate. PN junctions on the front side form segmented field shaping cathodes whereas a uniform, *p-n* junction forms the back-cathode. A reverse bias gradient when applied to the field shaping cathodes together with a constant back-contact voltage creates a potential distribution in the shape of a "Potential Gutter" with the ultimate electron potential energy minimum at the anode. Electron-hole pairs created by passage of ionizing radiation are swept vertically by the parabolic potential along the depth and focused at the local potential minima from where they get drifted along the lateral drift channel towards the anode. The distinguishing feature of the SDD is that its small output (anode) capacitance is independent of its large detector active area.

Thus SDDs are suitable for high resolution (127eV @ 5.9 keV for Mn-Kα line; Ketek Vitus SDD) and high count rate (~$1x10^6$ cps) X-ray spectroscopy applications. These detectors have found wide application in high-energy physics for tracking applications. SDDs have been incorporated in the ALICE detector along the Large Hadron Collider at CERN.

This high-resolution capability of SDDs can be further augmented by integrating the input device of the pre-amplifier (JFET) with the detector so as to avoid stray capacitance and microphonism arising due to wire bonding between them. The integration of JFET onto the detector also facilitates better matching between detector and transistor capacitances.

The proto-typing stage fabrication of SDDs at IIT-B has been successfully completed. The first run of the fabrication of the commercial grade SDDs and JFETs has yielded satisfactorily good results.

SDDs fabricated at BEL were aimed at both X-ray Spectroscopy and position sensing applications. Circular geometry SDDs with in-built low noise JFETs were designed for X-ray Spectroscopy applications. Linear geometry SDDs with on-chip poly-silicon resistors were designed for 1D & 2D position sensing applications. Additionally, high transconductance JFETs were also designed together with various different kinds of SDDs over the 4-inch silicon wafer.

II. Detector Design

This particular version of SDD has an on-chip Poly-Resistor network for biasing the intermediate p+ strips together with an on-chip JFET for first level

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amplification [Fig. 1(b)]. The anode is in geometry of an annular ring having 50 μm radii with an area of 7.7 x 10^4 μm^2 that fetched an analytical full depletion capacitance of 27 fF for 300 μm thick fully depleted silicon wafer. The total active area of the detector was 2.31 x 10^7 μm^2. This device had 20 p+ strips with two guard rings encircling its outer perimeter. The first, fifth, tenth, fifteenth, twentieth, and last p+ strips were individually biased whereas the of rest p+ strips got biased by the on-chip resistor. Each poly resistor was designed to present a resistance of 102.4 kΩ (R_S=138.88 kΩ/□). The embedded lownoise JFET (named as JFET-10) for this SDD design had the smallest channel length (15 μm) possible with BEL process [Fig. 1(b)]. For a designed channel length of 15 μm and the channel width of 172 μm, the analytical Transconductance (g_m) works out to be **0.247 mS.**

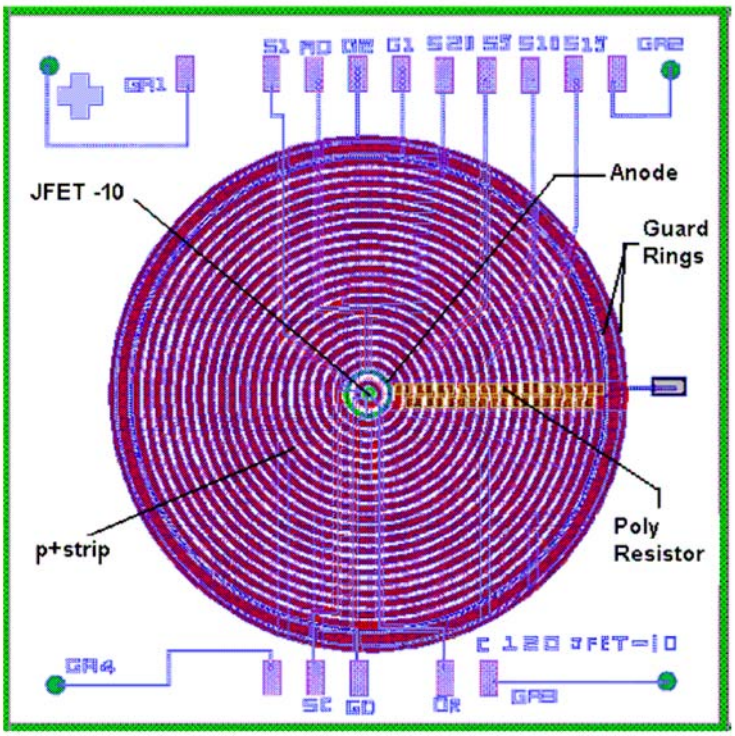

Fig. 1 (a) : Composite layout of Circular SDD (Pitch-120µm) with in-built JFET.

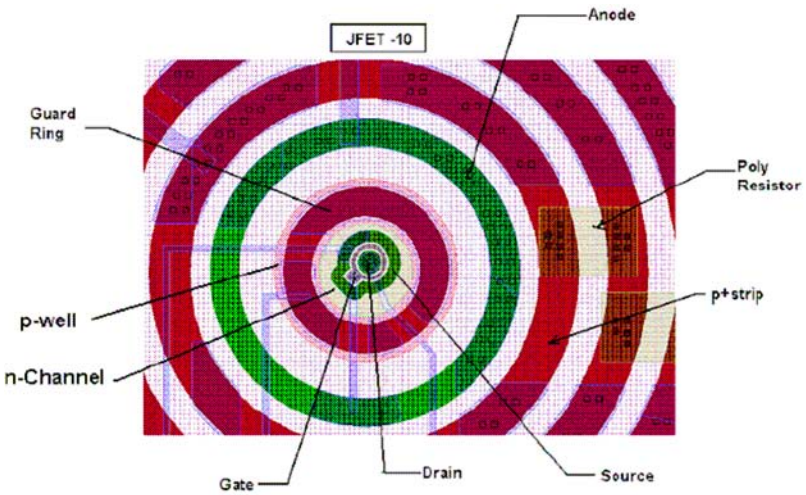

Fig. 1 (b) : Zoomed view of the embedded JFET (JFET-10) showing all mask layers.

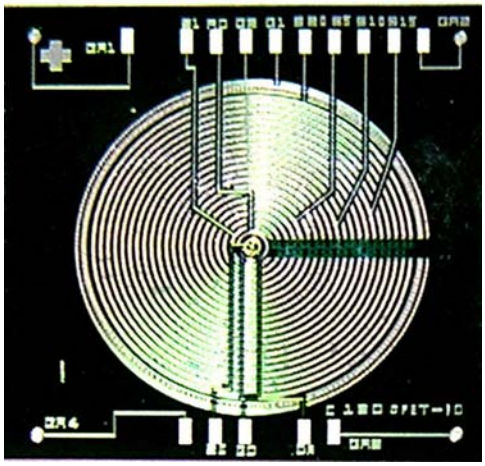

Fig. 1 (c) : Photograph of the completely fabricated SDD with in-built JFET.

III. Fabrication Of Sdds & Low-Noise Jfets

a) Fabrication Objectives

On the basis of the success of the fabrication effort at IIT-B, the process for the BEL effort was formulated. Formulation of a process for fabrication of SDD and JFET over high resistivity silicon substrate was a significant technological challenge. The process for the fabrication of SDD with integrated JFET was formulated with a view of achieving a high breakdown voltage of >100V, and achieving as low leakage current as possible using the existing fabrication setup at BEL. The process employed at BEL involved all the standard unit processes like oxidation, lithography, etching, and implantation, metallization etc. employed in a bipolar fabrication line. The process parameters have been fine tuned and frozen after a thorough TCAD process simulation study in order to achieve the desired doping profiles for both SDD & JFET. The highest standards of cleanliness and care in planning the unit processes have been maintained to achieve the objectives of low leakage currents together with admissibly high breakdown voltages. Moreover, the process had to be compliant with the technological constraints of the BEL foundry. Additionally, Polysilicon process has been employed for fabrication of on-chip resistor network. The distinguishing feature of this process was the employment of a double-sided processing for back to front alignment of cathode implants. Thus making double sided SDDs a reality, which are far more superior to single sided SDDs. The lithographic quality was again a challenge as the fabrication process involved 14 lithographic steps.

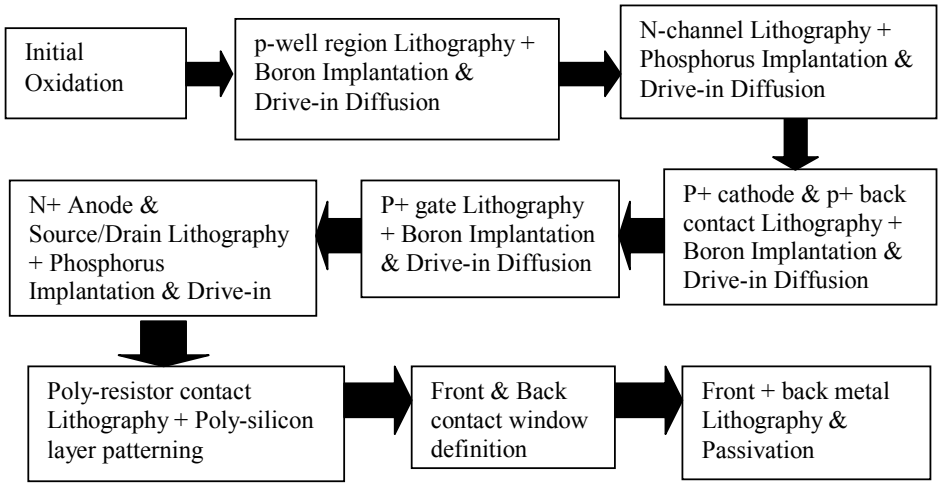

Fig. 2 : Block Diagrammatic illustration of the process flow.

b) Fabrication Process and TCAD Simulations

Starting with a 4-inch n-type, high resistivity (3-5 kΩ.cm) compensated silicon wafer of <111> orientation, an initial oxide was grown employing the Dry-Wet-Dry regime (Thickness = 0.6μm). The bulk comprising of the wet oxide (t = 0.4μm) was sandwiched between two high quality dry oxide layers (t = 0.1 μm) each. The next step was the lithographic

definition of the p-type isolation well (**Mask-1**) within the center of the SDD for housing the embedded JFET. This was followed by an oxide etch step to expose the substrate for boron implantation (E = **80 keV**; Dose = **$5x10^{11}$ cm^{-2}**). Subsequent dopant activation and drive-in diffusion of boron species was performed employing the Drive-in cycle as illustrated in the Fig. 4. The simulated doping profile for the p-well implant showed a peak boron concentration of $3.39x10^{14}$ cm^{-3} for a junction depth of **3.19 μm** and an extracted sheet resistance of **102.705 kΩ/□**. Subsequently, the n-channel within the p-well region was lithographically defined **(Mask-2)** and phosphorus implantation (E = **150 keV**; Dose = **$5x10^{12}$ cm^{-2}**) was performed followed by a drive-in cycle (Fig. 6) to form the n-channel. The simulated doping profile (Fig. 7) for the n-channel showed a peak phosphorus concentration of **$3.24x10^{16}$ cm^{-3}** for a junction depth of **2 μm** and an extracted sheet resistance of **2.703 kΩ/□**. Going ahead from here, the p+ cathodes & p+ guard ring (**Mask-3**) were lithographically defined on the top-surface whereas the p+ backcontact (**Mask-4**) was defined on the bottom surface of the wafer employing back to front double-sided alignment lithography. A thin screen-oxide (Fig. 8) was grown over the exposed silicon to create shallow junctions and prevent implantation damage. Boron Implantation (Dose = **$1x10^{15}$ cm^{-2}**; Energy = **80 keV**) followed by dopant activation and drive-in (Fig. 9) was performed to create p+ strips, p+ guard ring and p+ back-contact regions. The simulated doping profile showed a peak boron concentration of **$2.24x10^{18}$ cm^{-3}** for a junction depth of **1.5 μm** and extracted sheet resistance of **181.93 Ω/□**. The 5th lithographic (**Mask-5**) step was performed for definition of p+ type Gate region of the JFET. Boron Implantation (Dose = **$1x10^{15}$ cm^{-2}**; E = **80keV**), followed by Drive-in (Fig. 12) was performed to realize the p+ gate region. In the p+ Gate Drive-in case, the analytical value of sheet resistance was **181.93 Ω/□**, for a junction depth of **1.1 micron** and the extracted peak Boron concentration of **$1x10^{19}$ cm^{-3}**. Subsequently, n+ Anode, Source & Drain were defined (**Mask-6**) followed by Phosphorus Implantation (Dose = **$1x10^{15}$ cm^{-2}**; E = **80 keV**) forms the n+ regions. The dopant activation and drive-in was performed as per schedule in figure 14. The simulated analytical sheet resistance was **79.3 Ω/□**, for a characteristic depth of **1 micron** and the extracted peak Phosphorus concentration was **$1.1x10^{20}$ cm^{-3}**. Following this, oxide openings (Poly-contact: **Mask-7**) were defined over the p+ strips region to facilitate the poly-silicon layer deposited in the next step to make contact with under-lying p+ region. Poly-Silicon was then deposited and boron implantation was performed to form the poly-resistors having a Sheet Resistance of **138.88 kΩ/□**. After lithographically patterning (**Mask-8**) the polysilicon layer a short anneal step (Time = **30 minutes**; Temperature = **900ºC**) was carried out to dopant activation of the species in the poly layer. Proceeding from that, the contact lithography (**Mask-9**) was performed to open windows through the oxide for making contact with Aluminum metal deposited above for purpose of electrical connection with rest of the electronics. The back-contact was defined (**Mask-10**) for contact window openings on the back surface of the wafer. Aluminum metallization (Thickness = 1.5 microns) was carried out over the front-surface and lithography was performed (**Mask-11**) to pattern the metal layer to define the various electrical connections. The back-side was then metalized keeping the front-surface protected and the metal layer was patterned lithographically (**Mask-12**) to form the backelectrodes of the SDD. Lastly, Protective glass was deposited over both the front and back-sides followed by lithography (**Masks-13 & 14**) to open areas over the metal bond pads. The values for sheet resistances, junction depths for various regions have been tabulated in **Table-1**.

Table 1 : Analytical Values of sheet resistance and junction depth for various Process stages.

Sr. No.	Process stage	Junction Depth (μm)	Sheet Resistance (Ω/□)
1	p-well	3.19	102.7 k
2	n-channel	2	2.7 k
3	p-cathode	1.5	181
4	p+ gate	1.1	181.93
5	n+ Source/Drain & Anode	1.0	79

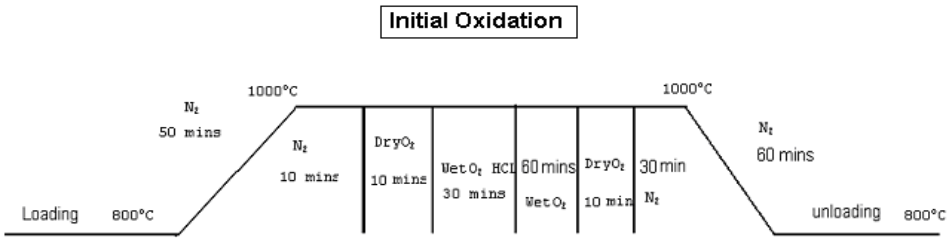

Fig. 3 : Schematic of the Initial Oxidation cycle

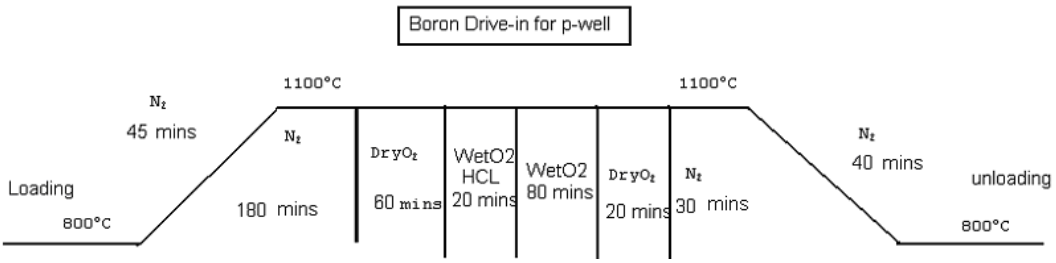

Fig. 4 : Schematic of the Boron Drive-in cycle for p-well.

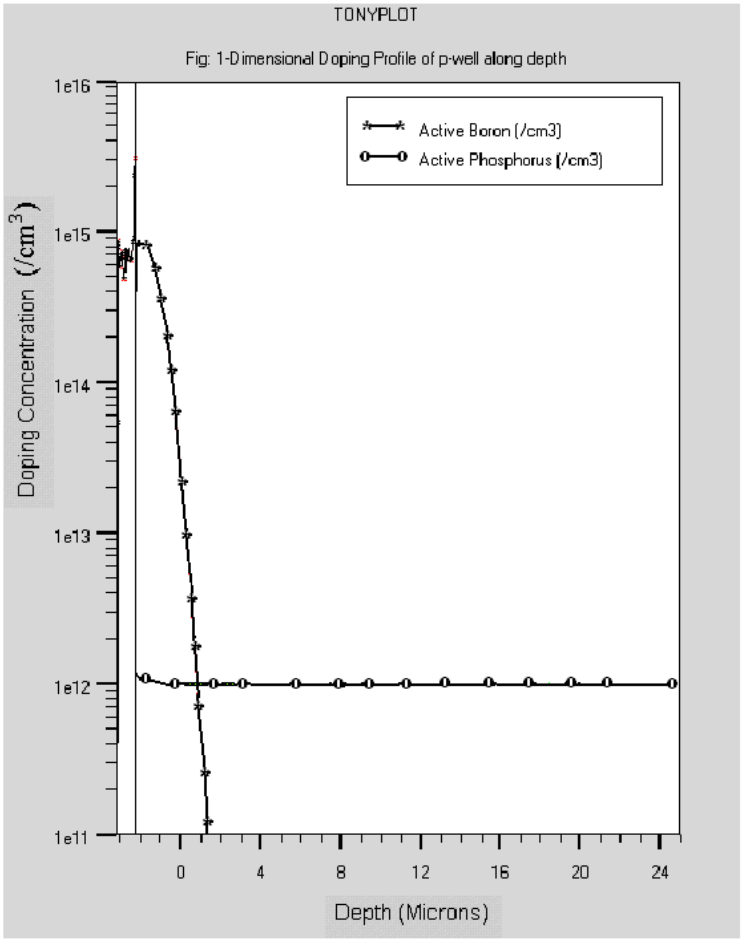

Fig. 5 : One-Dimensional doping profile of p-well region along depth.

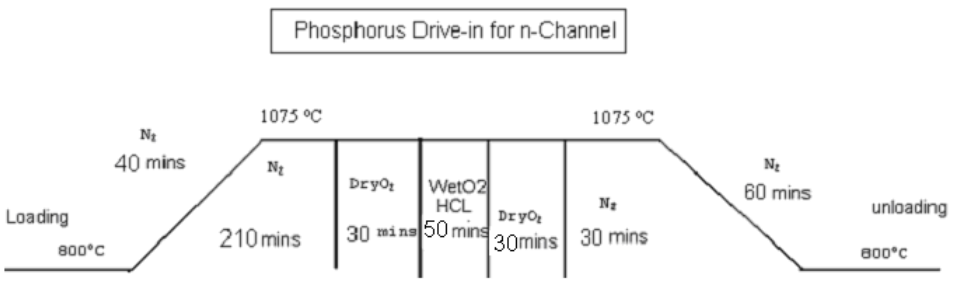

Fig. 6 : Schematic of the Phosphorus Drive-in cycle for n-Channel.

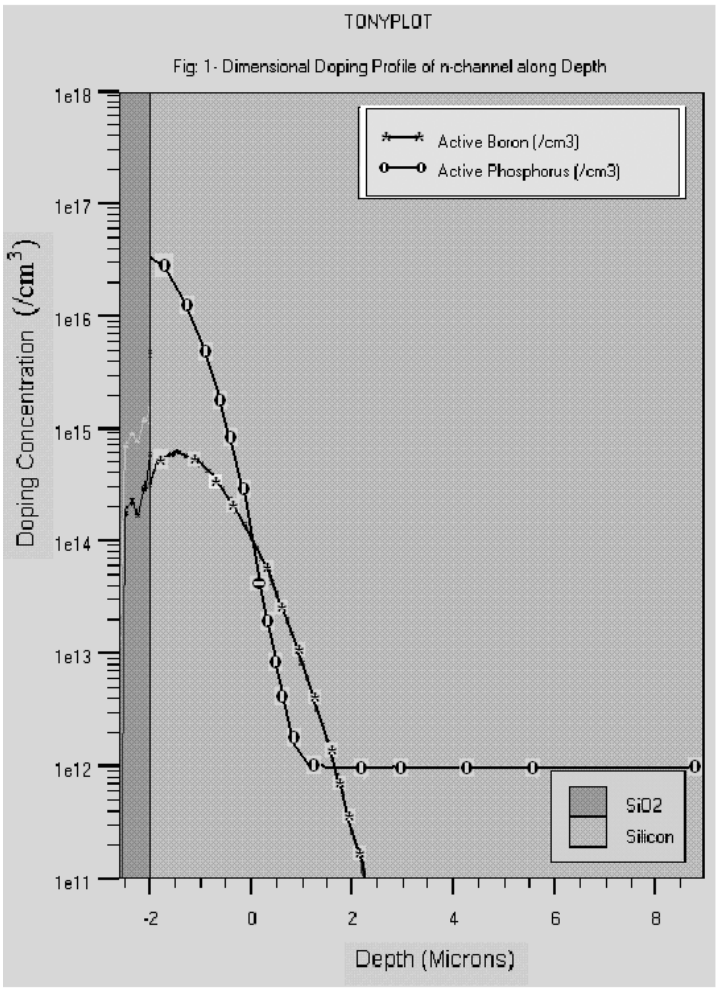

Fig. 7 : One-Dimensional doping profile of n-Channel region along depth.

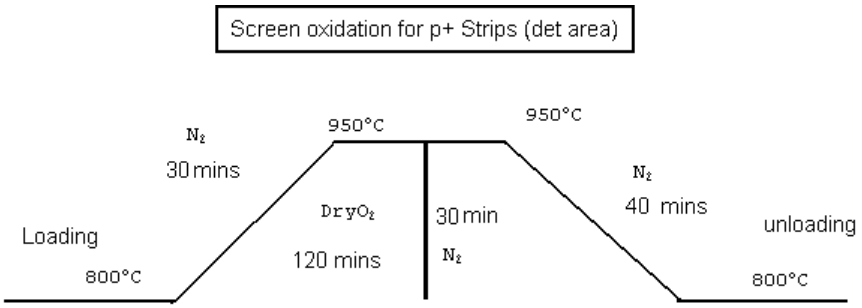

Fig. 8 : Schematic of the Screen Oxidation cycle for p+ Strips.

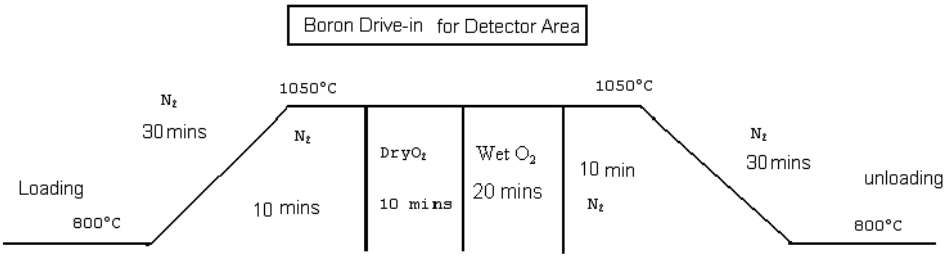

Fig. 9 : Schematic of the Boron Drive-in cycle for p+ Strips and p+ back contact.

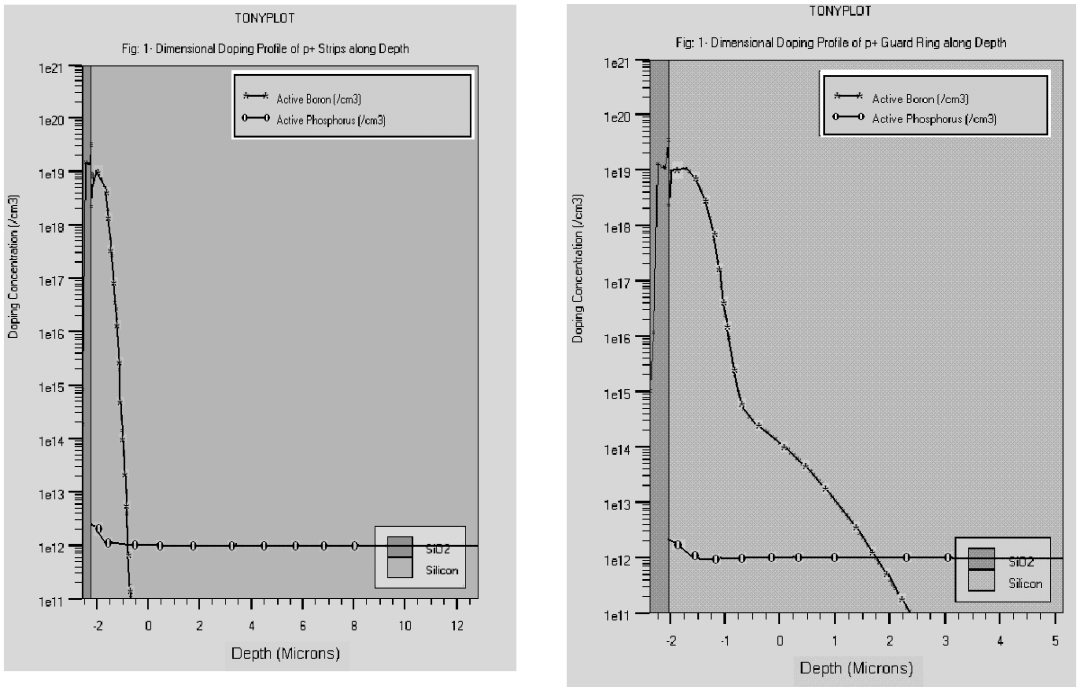

Fig. 10 : One-Dimensional Doping Profile of Annealed Boron Implant for p+ Strips & p+ Guard Ring.

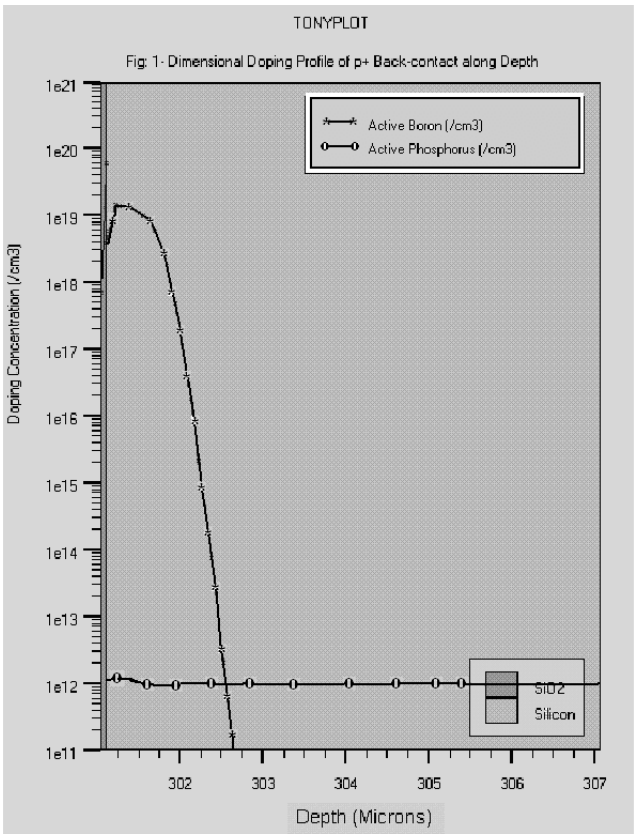

Fig. 11 : One-Dimensional Doping Profile of Annealed Boron Implant for p+ Backcontact.

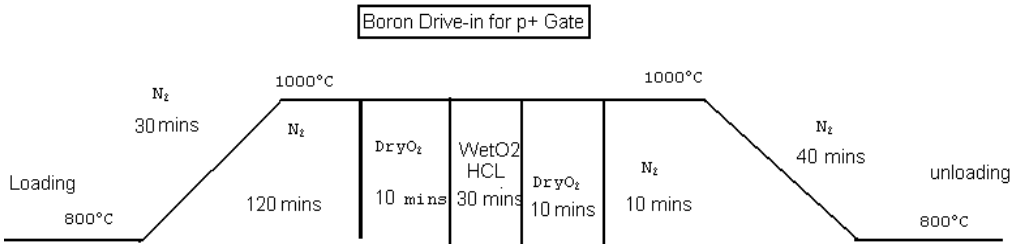

Fig. 12 : Schematic of the Boron Drive-in cycle for p+ Gate.

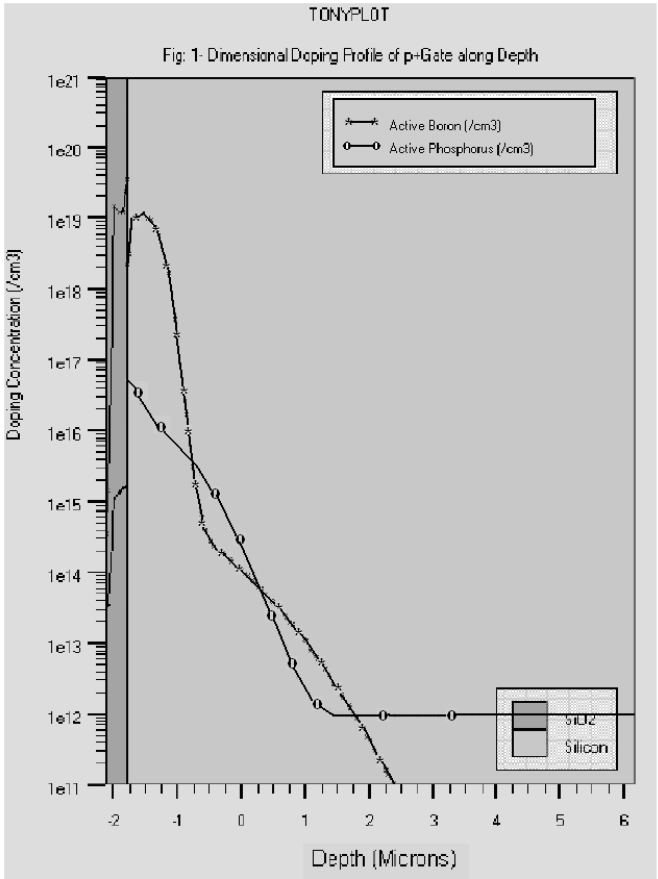

Fig. 13 : One-Dimensional doping profile of Gate region along the depth.

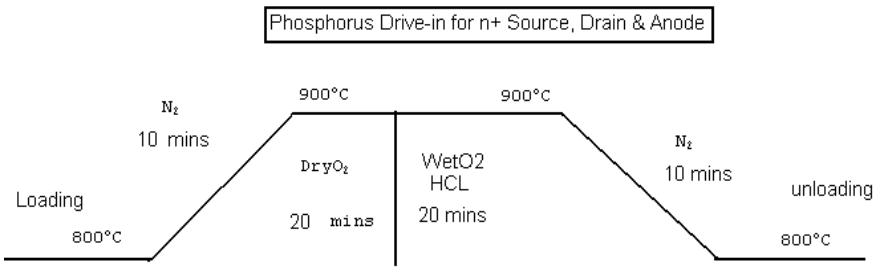

Fig. 14 : Schematic of the Phosphorus Drive-in cycle for n+ Source, Drain & Anode.

IV. I-V Characterization

a) Objectives & Measurement Methodology

I-V characterization of the completely biased SDD was performed to get the total biasing current across all the *p* strips and the total leakage current at the anode for a detector bias of -100V. A single Keithley-2400 source-measure unit was used to supply voltages to all the nodes through an external resistor network consisting of 20 resistors of 100 kΩ each, giving a minimum voltage of 5V at each node. Wafer level characterization was performed for each design of SDD.

The anode was given a zero potential (ultimate potential energy minima for electrons) and the first p+ cathode (Cathode - 1) was given a bias of –5 V. The last p cathode (Cathode-6) was biased at -100V and the back-cathode potential was fixed at -50V. The p cathodes intermediate between the first and last cathodes got biased automatically through onchip poly resistors. The p-well guard ring was kept floating in this case. A C++ program was coded for interfacing and automation of the Keithley meters for the measurement process. I-V was taken by ramping the voltage at the last strip (Cathode-6) from -100 V to 0 V and the anode current was measured through an ammeter (Keithley-2400 SMU used in current sense mode). I-V characteristics were measured for various values of guard-ring voltages (illustrated in Fig. 15). The nature of the I-V curve matched with the nature of I-V curve achieved for the SDDs in IIT case. The embedded low-noise JFET was characterized for its dc performance using the same experimental setup.

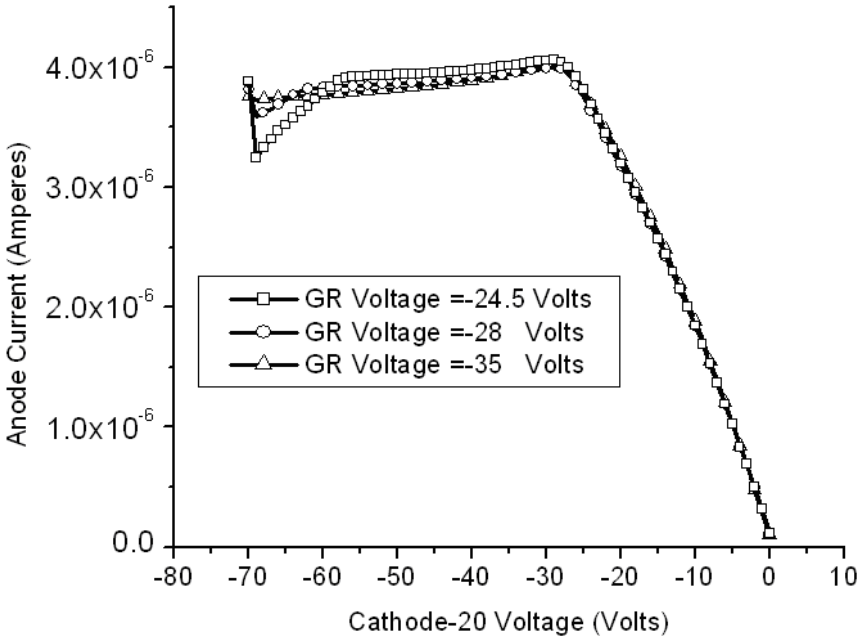

Fig. 15 : I-V Characteristics of Circular SDD (Pitch =120μm).

b) Results & Discussions

The anode current (Fig. 15) rises till above full depletion voltage (~ -25V) and then saturates to a value of ~ 3.7 μA till a cathode voltage of -70 Volts. The embedded low-noise JFET was also characterized for extracting the drain and transfer characteristics (Figs. 16 & 17). The experimentally achieved Transconductance (g_m) was 0.34 mS for a Pinchoff voltage of -7 Volts. The experimentally derived transconductance value was within 30% of the analytical value derived from simulation. The channel resistance value derived from the I-V plot was 20 kΩ and the calculated thermal noise $[(8kT / 3g_m)^{1/2}]$ worked out to be 5.69 nV√Hz. The value of noise figure achieved was good enough to qualify the JFET in the low-noise category.

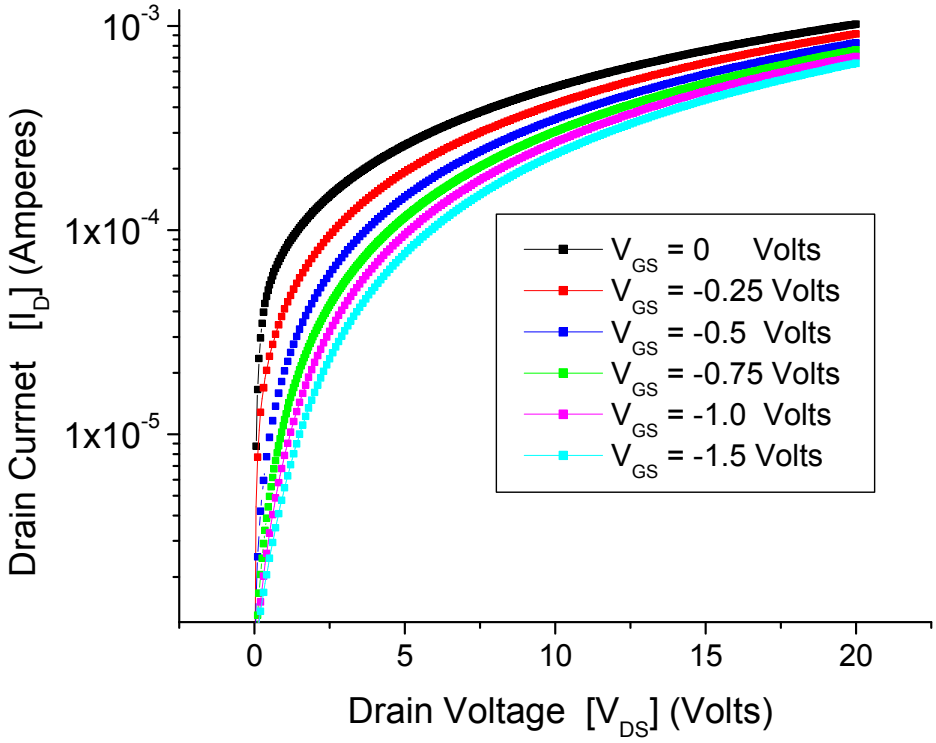

Fig. 16 : Drain Characteristics of embedded JFET.

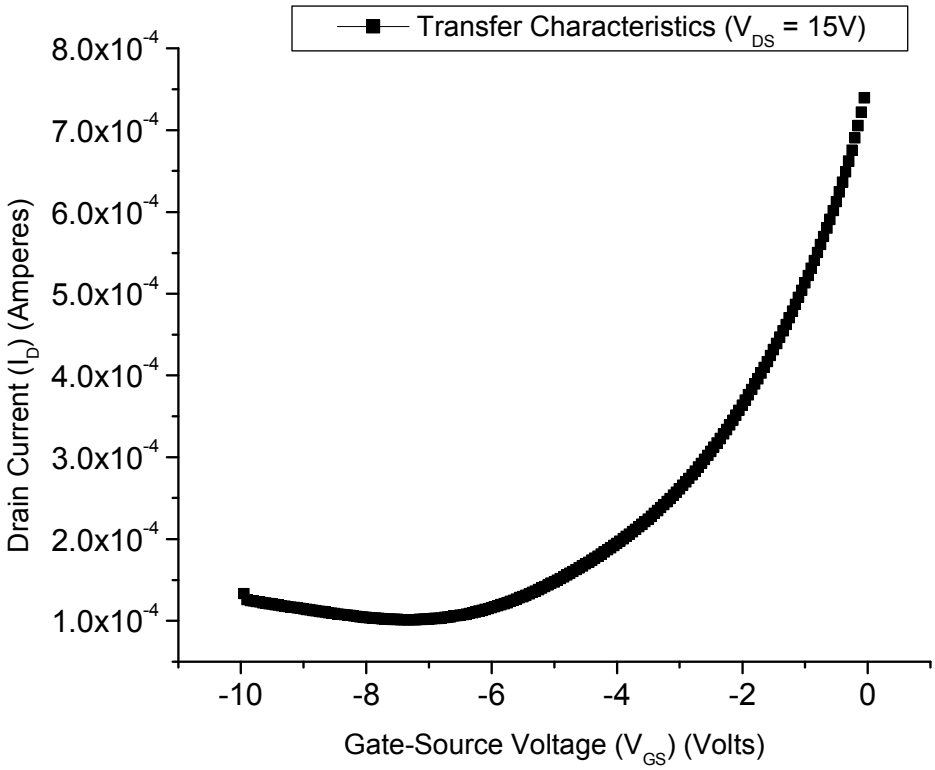

Fig. 17 : Transfer Characteristics of embedded JFET.

V. Conclusions

First prototypes of SDDs with embedded low noise JFETs have been successfully fabricated at BEL, Banglaore. Process technology for fabrication of SDDs and lownoise JFETs has been developed employing simulation studies in TCAD. Dc characterization of SDDs and embedded low-noise JFETs have been successfully carried out. The experimentally achieved values for anode current were higher than expected. Analytical value of transconductance was found to have a

deviation of less than 30% from that achieved from characterization. The value of noise figure (5.69 $nV\sqrt{Hz}$) was within the low noise band.

Acknowledgements

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