

Implementation of Closed Loop System for Diode Clamped Multilevel Inverter with Stand-Alone Photovoltaic Input

ramani kannan¹ and Mr. Venus.V²

¹ K.S.Rangasamy College of Technology, Tiruchengode, Tamilnadu, India

Received: 11 December 2012 Accepted: 3 January 2013 Published: 15 January 2013

Abstract

Multilevel inverter is as one of the most recent and popular type of advances in power electronics. It synthesizes desired output voltage waveform from several dc sources used as input for the multilevel inverter. This paper describes a diode-clamped five-level inverter-based battery/super capacitor direct integration scheme for photovoltaic energy systems. The study is carried out for three cases. In the first case, one of the two dc-link capacitors of the inverter is replaced by a battery bank and the other by a super capacitor bank. In the second case, dc-link capacitors are replaced by two battery banks. In the third case, ordinary dc-link capacitors are replaced by two super capacitor banks. The first system is supposed to mitigate both long-term and short-term power fluctuations while the last two systems are intended for smoothening long-term and short-term power fluctuations, respectively. These topologies eliminate the need for interfacing dc-dc converters and thus considerably improve the overall system efficiency. The major issue in aforementioned systems is the unavoidable imbalance in dc-link voltages. An analysis on the effects of unbalance and a space vector modulation method, which can produce undistorted current even in the presence of such unbalances, are presented in this paper. Simulation work is done using the MATLAB software which validates the proposed method and finally THD comparison is presented for analysis

Index terms— diode-clamped five-level inverter, direct integration of battery energy storage systems, space vector modulation, unbalanced operation of diode-clampe

1 Implementation of Closed Loop System for Diode Clamped Multilevel Inverter with Stand-Alone Photovoltaic Input

Venus.V & K.Ramani A Abstract -Multilevel inverter is as one of the most recent and popular type of advances in power electronics. It synthesizes desired output voltage waveform from several dc sources used as input for the multilevel inverter. This paper describes a diode-clamped five-level inverter-based battery/super capacitor direct integration scheme for photovoltaic energy systems. The study is carried out for three cases. In the first case, one of the two dc-link capacitors of the inverter is replaced by a battery bank and the other by a super capacitor bank. In the second case, dc-link capacitors are replaced by two battery banks. In the third case, ordinary dc-link capacitors are replaced by two super capacitor banks. The first system is supposed to mitigate both long-term and short-term power fluctuations while the last two systems are intended for smoothening long-term and short-term power fluctuations, respectively. These topologies eliminate the need for interfacing dc-dc converters and thus considerably improve the overall system efficiency. The major issue in aforementioned systems is the unavoidable imbalance in dclink voltages. An analysis on the effects of unbalance and a space vector modulation method, which can produce undistorted current even in the presence of such unbalances, are presented in this paper. Simulation work is done using the MATLAB software which validates the proposed ethod and finally THD comparison is presented for analysis.

2 Introduction

ultilevel converters are mainly utilized to synthesis a desired single or three-phase voltage waveform. The desired multi staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra capacitors are the most common independent sources used. The intermittent nature of renewable energy sources can create serious system stability issues, especially at increased levels of penetration [1], [2]. Renewable energy resources will be an Increasingly important part of power generation in the new millennium. Besides assisting in the reduction of the emission of greenhouse gases, they add the muchneeded flexibility to the energy resource mix by decreasing the dependence on fossil fuels. Recently, batteries and super capacitors have emerged as leading energy storage devices [3]- [6]. Furthermore, the combination of battery and super capacitor provides an excellent match that can cover a wide range of power and energy requirements [5], [15]. The simplest way of adding a battery (or a super capacitor) bank is the direct connection to the dc link of the grid side inverter, as shown in Fig. 1(a). But it suffers from several drawbacks such as large internal resistance, fixed current distribution governed by internal resistors, and lack of control over the power flow [8]. Effects of these issues can somewhat be reduced if an intermediate dc-dc converter is placed between the ve Therefore, the possible alternative ways of connection to avoid additional dc-dc converter while maintaining the control flexibility. The result is the simple configuration shown in Fig. 1(c). In the figure, the dc-link capacitors of a standard diode-clamped five-level inverter are replaced by a battery bank and a super capacitor bank. Latter part of this paper discusses two more cases: one with two super capacitor banks and the other with two battery banks. If a change in the source or the load happens, the power imbalance will be compensated by the battery bank and/or super capacitor bank. $V_{i1} V_{n1} V_{dc} V_{ce}$

The main issue with this particular topology is the imminent imbalance of the neutral point potential which is due to unequal states of charge of the battery bank and the super capacitor bank. Comprehensive analysis on capacitor voltage unbalance and balancing techniques used in diode-clamped inverters can be found in the literature [1], [8]. A new Space Vector Modulation (SVM) method has been developed for diode-clamped five-level inverters with variable dc-link voltages. Furthermore, full controllability over small vector selection is available in the proposed SVM method. Relevant equations and diagrams are given in Section III with a detailed analysis. The proposed SVM technique involves more computations compared to simplified SVM techniques proposed in the literature. The THD values for the Traditional, Conventional and proposed inverters are compared and analysed.

3 II. Unbalanced Dc-Link Voltages Effects

For the diode-clamped Five-level inverter, shown in Fig. 1(c), line-to-ground voltages can be derived from switching states S_a , S_b , and S_c , and the results are given in Table ?? . If the inverter is connected to a balanced three-phase load, corresponding phase voltages can be derived from line-to-ground voltages using (1). Then, these phase voltages are transformed into the dq reference frame by (2). The locations of small and medium vectors vary with dc-link voltages as shown in Fig. 2. However, locations of large vectors (2 0 0, 2 2 0, 0 2 0, 0 2 2, 0 0 2, and 2 0 2) depend only on the total dc-link voltage and would remain unchanged if the total voltage is constant. When capacitor voltages are balanced, positive and negative small vectors (2 1 1, 2 2 1, 1 2 1, 1 2 2, 1 1 2, 2 1 2, 1 0 0, 1 1 0, 0 1 0, 0 1 1, 0 0 1, and 1 0 1) coincide and only one inner hexagon is formed as shown in Fig. 2(b). Furthermore, medium vectors (2 1 0, 1 2 0, 0 2 1, 0 1 2, 1 0 2, and 2 0 1) reach midpoints of the outer hexagon. If an unbalance is present, small vectors split and two separate inner hexagons appear as shown in Fig. 2(a) and (c). In addition to that, medium vectors move toward large vectors. The size of the inner hexagon formed with negative small vectors depends on the battery voltage, which is nearly constant in the proposed system. Similarly, the size of the inner hexagon formed with positive small vectors varies with the super capacitor voltage. The circles marked with dotted lines in Fig. 2 represent the path of the reference voltage vector. In the proposed method, the super capacitor voltage is allowed to vary in a way that this circle will always remain within the outer hexagon and middle inner hexagon. If the normal SPWM with two equal carriers, as shown in Fig. 3 Therefore, a novel space vector modulation method has been developed, from the scratch, to reduce voltage stresses and to produce desired fundamental components even at large imbalanced conditions. The result of the proposed SVM technique is shown in Fig. 3(h). Its fundamental component is very similar to that of the waveforms shown in Fig. 3(g), and hence, it is not shown here exclusively. A detailed description of the proposed SVM technique is given in Section III. of the reference voltage vector are generated by the grid side inverter controller. Currently, serving sector of the space vector diagram is derived from the phase angle. However, due to the presence of two candidate triangles, four different limit angles, 1, 2, 3, and 4, need to be calculated for a given sector. First two limit angles (1 and 2) are related to the triangles formed with lower small vectors as shown in Fig. ??(a) whereas the other two limit angles ?? 3 and 4) are associated with the triangles formed with positive small vectors as shown in Fig. ??(b). For the simplicity of subsequent calculations, dc-link voltages are transformed into two variables x and y using (5).

4 III. Implementation of Svm Technique

These two values are directly related to the lengths of triangles as marked in Fig. ?? . Limit angles are calculated using (??)-(10), where is an intermediate variable. The limit angles given in (??)-(??0) are valid only for sector

1. Once the limit angles are calculated, the triangle and corresponding three vectors can easily be derived. After finding the three vectors, the next step is to determine switching times. According to the wellknown volt-second balancing principle, a given reference vector can be synthesized by three adjacent vectors. Equations (??1) and (??2) provide the mathematical description of this process. Equations (??3)-(??6) are used to calculate corresponding switching times d_1 d_3 that are expressed as fractions of the sampling time.

IV.

5 Simulation and Results

The five level diode clamped multilevel inverter simulation results and analysis describe in this section. The simulation diagram for space vector Modulation is shown in Figure ??With the use of this proposed method harmonics are eliminated. Therefore the efficiency of the inverter is increased. Some soft switching method can be used for multilevel inverter to reduce the switching loss and to increase the efficiency. The figure 14 Total Harmonics Distortion for open loop system. The Total harmonic distortion of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. THD is used to characterize the linearity of audio systems and the power quality of electric power systems. From the table 3 different inverter THD values are compared. The proposed inverter THD value is obtained as 10.16%, which is the best among all. This shows that quality of the five level inverter is improved.

V.

6 Conclusion

This paper is the first step to develop a complete solar photovoltaic power electronic conversion system in simulation. The Proposed topologies eliminate the need for additional dc-dc converters by connecting two battery banks, two super capacitor banks or a battery bank, and a super capacitor bank directly across dc links of a diode clamped five-level inverter. Unavoidable dc-link voltage imbalance is the major issue with these topologies. This problem is handled by a novel space vector modulation technique. Further work is needed to improve the efficiency by reducing THD and the hardware will be designed for different power levels. The THD values for the Traditional, Conventional and proposed inverters are compared and analysed.



Figure 1: Fig. 1 (

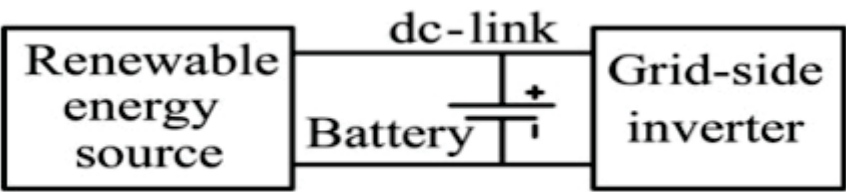


Figure 2:

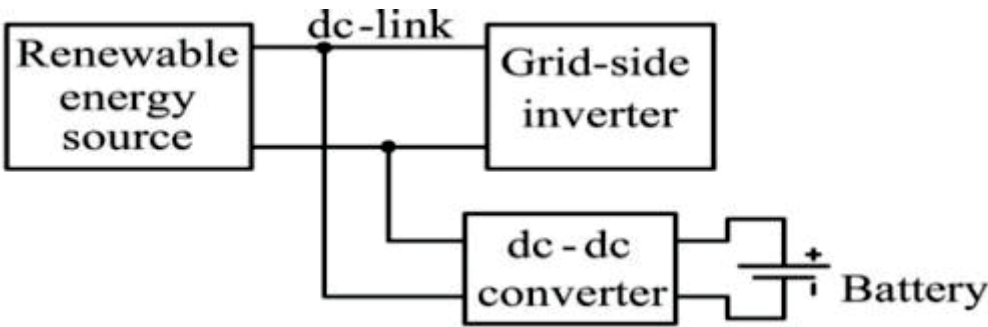


Figure 3: Table 1 :

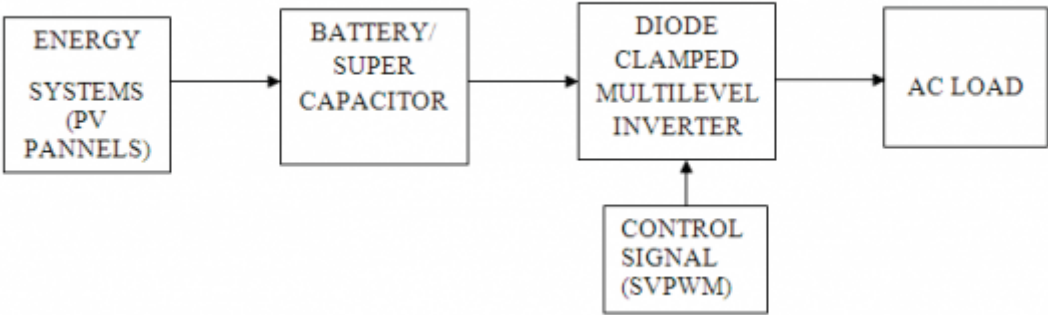


Figure 4: Fig. 2 (

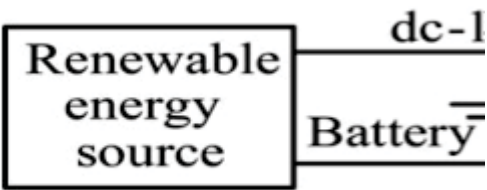


Figure 5: Fig. 3 :

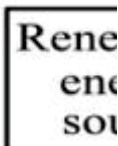


Figure 6: Fig. 4 (Fig. 4 (

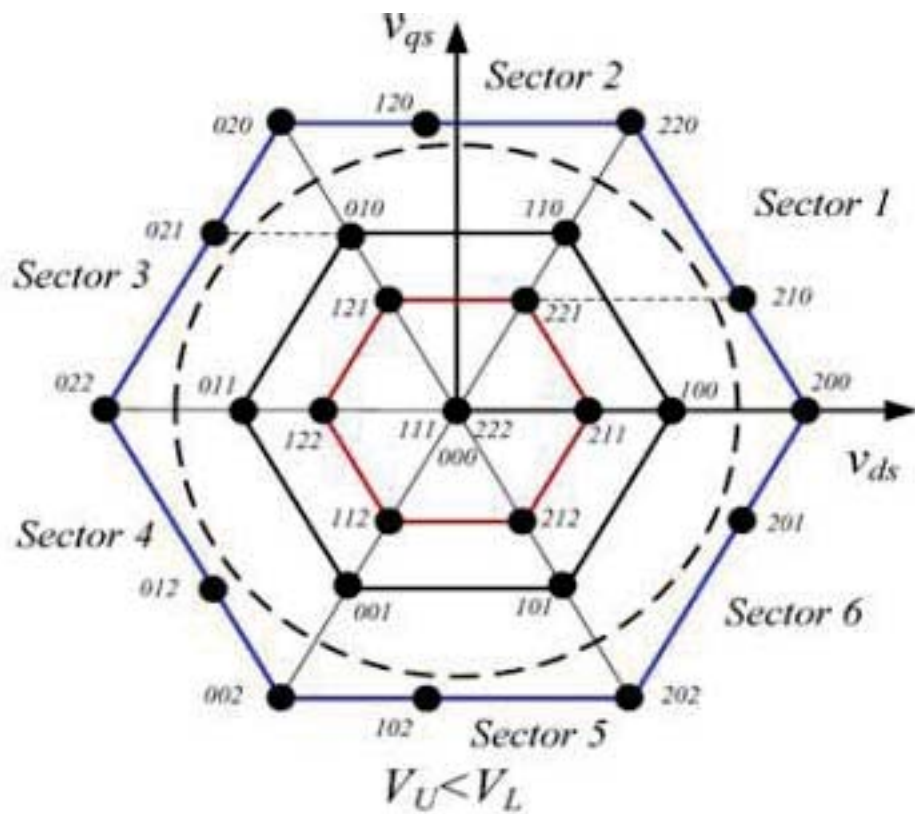
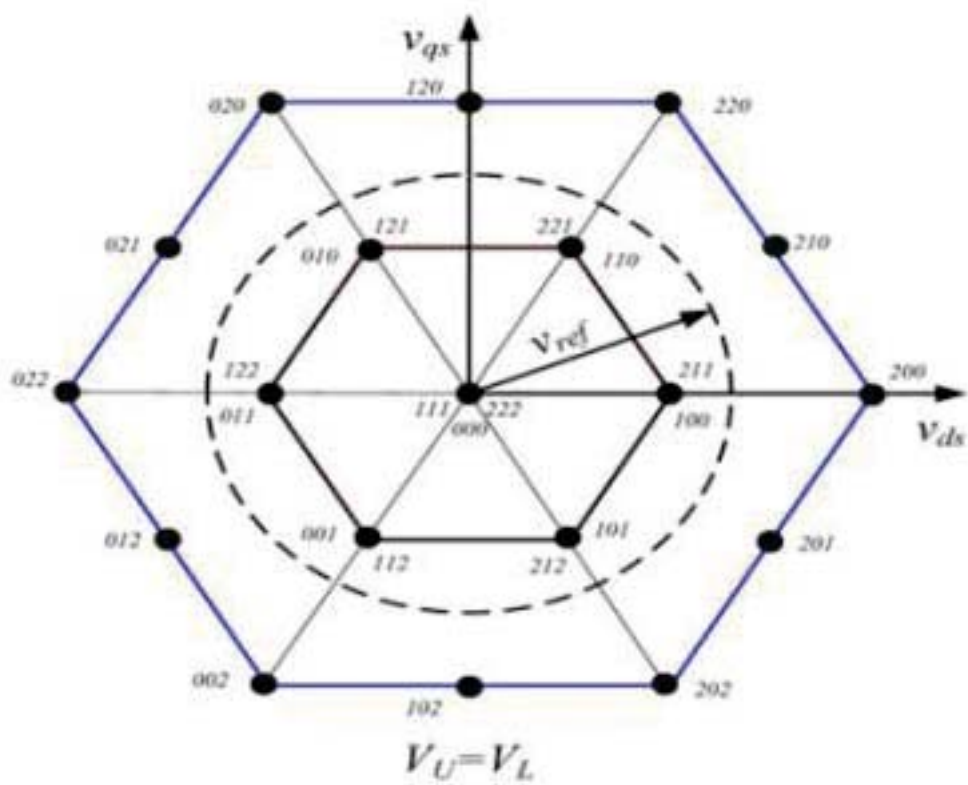


Figure 7:



5637

Figure 8: Fig 5 :Fig 6 : 3 .Fig. 7 :

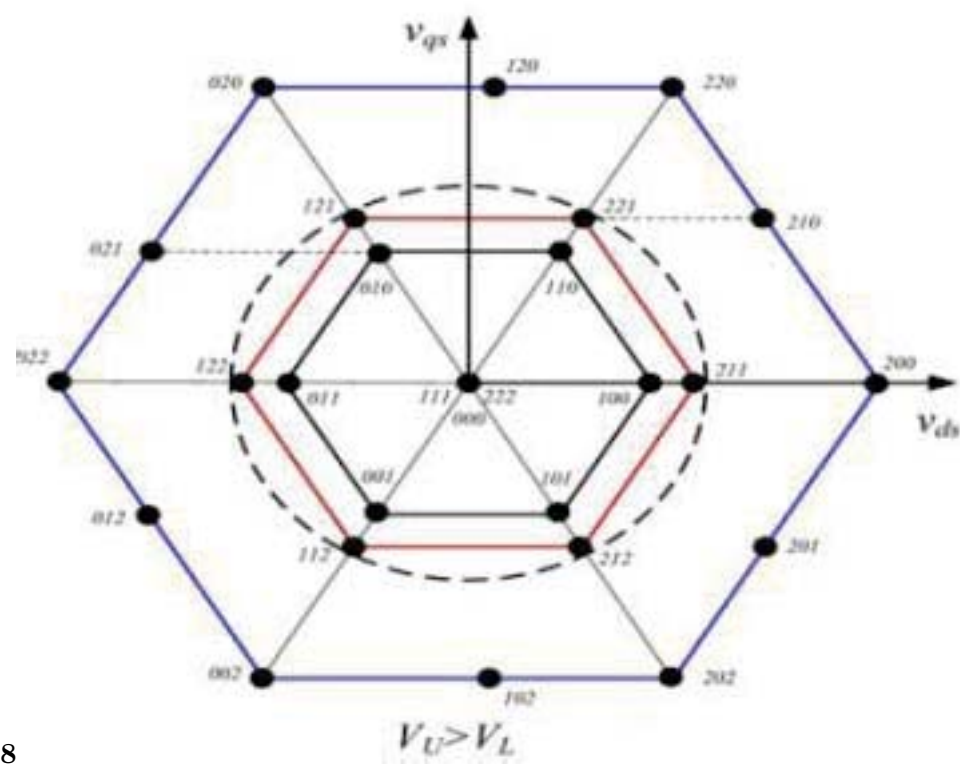


Figure 9: Fig. 8 :

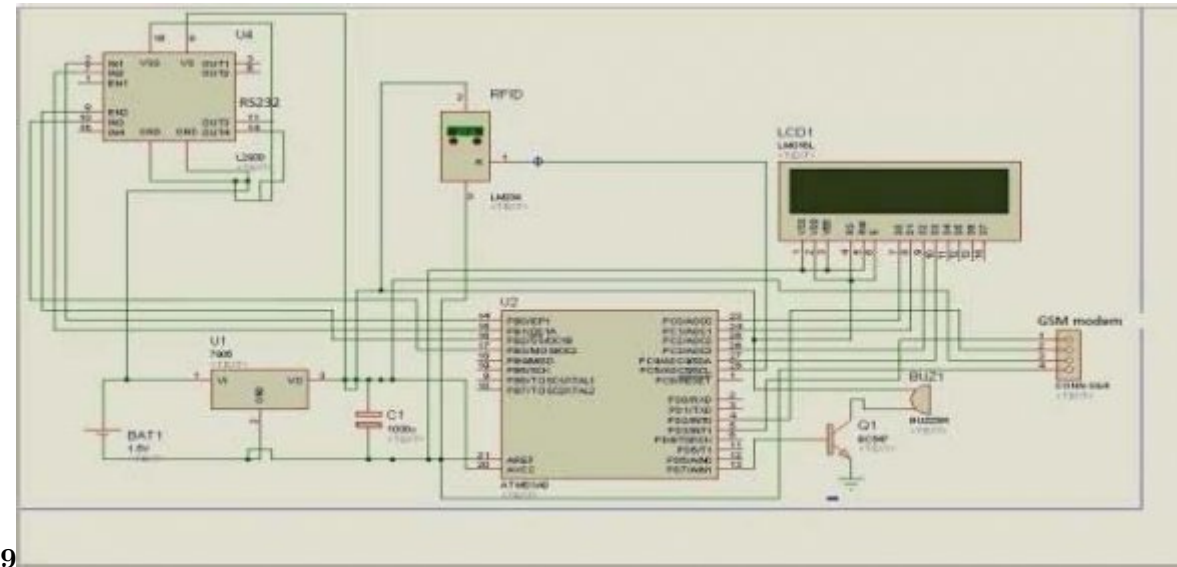
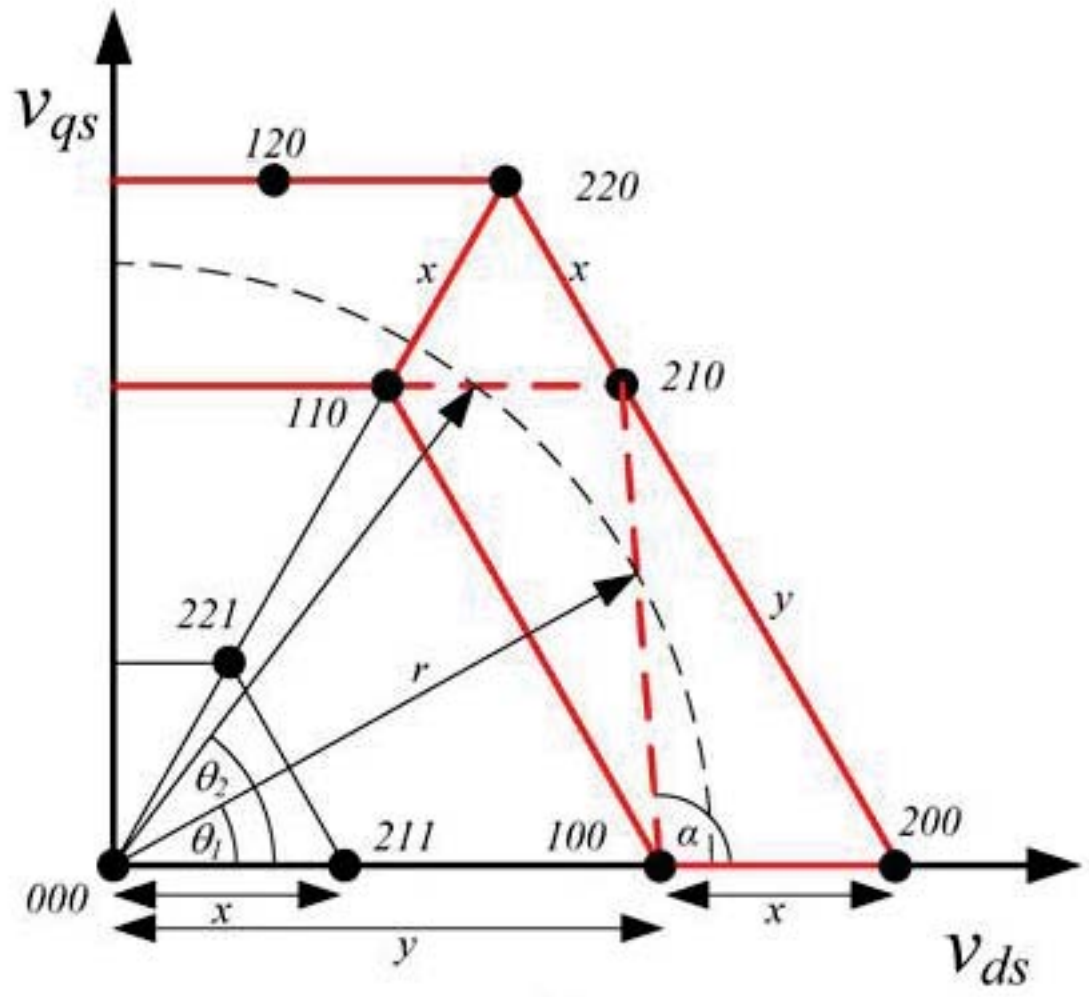
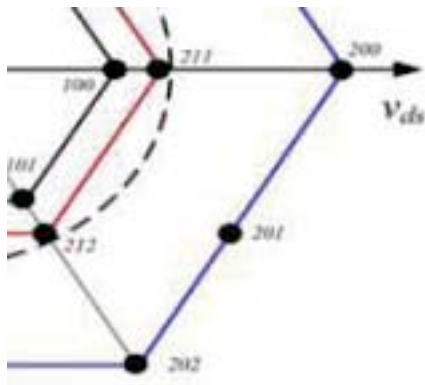


Figure 10: Fig. 9 :



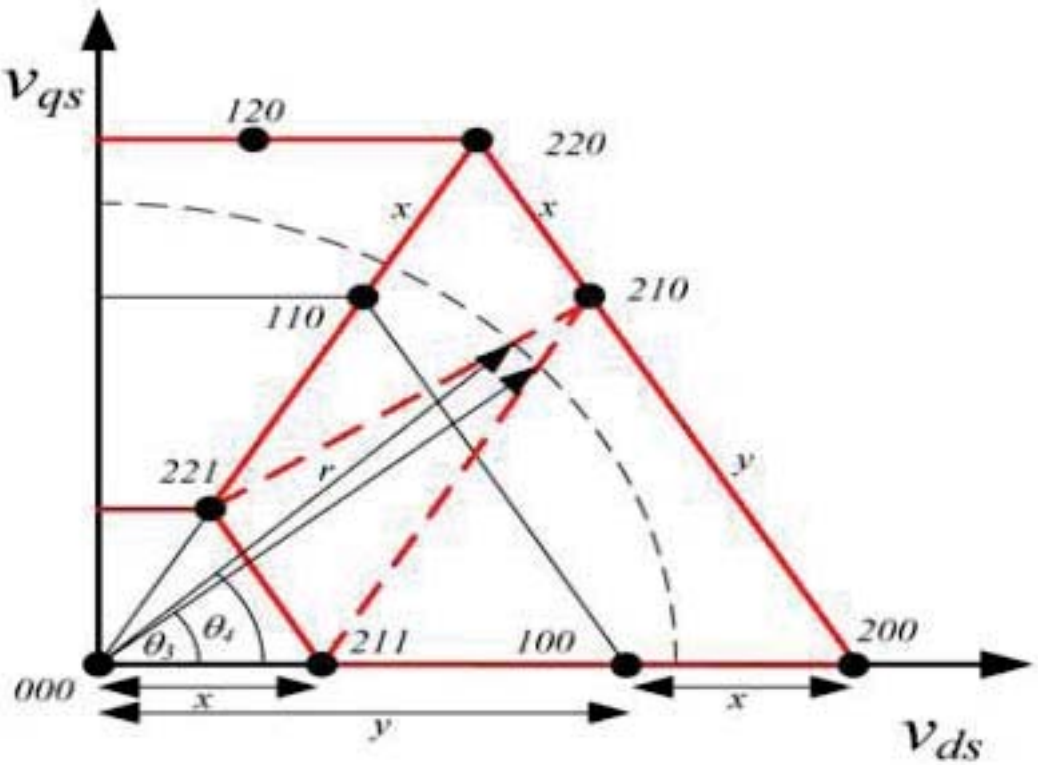
1112

Figure 11: Fig. 11 :FigFig. 12 :



14

Figure 12: Fig. 14 :



15

Figure 13: Fig. 15 :

2

Kind of the MLI	2 Level MLI	3 Level MLI	5 Level Propose d MLI
THD		53.84%	10.16%

Figure 14: Table 2 :

¹F © 2013 Global Journals Inc. (US)

²F © 2013 Global Journals Inc. (US)

³F © 2013 Global Journals Inc. (US)

⁴F © 2013 Global Journals Inc. (US)

-
- [Ewanchuk and Salmon ()] ‘A Five-/Nine-Level Twelve-Switch Neutral-Point-Clamped Inverter for High-Speed Electric Drives’. Jeffrey Ewanchuk , John Salmon . *IEEE Transactions on Industry Applications* 2011. 47 (5) p. .
- [Alirezanami ()] ‘A Hybrid Cascade Converter Topology with Series-Connected Symmetrical and Asymmetrical Diode-Clamped H Bridge Cells’. Alirezanami , Firuzzare . *IEEE Transactions on Power Electronics* 2011. 26 (1) p. .
- [Akagi and Hasegawa ()] ‘A New DC-voltage-Balancing Circuit Including a Single Coupled Inductor for a Five-Level Diode-Clamped PWM Inverter’. Hirofumi Akagi , Kazunori Hasegawa . *IEEE Transactions on Industry Applications* 2011. 47 (2) p. .
- [Hasegawa and Akagi ()] ‘A New DC-voltage-Balancing Circuit Including and Single Coupled Inductor for a Five-Level Diode Clamped PWM Inverter’. Kazunori Hasegawa , Hirofumi Akagi . *IEEE Transactions on Industry Applications* 2011. 47 (2) p. .
- [Behzadvafakhah and Ewanchuk ()] Jeffrey Behzadvafakhah , Ewanchuk . *Multicarrier Interleaved PWM Strategies for a Five-Level NPC Inverter Using a Three-Phase Coupled Inductor*, 2011. 47 p. .
- [Krstic ()] ‘Comparative Evaluation of Modulation Algorithms for Neutral-Point-Clamped Converters’. Ashishbendre , Slobodan Krstic . *IEEE Transactions on Industry Applications* 2005. 41 (2) p. .
- [Berkouk and Saudemont (2007)] ‘DC Link Capacitor Voltage Balancing in a Three-Phase Diode Clamped Inverter Controlled by a Direct Space Vector of Line-to-Line Voltages’. C Berkouk , Saudemont . *IEEE Transactions on Power Electronics* September [2007. 22 p. .
- [Gaminijayasinghe and Mahindavilathgamuwa ()] ‘Diode-Clamped Three-Level Inverter-Based Battery/Super capacitor Direct Integration Scheme for Renewable Energy Systems’. D Gaminijayasinghe , Mahindavilathgamuwa . *IEEE Transactions on Power Electronics* 2011. 26 (12) p. .
- [Takagi and Iwafune ()] ‘Economic Value of PV Energy Storage Using Batteries of Battery-Switch Stations’. Masaaki Takagi , Yumiko Iwafune . *IEEE Transactions on Sustainable Energy* 2012. p. .
- [Shukla and Ghosh ()] ‘Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel Inverter’. Anshuman Shukla , Arindam Ghosh . *IEEE Transactions on Industrial Electronics* 2010. 57 (7) p. .
- [Enginozdemir and Suleozdemir ()] ‘Fundamental-Frequency-Modulated Six-Level Diode-Clamped Multilevel Inverter for Three-Phase Stand-Alone Photovoltaic System’. Enginozdemir , Suleozdemir . *IEEE Transactions on Industrial Electronics* 2009. 56 (11) p. .
- [Hasegawa and Akagi ()] ‘Low Modulation -Index Operation of a Five Level Diode Clamped PWM Inverter with DC-voltage-Balancing circuit for a motor drive’. Kazunori Hasegawa , Hirofumi Akagi . *IEEE Transactions on Power Electronics* 2012. 27 (8) p. .
- [Leon and Vazquez ()] ‘Three-Dimensional Feed Forward Space Vector Modulation Applied to Multilevel Diode-Clamped Converters’. Jose I Leon , Sergio Vazquez . *IEEE Transactions on Industrial Electronics* 2009. 56 (1) p. .
- [Xiao ()] ‘Transformer Less Split-Inductor Neutral Point Clamped Three-Level PV Grid-Connected Inverter’. Huafeng Xiao , Shaojunxie . *IEEE Transactions on Power Electronics* 2012. 27 (4) p. .
- [Arash and Boora ()] ‘Voltage-Sharing Converter to Supply Single-Phase Asymmetrical Four-Level Diode-Clamped Inverter with High Power Factor Loads’. A Arash , Alirezanami Boora . *IEEE Transactions on Power Electronics* 2010. 25 (10) p. .