Design and Implementation of Low Power 12-Bit 100-MS/s Pipelined ADC Using Open-Loop Residue Amplification

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Abstract

In this paper a high speed, low power 12-bit, analog-to-digital converter in CMOS 0.13 micron technology that makes it suitable for UWB is designed and implemented. For designing the particular ADC a bottom up hierarchical method is adopted. First according to the specification, the design of aspect ratio of the transistors used in our design is done. There were many challenges throughout the design process, including determining the matching requirements of the devices, investigating what percentage of segmentation to be used to design the whole system. For checking the functionality of the whole system a spice code is written using HSPICE by defining all blocks in the circuit as sub circuits. Then a schematic capture is done using schematic composer from virtuoso stating from bottom level to top level. Finally the layout for the complete ADC is done using Electric Layout editor. A 12-bit pipelined ADC that can operate at maximum frequency of 100 MSPS, and power consumption less than 70mW is designed and implemented.

Index terms— Multi-stage, high Speed, high Accuracy, Low power, low voltage, ADC, CMOS.

1 Introduction

any and the communication systems today digital signal processing (DSP) to resolve the transmitted information. Therefore between the received analog signal and DSP system an analog-todigital interface is necessary. This interface achieves the digitization of received waveform subject to a sampling rate requirement of the system. Being a part of communication system, the low power constraint mentioned above the A/D interface also needs to address to the low power constraint. There are many ADC architectures; pipelined ADCs are advantageous and widely used in applications with signal bandwidths that are too high for oversampling delta-sigma ADCs and resolution requirements that are too high for flash ADCs. Nevertheless they are sensitive to distortion introduced by the residue amplifiers in their first few stages, and residue amplifier distortion tends to be inversely related to both power supply voltage and power consumption. Therefore, the residue amplifiers are usually the dominant consumers of power in highresolution pipelined ADCs, particularly in low supply voltage designs [1]- [6]. Among the key building blocks in pipelined ADCs are the residue amplifiers that interface successive converter stages. Especially in the converter front-end, these gain elements have to meet very stringent speed, noise, and linearity requirements and tend to dominate overall power dissipation. To address this issue, a variety of techniques have been developed to minimize amplifier power in pipelined ADCs. Among them, stage scaling [3], [4], optimization of the per-stage resolution ??5]- [7], and amplifier sharing techniques [8], [9] are commonly used. In addition to their dominance in power consumption, it has also been recognized that residue amplifiers are most susceptible to complications that arise from continuing integrated circuit technology scaling [10], [11]. For implementations in future deep submicron processes, it is often predicted that limited supply headroom and low intrinsic device gain may lead to a relative power increase in such noise-limited precision analog circuit blocks [12], [13]. In this paper, a pipelined ADC is designed that achieves superior SNR, and operates at 100Msps, with power dissipation less than 70mW. Section II discusses pipelined ADC architecture, section III discusses design of software model for proposed pipelined ADC. Section IV discusses the schematic design of pipelined ADC and layout design. Section V presents conclusion. a) Architecture of Pipelined ADC The purpose of analog to digital converts is to sample and digitize an analog signal. The more precisely the analog signal is converted to digital, the more information can be obtained from it. It is also desirable to convert high bandwidth or high frequency analog signals; thus, ADCs must be capable of a fast sampling rate as well being accurate. The pipeline ADC is the architecture of choice for applications that require both speed and accuracy and where latency is not ear 2012 Y concern. The basic idea behind the pipeline ADC is that each stage will first sample and hold the input then it is compared with VREF/2. If the input is greater than VREF/2, output a 1 for that stage and pass the input voltage directly to the next stage. If the input is less than VREF/2, output a 0 for that stage and multiply the input voltage by 2 before passing it to the next stage. Figure **??** shows the block diagram for this basic operation. Fig. **??** : Pipeline ADC Block Diagram [1] There are a few challenges with the basic pipeline ADC architecture that this project will attempt to address. Before looking at the sources of error, it is worth noting that an error in the early stages of the pipeline will propagate through the pipeline affectively being amplified by 2 by each successive stage. Errors can be created by the comparators not switching at the correct point. This means that the comparator may have some offset which will result in it making the wrong decision. The sample and hold may also have some offset causing the wrong voltage to be passed to the comparator which will result in the same problem of the comparator making a wrong decision. The other source of error is the multiply by 2 function, because it is difficult to multiply by a gain of exactly 2. These limitations with real op-amps and comparators will result in integral nonlinearity (INL) and differential nonlinearity (DNL) errors. This design requires 12-bit resolution. This means that there will be 2 12 or 4096 possible output bit combinations. Assuming a VREF of 1V, 1LSB or the level of analog resolution is given by To correct the errors caused by the offsets in the comparators and the sample and hold op-amps, a technique called 1.5 bits/stage will be used. The name 1.5 bits/stage is based on the fact that each stage has an output with three possible cases consisting of a and b signals, where ab can be 00, 01, or 11. The ideal transfer curve for the 1.5 bits/stage of vin versus vout is shown in Figure 2. And, the relationship between vin and vout can be expressed as: The functional block diagram of the pipelined ADC is simulated using Simulink in MATLAB. The 1-bit single stage converter behavioural block has been designed and simulated. The behaviour of the block has been developed using the equations given below.? If Vin > Vmid Vresidue=2(Vin-Vref) ? If Vin < Vmid Vresidue=2(Vin)

Using a reference value this single stage block would act as a comparator and gives a bit as output. Again that bit will be converted in to analog value that value again compared with the actual input signal and the difference signal will be produced. The difference signal will be in the range of half of the actual input range. Since the total pipelined architecture has been developed using these similar types of 1-bit single stage blocks should give the same input rage to all stages. To get that voltage range we should multiply the error signal with 2 then we can give output of one stage to input of next stage. Every stage has its own sample and hold circuit operating at 100 MS/s. the output of the sample and hold stage will be consider as the input to the 1-bit converter. Figure 3 shows the software reference model of 1-bit conversion. The 3dB Bandwidth of the op-amp is selected as 100 MHz to meet the application of the architecture. The schematic has simulated by the cadence specter and layout has drawn by the virtuoso. The simulated transient and ac analysis waveforms are shown in the Figure **??**. The digital outputs for a given input analog sample are not generated at the same time. MSB comes first and LSB last. The time delay between adjacent bits is one half clock cycle. All bits need to be synchronized. The 1-bit digital output from the first stage is delayed by 12 half cycles and the output from the second stage is delayed by 11 half cycles and so on. The output from the last stage is delayed by a half cycle. The delay block is made of D flip-flops (DFF) implemented with transmission gate and static NAND gates. Since sampling rate is only 100 MS/s and the word length is 12 bits the carry ripple is not an issue under 0.13µm process.

g) 1-Bit Single stage of Pipelined Architecture This stage is consist of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. The analog signal will be sampled and fed to the comparator acts as the 1-bit ADC that would give the 1-bit digital output. Before giving to the comparator the sample signal should lift to the 0.9V of the DC voltage, so that the comparator can compare the value to the threshold voltage and give the output.

2 Conclusion

The goals of this paper is First different ADC architectures were analyzed to determine the optimal topology for the given performance specifications with minimum power consumption. Second the exact implementation of the chosen architecture was investigated in an effort to use the minimum amount of power. This Paper involved designing an integrated CMOS Analog-to-Digital converter for communication and video applications. The performance specifications were 12-bits, power dissipation less than 70 mW, area should be less than 6.5mm 2 and static performance parameters such as INL and DNL should be less than 1 LSB and 0.5 LSB in order to make a monotonic ADC. This pipelined ADC has been met the performance requirements. The ADC was designed in 0.13um technology at an operating voltage of ±1.8 V. Sample and hold circuit is designed by the switched-capacitor implementation. We can use the rail to rail op amp to increase the input voltage range of the ADC but by increasing the input voltage swing the resolution will be affected. Common-mode drift issue Since there is no common-mode feedback inside the loop the commonmode drift caused by the mismatch of capacitors, offset of op amp and charge injection will accumulate stage by stage. Careful design and layout are supposed to minimize the total drift within 100 mV such that the residue output signal will not be out of saturation. But this problem is likely to cause trouble if the commonmode signal is not controlled well as expected.

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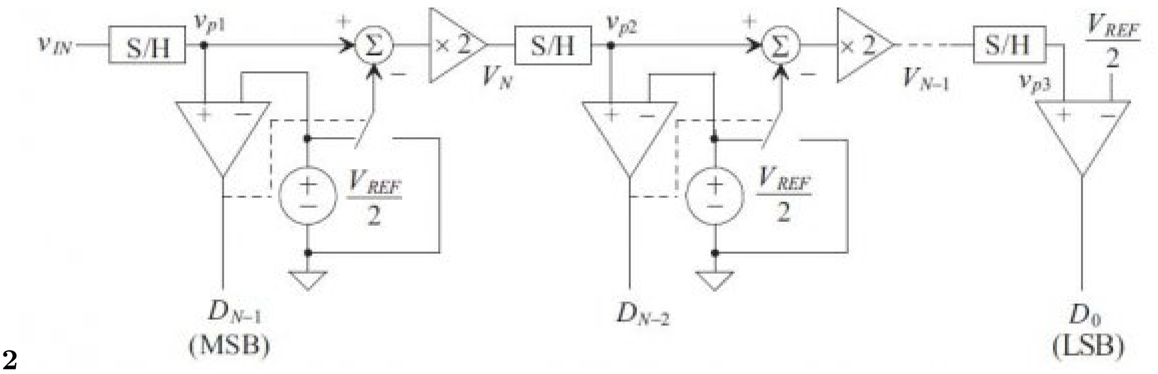
Figure 1: M



2

Figure 2: Fig. 2 :

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$$1LSB = \frac{V_{REF}}{2^N} = \frac{1}{4096} = 244\mu V$$

3

Figure 3: Fig. 3 :

$$v_{out} = 2 \cdot \left(v_{in} + \overline{ab}\frac{V_{CM}}{2} - \bar{a}b\frac{V_{CM}}{2} - ab\frac{3V_{CM}}{2} \right).$$

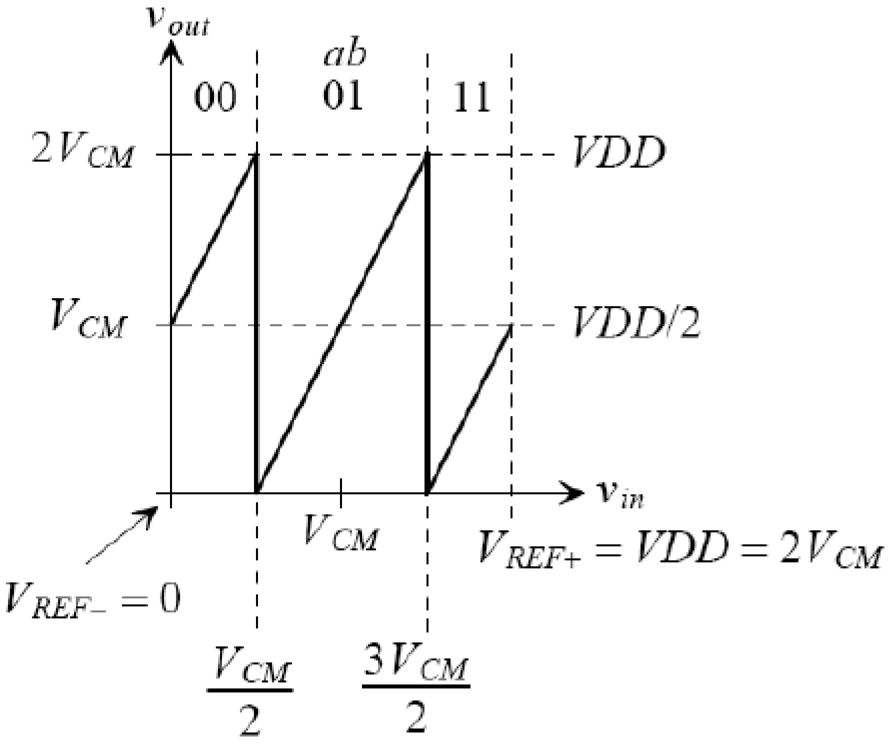

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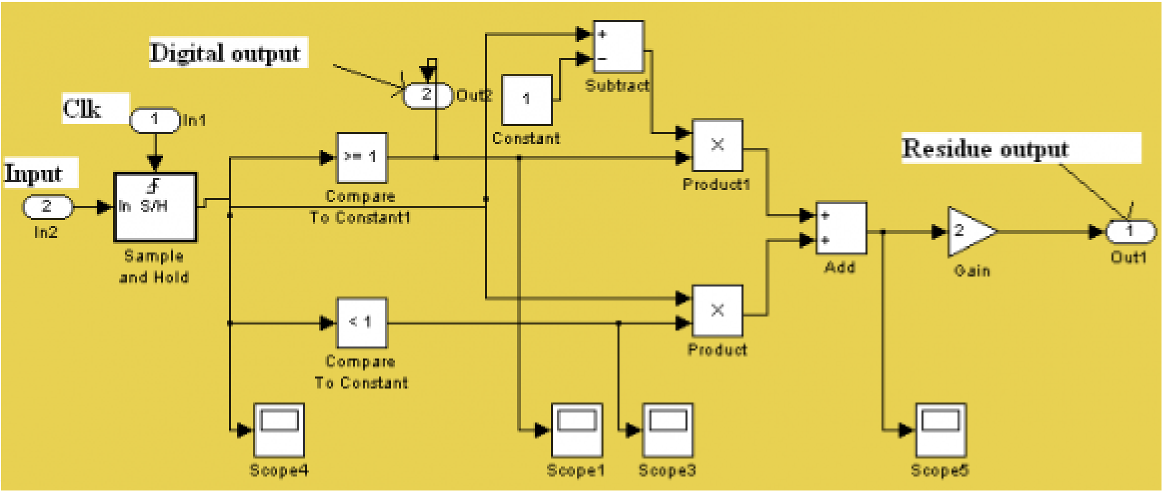
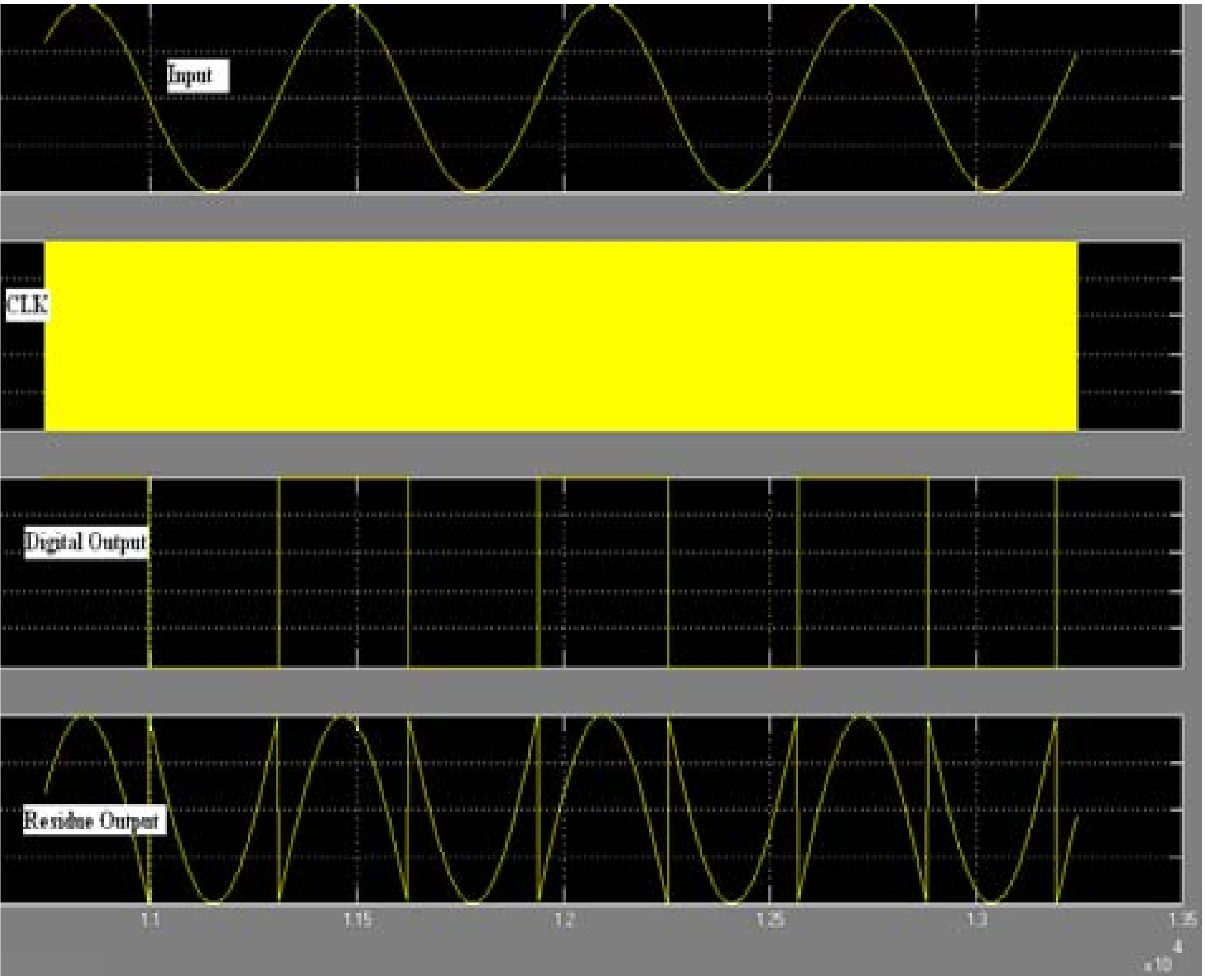
Figure 4: Fig 4 :Fig. 6 :Fig. 7 :



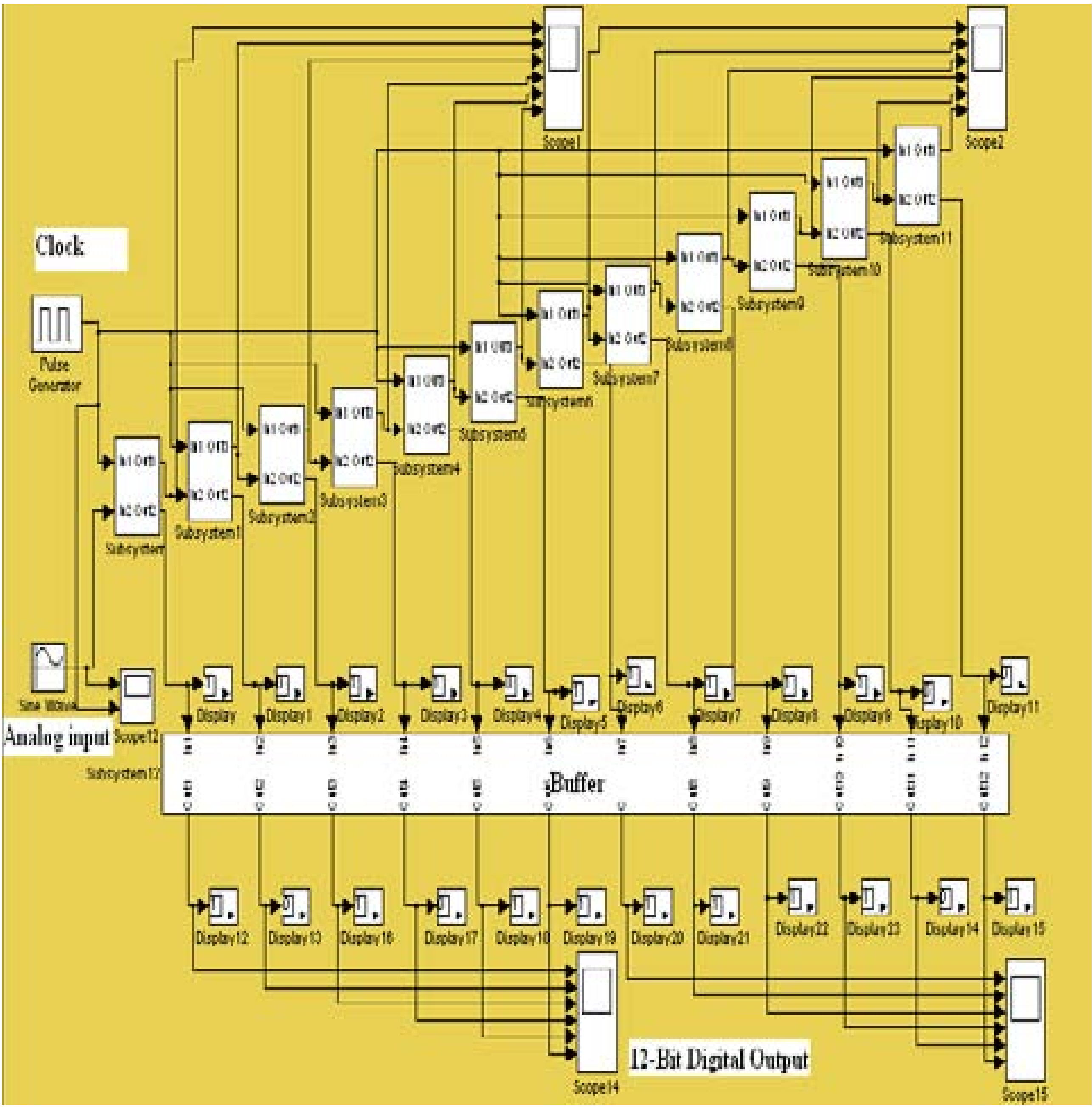
89

Figure 5: Fig. 8 :Fig. 9 :



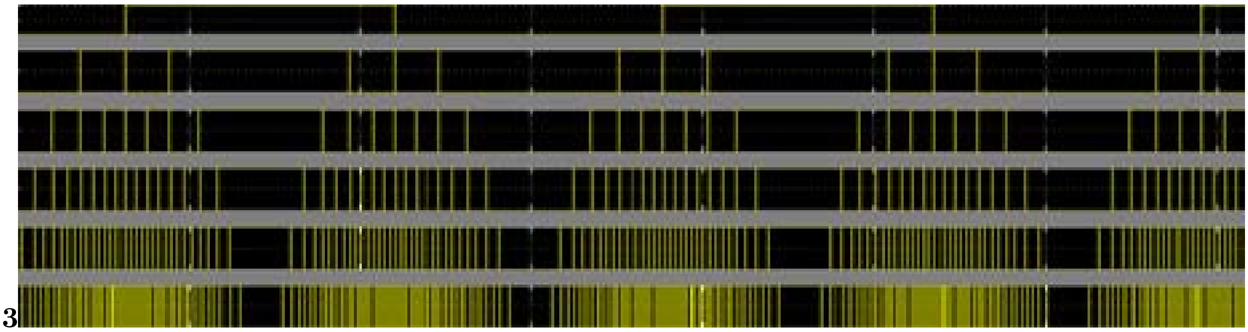
10

Figure 6: Fig. 10 :



11

Figure 7: Fig. 11 :



1213

Figure 8: Fig. 12 :Fig. 13 :

14

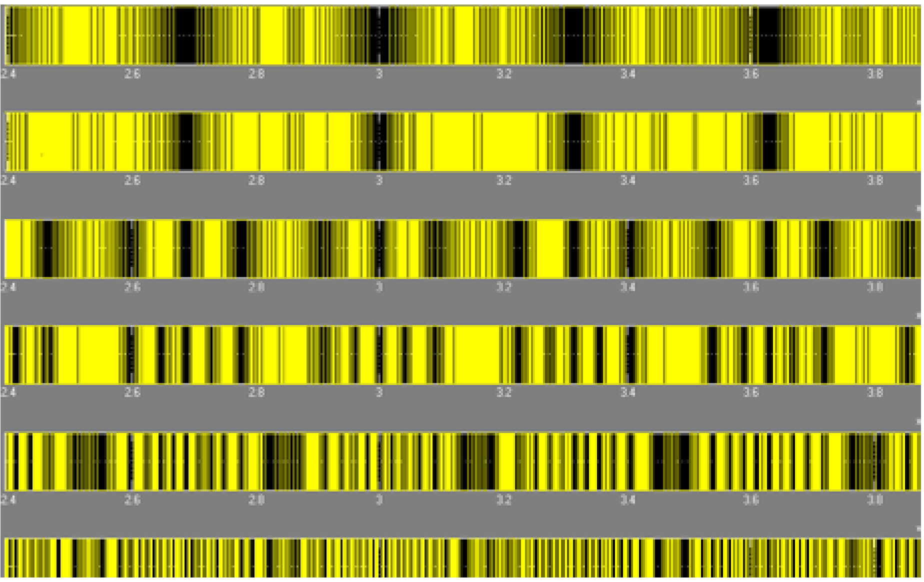


Figure 9: Fig. 14 :

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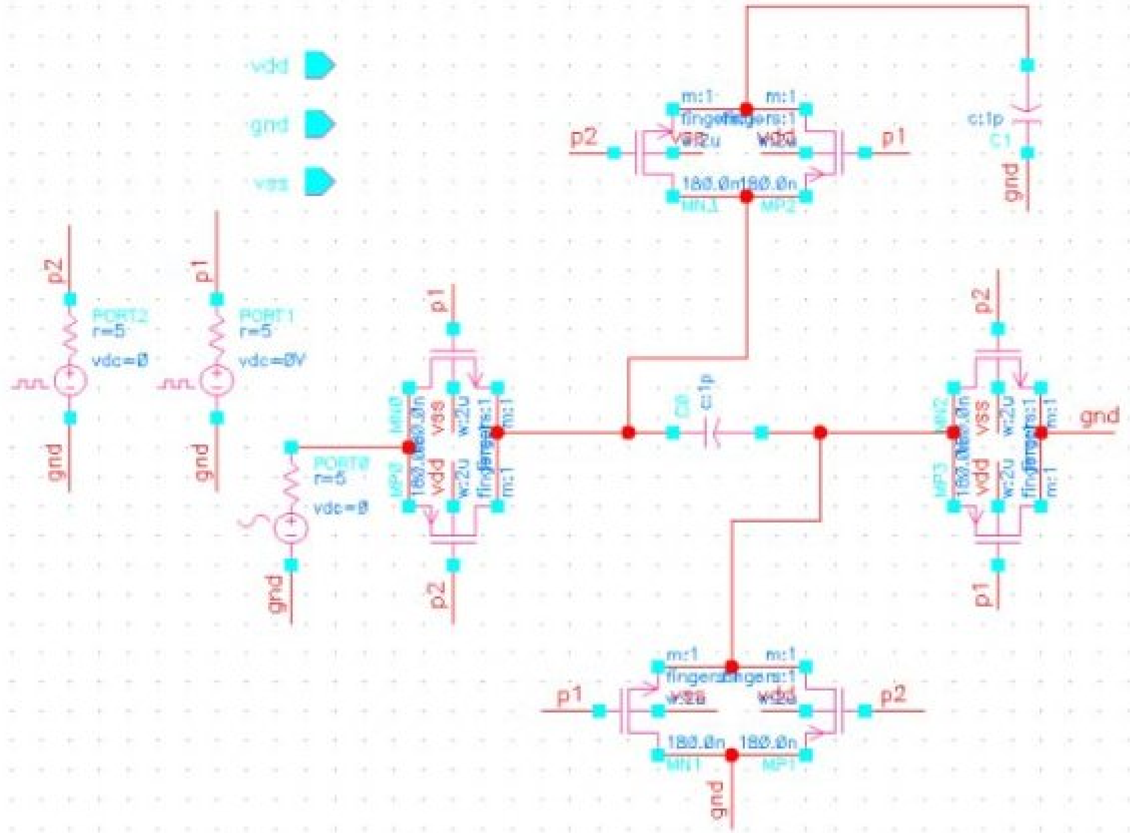
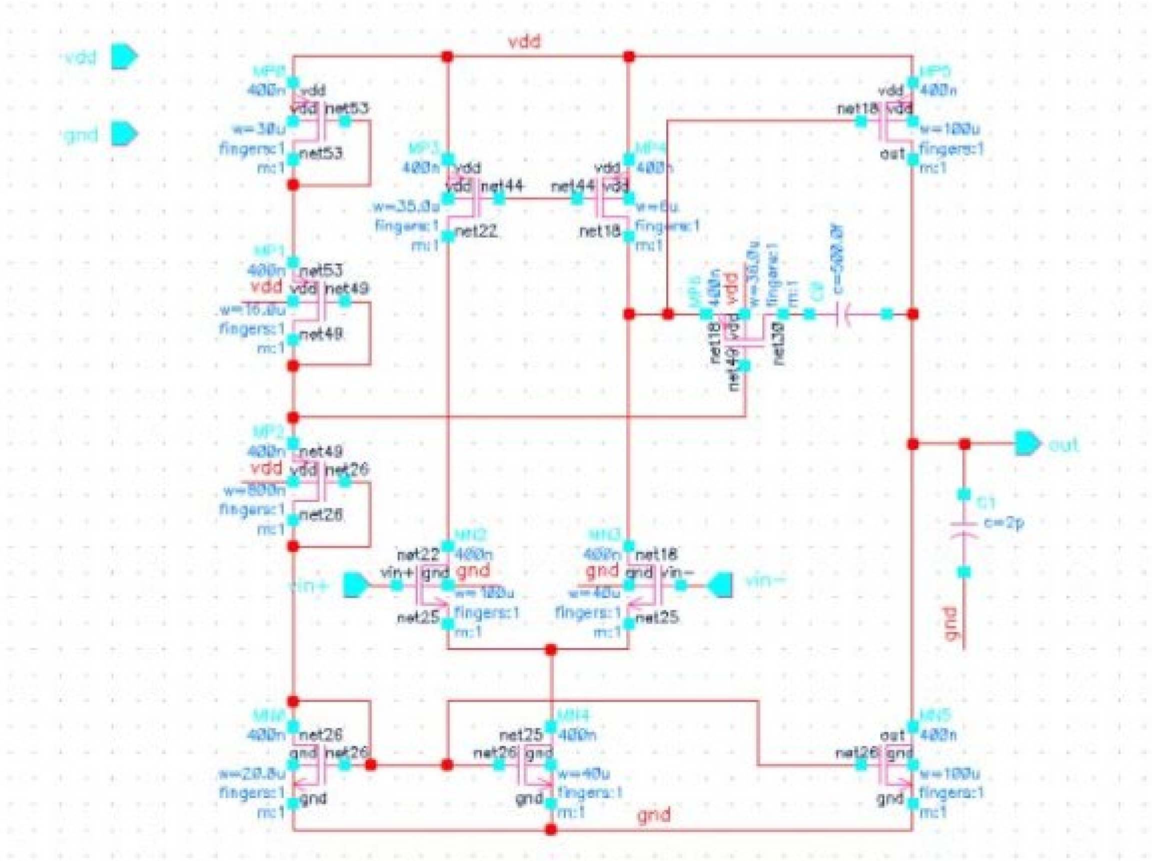


Figure 10: Fig. 15 :


vdd
gnd
MP0
400n
w=30u
fingers:1
m:1
net53
MP1
400n
w=16.0u
fingers:1
m:1
net49
MP2
400n
w=800n
fingers:1
m:1
net26
MP3
400n
w=35.0u
fingers:1
m:1
net44
net22
MP4
400n
w=6u
fingers:1
m:1
net18
MP5
400n
w=100u
fingers:1
m:1
out
MP6
400n
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m:1
vin−
MN0
400n
w=20.0u
fingers:1
m:1
MN4
400n
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MN5
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m:1
out
C1
c=2p

Figure 11:

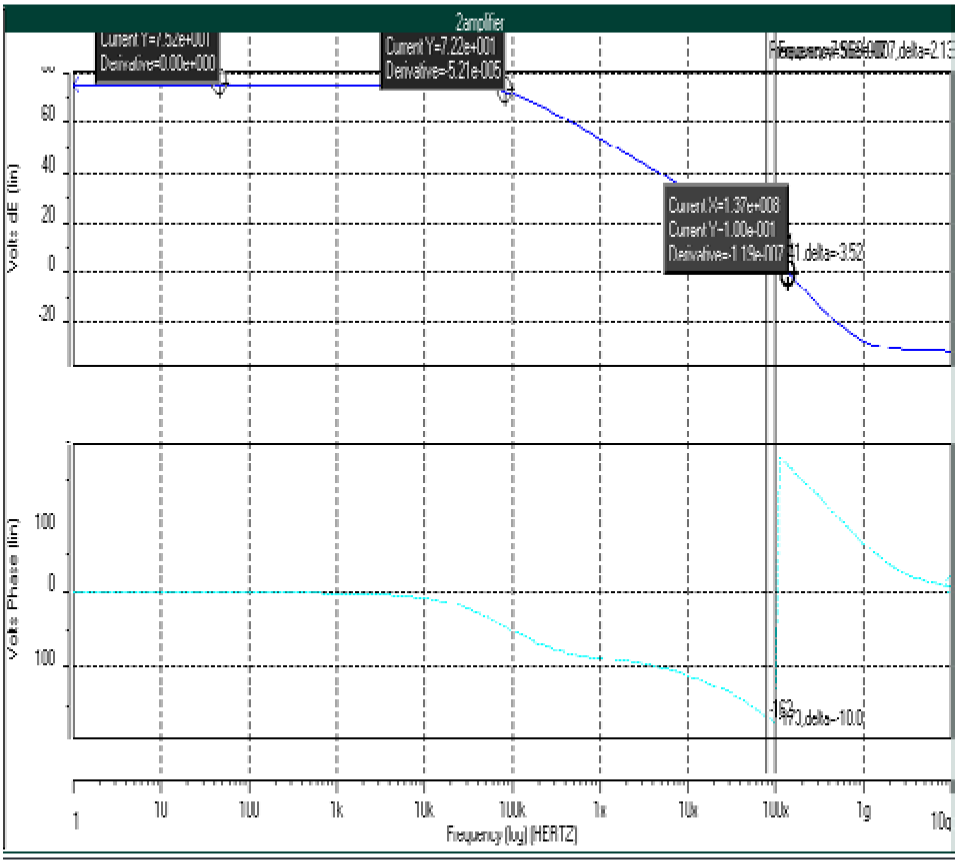

Figure 12:

1

		Previous work	Present Work
Technology		CMOS 0.35um	CMOS0.13um
Power Supply 3V			± 1.8V
Input Freq	Signal	200kHz	up to 10 MHz
Input range	voltage	—	+/-250mV
Power dissipation		290uW	70mW
Area		7.9 mm2	6.5 mm2
Sampling freq 75MHz			100 MHz

Figure 13: Table 1

1

Figure 14: Table 1 :

[Cline and Gray] , D W Cline , P R Gray . p. 13.

[Yoo (2003)] ‘A 10 b 150 MS/s 123 mW 0.18 _m CMOS Pipelined ADC’. S.-M Yoo . *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2003. p. .

[Loloee et al. ()] *A 12 bit 80 Msps Pipelined ADC Core with 190mw consumption from 3v in 0.18um Digital CMOS*, Arash Loloee , Alfio Zanchi , Shereef Huawen Jin , Eduardo Shehata , Bartolome . 2002. Dallas, TX(U.S: Texas Instruments, Inc.-Wireless Infrastructure Data Converters 12500 TI Boulevard. p. .

[Murmann and Boser (2003)] ‘A 12-Bit 75-MS/s Pipelined ADC Using Open-loop Residue Amplification’. Boris Murmann , Bernhard E Boser . *IEEE Journal of Solid-State Circuits* Dec. 2003. 38 (12) p. .

[Singer and Brooks (1996)] ‘A 14-bit 10-MHz calibration-free CMOS pipelined A/D converter’. L A Singer , T L Brooks . *Symp. VLSI Circuits Dig. Tech. Papers*, June 1996. p. .

[Yu and Lee (1996)] ‘A 2.5-V, 12-b, 5-Msample/s pipeline CMOS ADC’. P C Yu , H.-S Lee . *IEEE J. Solid-State Circuits* Dec. 1996. 31 p. .

[Varzaghani and Yang (2006)] ‘A 600 MS/s 5-bit pipelined analog-to-digital converter using Digital reference Calibration’. A Varzaghani , C K K Yang . *IEEE Journal of Solid-State Circuits* Feb. 2006. 41 (2) p. .

[Min et al. (2003)] ‘A 69 mW 10 b 80 MS/s pipelined CMOS ADC’. B.-M Min , P Kim , D Boisvert . *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2003. p. .

[Ghovanloo] *A Classic Wide Band Operational Amplifier Design*, Maysam Ghovanloo . Ann Arbor, MI. p. . University of Michigan

[Ming and Lewis (2000)] ‘An 8 b 80 MSample/s pipelined ADC with background calibration’. J Ming , S H Lewis . *IEEE Int. Solid-State Circuits Conf. Dig.Tech. Papers*, Feb. 2000. p. .

[Ming and Lewis (2000)] ‘An 8 b 80 MSample/s pipelined ADC with background calibration’. J Ming , S H Lewis . *IEEE Int. Solid-State Circuits Conference*, Feb. 2000. p. .

[Blecker et al. (2000)] ‘An 8-bit 13-MSamples/s digital-backgroundcalibrated algorithmic ADC’. E B Blecker , O E Erdogan , P J Hurst , S H Lewis . *Proc. Eur. Solid-State Circuits Conf*, (Eur. Solid-State Circuits ConfStockholm, Sweden) Sept. 2000. p. .

[Annema (1999)] ‘Analog circuit performance and process scaling’. A.-J Annema . *IEEE Trans. Circuits Syst. II* June 1999. 46 p. .

[Johns and Martin ()] *Analog Integrated Circuit Design*, D Johns , K Martin . 1997. New York: John Wiley.

[Cho and Gray] T Cho , P R Gray . *A10 b*, p. 20.

[Allen Holberg and Baker ()] ‘CMOS Mixed Signal Circuit Design’. Phillip E Allen & Holberg , ; R Jacob Baker . *CMOS Analog Circuit Design*, 2002. 2002. Oxford University Press. (NJ)

[Rabaey ()] *Digital Integrated Circuits-A design Perspective*, J M Rabaey . 1996. Prentice Hall India.

[Lewis and Gray] S H Lewis , P R Gray . *A pipelined 5*,

[Arias et al. (2004)] ‘Low-Power Pipeline ADC for Wireless LANs’. J Arias , V Boccuzzi , L Quintanilla , L Enríquez , D Bisbal , M Banu , J Barbolla . *IEEE Journal of Solid-State Circuits* Aug. 2004. 39 (8) p. .

[Msample/s 9-bit analog-todigital converter IEEE J. Solid-State Circuits (1987)] ‘Msample/s 9-bit analog-todigital converter’. *IEEE J. Solid-State Circuits* Dec. 1987. p. . (SC-22)

[MSample/s, 35mWpipeline A/D converter IEEE J. Solid-State Circuits (1995)] ‘MSample/s, 35mWpipeline A/D converter’. *IEEE J. Solid-State Circuits* Mar. 1995. 30 p. .

[Msamples/s pipelined analog to-digital converter in 1.2-_m CMOS IEEE J. Solid-State Circuits (1996)] ‘Msamples/s pipelined analog to-digital converter in 1.2-_m CMOS’. *IEEE J. Solid-State Circuits* Mar. 1996. 31 p. .

[Lewis (1992)] ‘Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications’. S H Lewis . *IEEE Trans.Circuits Syst. II* Aug. 1992. 39 p. .

[Goes et al. (1998)] ‘Systematic design for optimization of high-speed self-calibrated pipelined A/D converters’. J Goes , J C Vital , J E Franca . *IEEE Trans.Circuits Syst. II* Dec. 1998. 45 p. .

[Tangel and Kyusun] Ali Tangel , Choi Kyusun . *The CMOS Inverter as a comparator in ADC designs*, (University Park, PA16802 USA) The Pennsylvania State University