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# Area Optimized High Throughput IDMWT/DMWT Processor for OFDM on Virtex-5 FPGA

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## Abstract

OFDM is one of the most popular modulation techniques that is been widely used in most of the wireless and wired communication links. The OFDM architecture consists of QAM modulator and orthogonal frequency modulator. In this work we propose DMWT based orthogonal frequency modulator for achieving higher BER. The IDMWT architecture is designed considering N=4, thus the preprocessing unit converts the QAM samples of N to 2N and is modulated using DMWT filters. The filtered output is further transmitted and is received at the receiver. During the post processing, N samples are extracted by use of DMWT demodulation technique. The complex architecture of IDMWT and DMWT are reduced for its complexity and speed by the modified architecture. The DMWT architecture is modified for FPGA implementation improving the area, power and speed performances. The modified DMWT architecture is implemented on VirtexII pro FPGA which operates at 300MHz frequency and occupies area of less than 1

***Index terms—***

## 1 INTRODUCTION

he FFT based OFDM uses complex exponential bases function to reduce interference hence it was replaced with wavelets to produce better performance at the cost of loss in orthogonality between the carriers [1] [2]. Mutiwavelets preserves high frequency components and also increases sensitivity better than scalar wavelets [7]. Multiwavelets show the perfect union of symmetry, orthogonally, finitely support and smoothness **??**8]. The design of orthogonal symmetric prefilter banks is shown with the discrete multiwavelet transform for image coding and digital communications. The new DMWT structure increases computational complexity, energy compaction ratio as well as the compression performance when applying to a VQ based image coding system[9][10]. A biorthogonal multi-wavelets filter has many characteristics, such as symmetry, compact support, orthogonality and 3-order vanishing moment **??**11].

The Fourier based OFDM (FFT-OFDM) use the complex exponential bases functions and it's replaced by an orthonormal wavelets in order to reduce the level of interference. It is found that OFDM based on Haarbased orthonormal wavelets (DWT-OFDM) are capable of reducing the inter symbol interference ISI and inter carrier interference ICI, which are caused by the loss in orthogonality between the carriers [1] [2].

To further improve the performance gains a new transform is implemented based on Multifilters called Multiwavelets (DMWT-OFDM). These filters shows more properties which is not achievable in other transforms (Fourier and wavelet) [3].

A most important Multiwavelets filter is the GHM filter proposed by Geronimo, Hardian, and Massopust The Multiwavelets functions coefficients are 2X2 matrices ,and they must multiply vectors instead of scalars during transformation step. Thus multifilter bank requires 2 input rows. To start the analysis algorithm and to reduce the noise effects , the preprocessing step associates given scalar input signal of length N to a sequence of length-2 vectors[4] [5].

# 2 II.

# 3 Proposed System For Dmwt-Ofdm

The block diagram of the proposed system for OFDM is depicted in figure (1). The S/P converter, the signal demapper and the insertion of training sequence are same as in DWT-OFDM. After that, a computation of IDMWT for 1-D signal is achieved by using an over-sampled scheme of preprocessing (repeated row), the IDMWT matrix is doubled in dimension compared with that of the input, which is a square matrix of NxN, where N is in power of 2. Transformation matrix dimensions is equal to input signal dimensions after preprocessing. To compute a single-level 1-D discrete multiwavelets transform, the next steps are:

1. Checking input dimensions: With input vector of length N, where N is in power of 2.

2. Constructing a transformation matrix W as in 3, using GHM low and high pass filters matrices given in 1 and 2, after substituting GHM matrix filter coefficients values, a 2NX2N transformation matrix results. 9 0 G ? ? ? ? ? ? ? ? ? ? ? ? ? ? = 0 2 10 1 0 20 1 3 G ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? = 1 0 3 2 3 2 1 0 3 2 1 0 3 2 1 0 1 0 3 2 3 2 1 0 3 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 G G G G G G G G G G G G G G G G G H H H H H H H H H H H H H W ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? 3.

Preprocessing the input signal by repeating the input stream with the same stream multiplied by a constant ? , for GHM system functions 2 / 1 = ? . 4. Transformation of input vector which can be done by apply matrix multiplication to the 2NX2N constructed transformation matrix by the 2NX1 preprocessing input vector.

# 4 III. Software Reference Model Results

In this section the simulation of the proposed DMWT-OFDM system in MATLAB version 7 are achieved. And the bit error rate (BER) performance of the OFDM system considered in different channel models, the additive white Gaussian noise (AWGN) channel, the flat fading channel, and the selective fading channel [6].

# 5 a) Performance of dmwt-ofdm in awgn channel

In this section, the result of the simulation for the proposed DMWT-OFDM system is calculated and shown in figure (3), which give the BER performance of DMWT-OFDM in AWGN channel. It is shown clearly that the DMWT-OFDM is much better than the two previous system FFT-OFDM and DWT-OFDM. This is a reflection to the fact that the orthogonal bases of the multiwavelets is much significant than the orthogonal bases used in FFT-OFDM and DWT-OFDM.

# 6 IV. Design Of Dmwt/Idmwt Architecture

In this work, design and FPGA implementation of a hardware efficient DMWT architecture is carried out. The QAM modulated data which generates the I and Q channel signals are preprocessed and is modulated using IDMWT, the OFDM modulated data is transmitted through AWGN channel and is demodulated using DMWT, the base band signal is extracted using QAM demodulation. Figure **??** shows the detailed block diagram of OFDM modulation and demodulation. The input signal is considered as 1MHz signal with sampling frequency of 64Msps, the QAM modulator carrier frequency is chosen to be 64 MHz, the QAM symbols are obtained at 512Msps. The OFDM modulator has to process the modulated data at the rate of 512Msps. From the previous discussions, it is found that prior to OFDM modulation, the input samples are to be scaled and extended as 2N x 1 vector, which is the requirement for GHM based IDMWT. In order to achieve this the pre processing unit performs the scaling and extension operation, thus the incoming samples to preprocessing that are at 512Msps are preprocessed to 2N x1 with 1024 Msps. The preprocessed data is to be processed using IDMWT, this has to operate at frequency greater than 1024Msps.

V.

# 7 Design Of Idmwt

In this work, we select N=4, thus the QAM symbols are grouped into frames of 4 samples and is preprocessed. With N=4, the preprocessing unit extends the samples to 8 with scaling. The scaled samples are to be processed in the IDMWT with GHM wavelets of size 2N x 2N, with N=8, the GHM filter size is 8 x 8. The GHM filter for N=4 is given in equationW= ? ? ? ? ? ? ? ? ? ? ? ? ? ? 1 0 3 2 3 2 1 0 1 4 3 2 3 2 1 0 G G G G G G G G H H H H H H H H

As we perform inverse IDMWT, the GHM filter coefficients are:W= ? ? ? ? ? ? ? ? ? ? ? ? ? ? 1 3 1 3 0 2 0 2 3 1 3 1 2 0 2 0 G G H H G G H H G G H H G G H H

Using the above equation, the preprocessed data is modulated to generate OFDM signal. The OFDM signal using GHM filter can be mathematically represented as:[ ] [ ][ ] [ ][ ][ ] 1 2 2 2 1 2 WT NX N NX NX X Y =

The above equation is implemented on FPGA. The input matrix is first stored in a memory of size Mx8, where M is an integer of size 1024. The input memory is loaded from the preprocessing unit. The controller reads the data from input memory into a intermediate memory of size 8x8, the controller also reads the corresponding GHM coefficients from memory. The input is multiplied and accumulated using dedicated multipliers on FPGA to compute the output samples. Modified DMWT architecture:

In the previous section the BER performance is analyzed and now the GHM matrix coefficients were calculated and substituted in equations 1, 2and 3 the equations 4 to 11 are derived to design multiwavelets. Here it is scaled scaling factor 128. The table below shows co-efficient before and after scaling. **??**————————( **??**————————( **??**————————-( From the above equations it is found that to compute every output sample, it is required to perform minimum of 3 multiplications and 2 additions. Thus for N=4, the number of multiplications and additions are 28 multiplications and 20 additions respectively. The number of multiplications and additions are reduced by more than 50%. This reduction in multiplication and addition optimizes the design in terms of area and power requirement. It is also found that the latency of the design is 8N clock cycles, but throughput is 7N clock cycles, which is faster compared with existing design which is 8N-1. The latency and throughput can be further improved with parallel and pipelining architecture.

# 8 VII. Fpga Implementation Of Modified Dmwt/Idmwt

The HDL model for the modified equations of GHM filter is developed and simulated using ModeSim. Multiple test cases are chosen to test the functionality of the modified equation and is verified against software reference model results. The functionally correct HL code is synthesized using Xilinx ISE 10.1 targetting VirtexII pro FPGA. Next section discuss the results of FPGA implementation. the design is perfectly mapped onto FPGA meeting the required design specifications.

The HDL co simulation of the design is performed using simulation which is shown in Figure5 below.

# 9 HDL CO-Simulation

# 10 Conclusion

In this work, we propose a modified GHM filter architecture for OFDM modulation and demodulation. Software reference model for DMWT based OFDM model is developed and simulated to find the BER performances for various SNRs. The simulation results show that the DMWT OFDM model outperforms FFT and DWT based OFDM models. The DMWT coefficients that are fractions are converted to integers and are modified to reduce the number of multiplications and additions. The reduced GHM filter coefficients are used to process the QAM modulated data, thus reducing the computation complexity and making it suitable for FPGA implementation. The modified equations are modeled using HDL and implemented on FPGA VirtexII pro. The design operates at maximum frequency of 300MHz and consumes less than 1% resources and thus is suitable for real time applications. The design can be further improved for its latency and throughput by designing a [1]


1

Figure 1: Figure 1 :

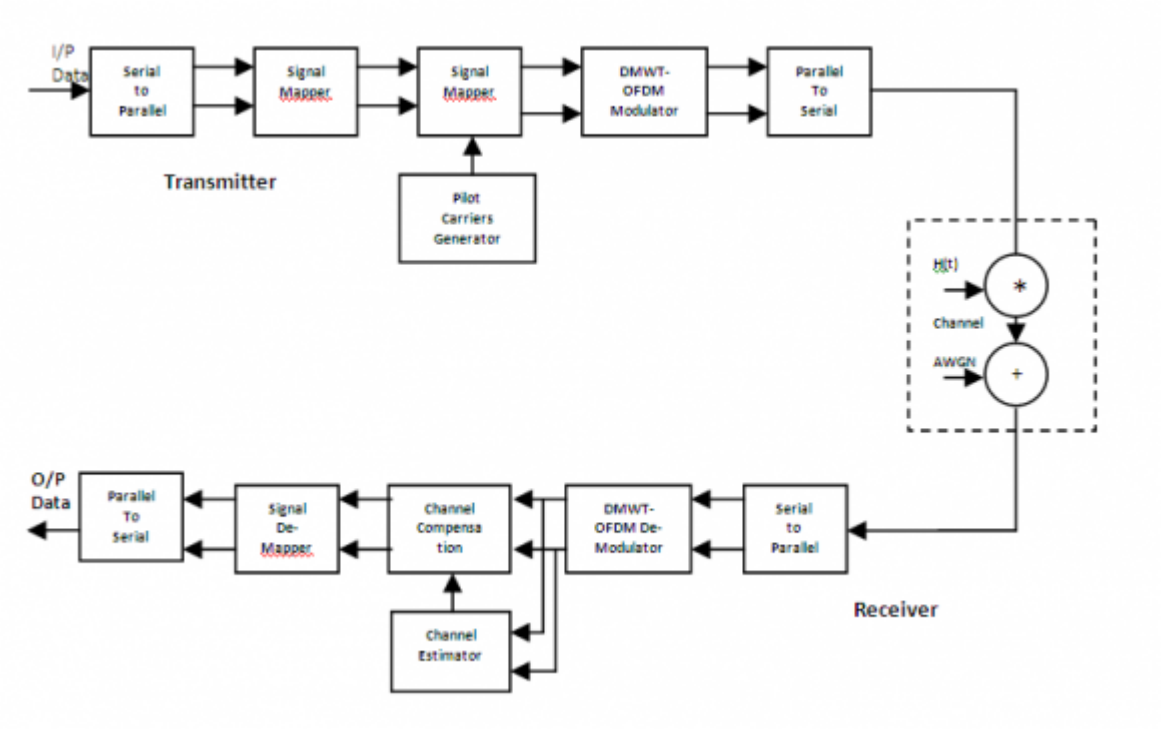
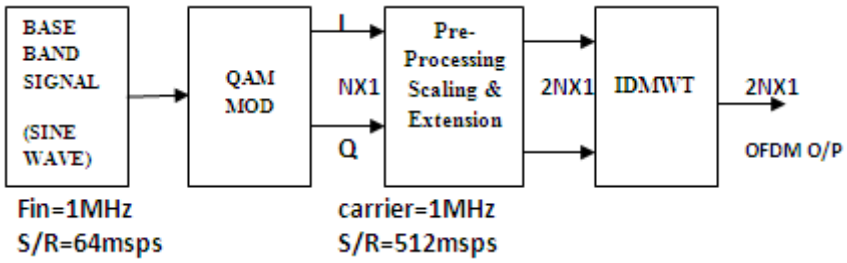



Figure 2:




3

Figure 3: FFigure 3 :

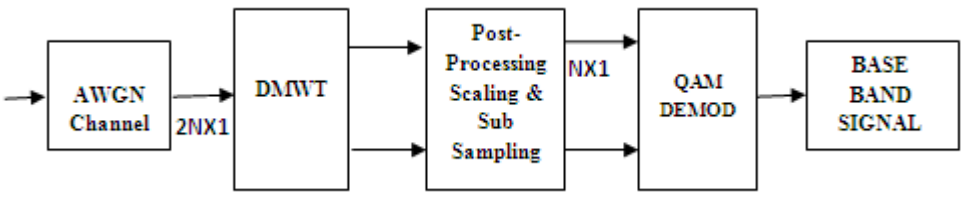



Figure 4:

Figure 5: Table 1 :

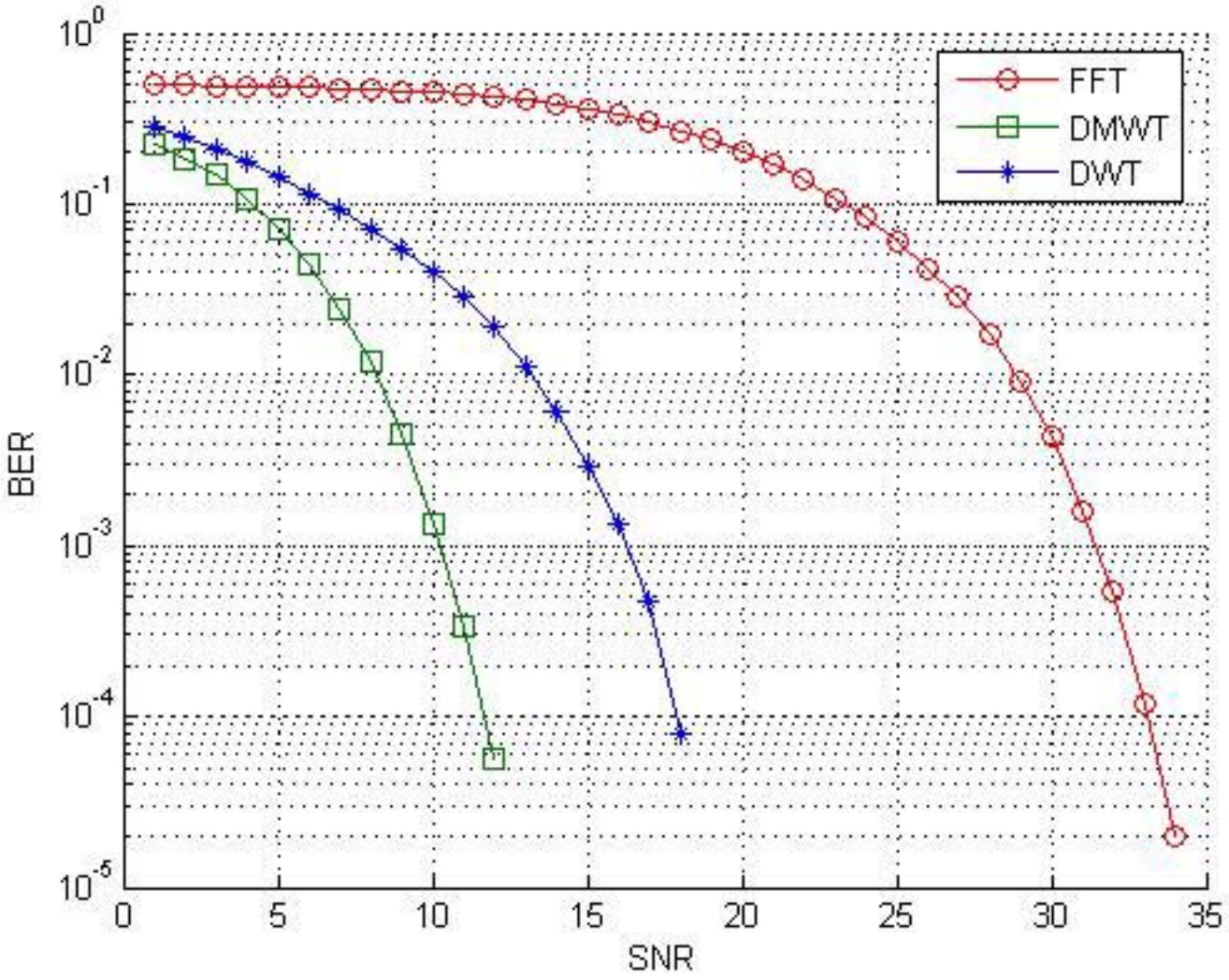



Figure 6:

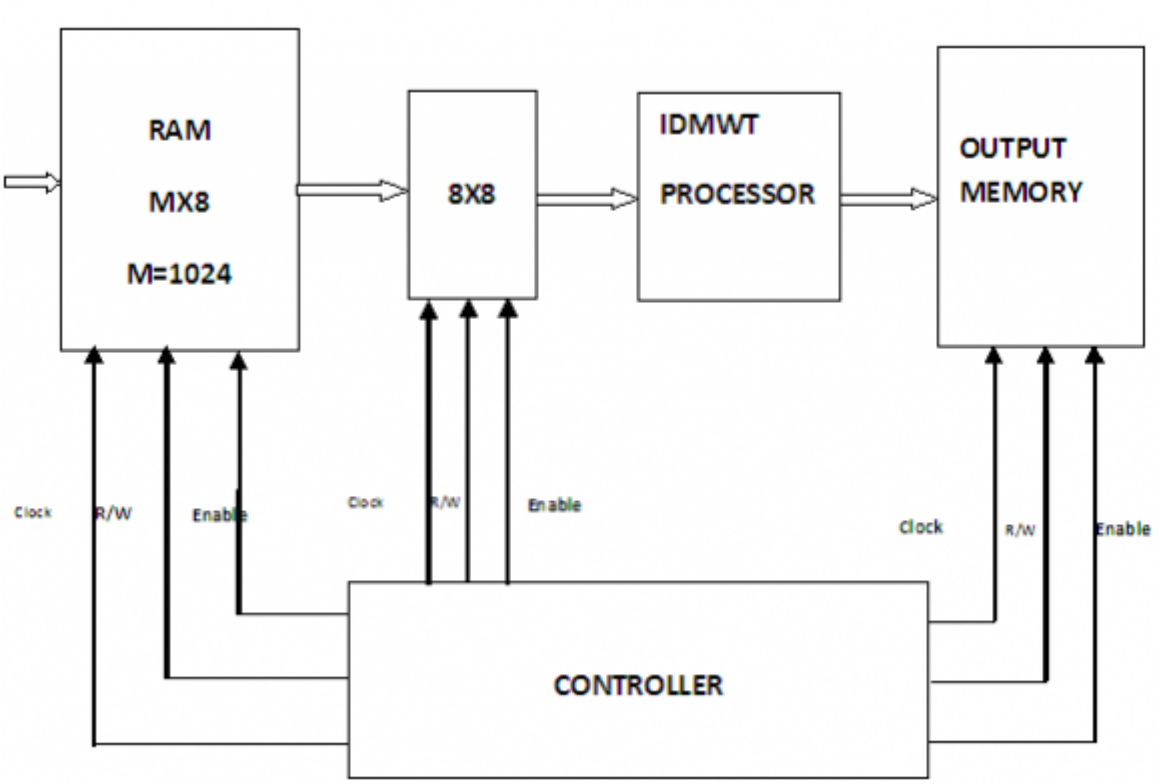



Figure 7:

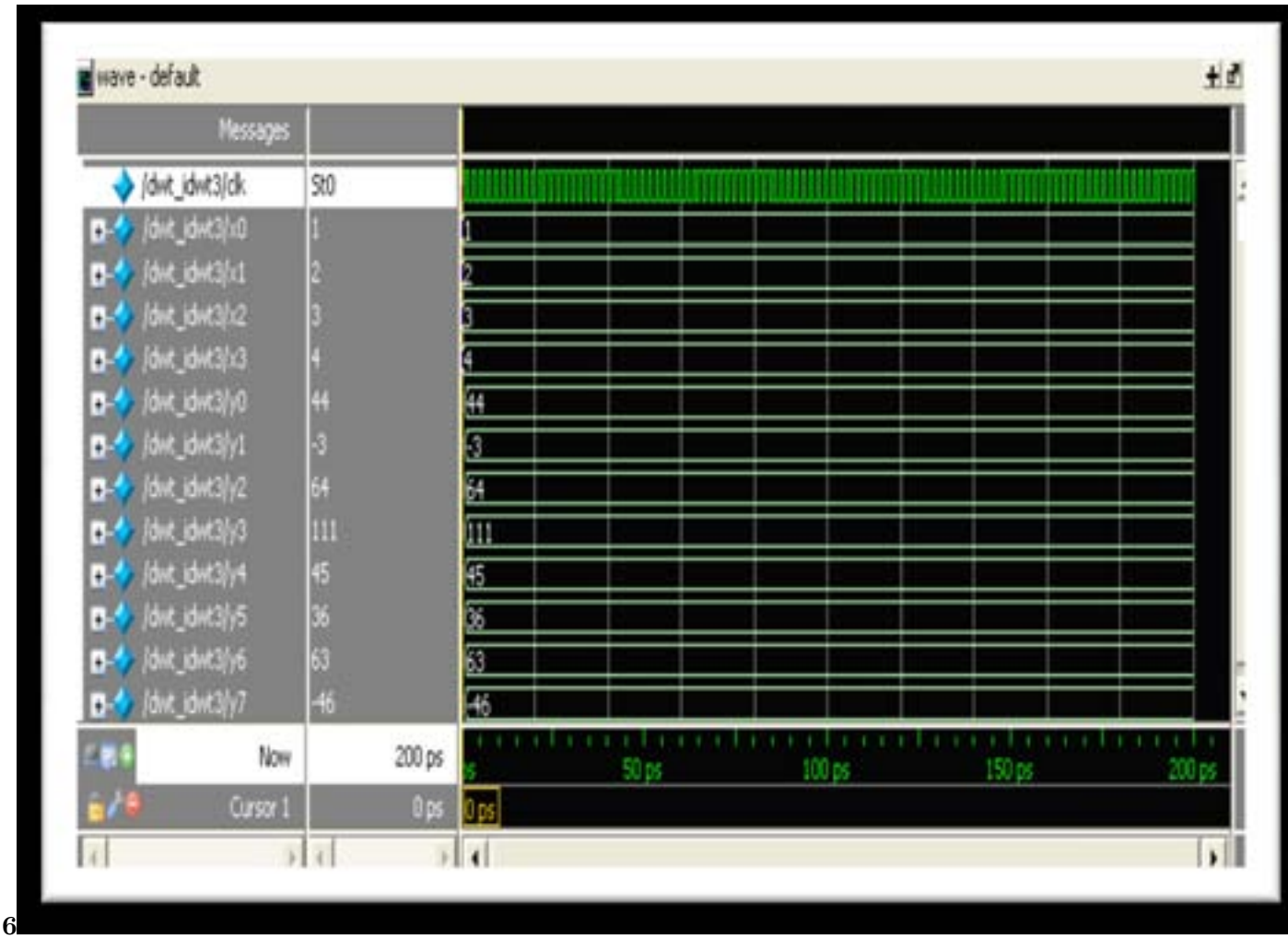
| Before Scaling | After Scaling |
|---|---|
| 3/5√2 | 54 |
| 4/3 | 170 |
| 0.26819 | 34 |
| 0.1707 | 22 |
| 0.4145 | 53 |
| 0.7070 | 90 |
| 3/10 | 38 |
| 2/3 | 84 |
| 1/2 | 64 |
| 0.5207 | 66 |
| 0.08787 | 11 |
| 0.5207 | 68 |
| 0.362 | 46 |
| 0.6864 | 88 |
| 0.3793 | 48 |

Figure 8:

$$\begin{bmatrix} Y0 \\ Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \\ Y6 \\ Y7 \end{bmatrix} = \begin{bmatrix} 3/5\sqrt{2} & 4/3 & -3/5\sqrt{2} & 0 & 0 & 0 & 0 & 0 \\ -1/20 & -3/10\sqrt{2} & 9/20 & 1/\sqrt{2} & 9/20 & -3/10\sqrt{2} & -1/20 & 0 \\ 0 & 0 & 0 & 0 & 3/5\sqrt{2} & 4/3 & 3/5\sqrt{2} & 0 \\ 9/20 & -3/10\sqrt{2} & -1/20 & 0 & -1/20 & -3/10\sqrt{2} & 9/20 & 1/\sqrt{2} \\ -1/20 & -3/10\sqrt{2} & 9/20 & -1/\sqrt{2} & 9/20 & -3/10\sqrt{2} & -1/20 & 0 \\ -1/10\sqrt{2} & 3/10 & 9/10\sqrt{2} & 0 & 9/10\sqrt{2} & -3/10 & -1/10\sqrt{2} & 0 \\ 9/20 & -3/10\sqrt{2} & -1/20 & 0 & -1/20 & -3/10\sqrt{2} & 9/20 & -1/\sqrt{2} \\ 9/10\sqrt{2} & -3/10 & -1/10\sqrt{2} & 0 & 1/10\sqrt{2} & -3/10 & 9/10\sqrt{2} & 0 \end{bmatrix} \begin{bmatrix} X0 \\ X1 \\ X2 \\ X3 \\ X0(1/\sqrt{2}) \\ X1/\sqrt{2} \\ X2/\sqrt{2} \\ X3/\sqrt{2} \end{bmatrix}$$

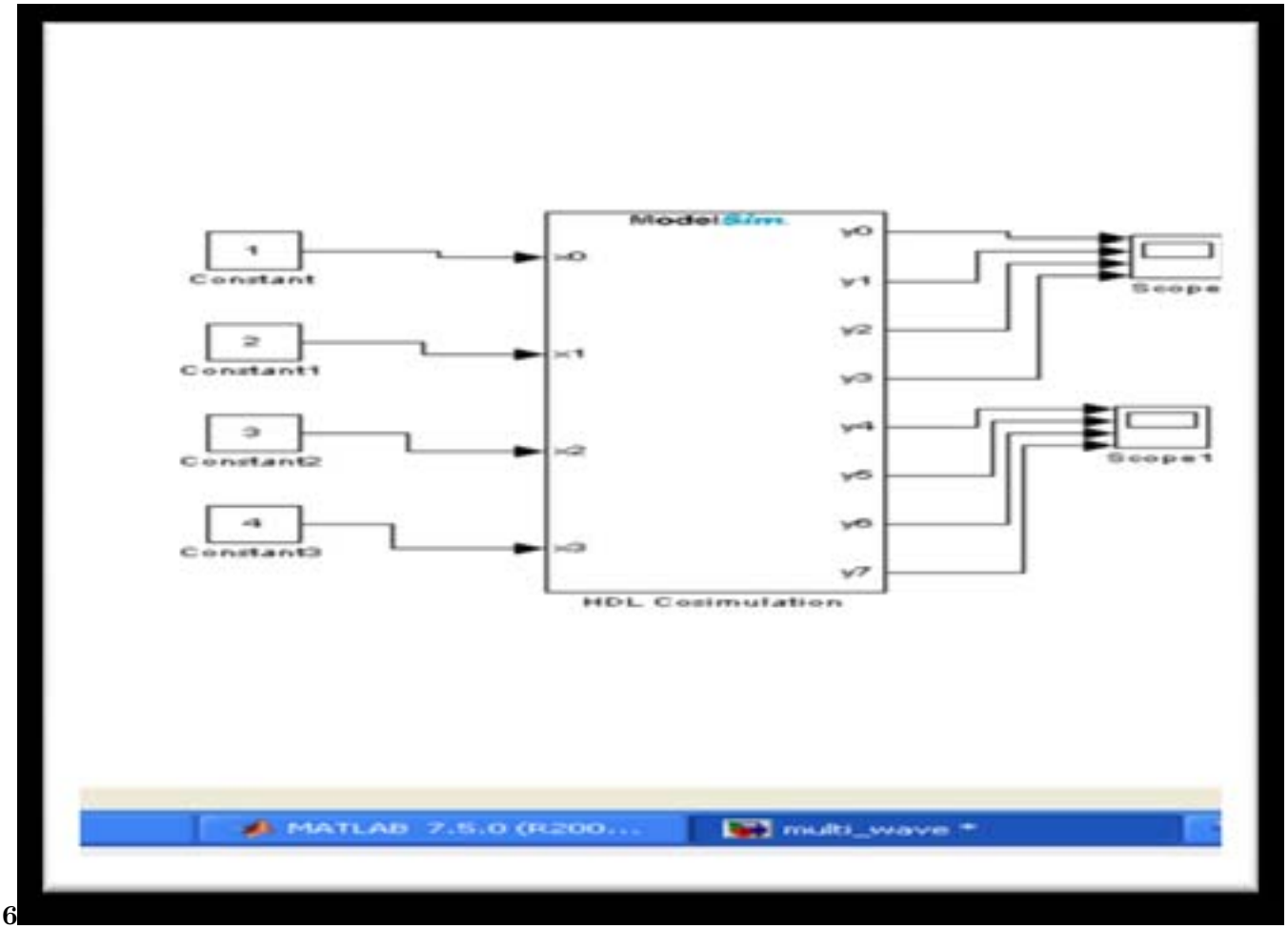
**4**

Figure 9: Figure 4 :




**6**

Figure 10: Figure 6




6

Figure 11: Figure 6 :

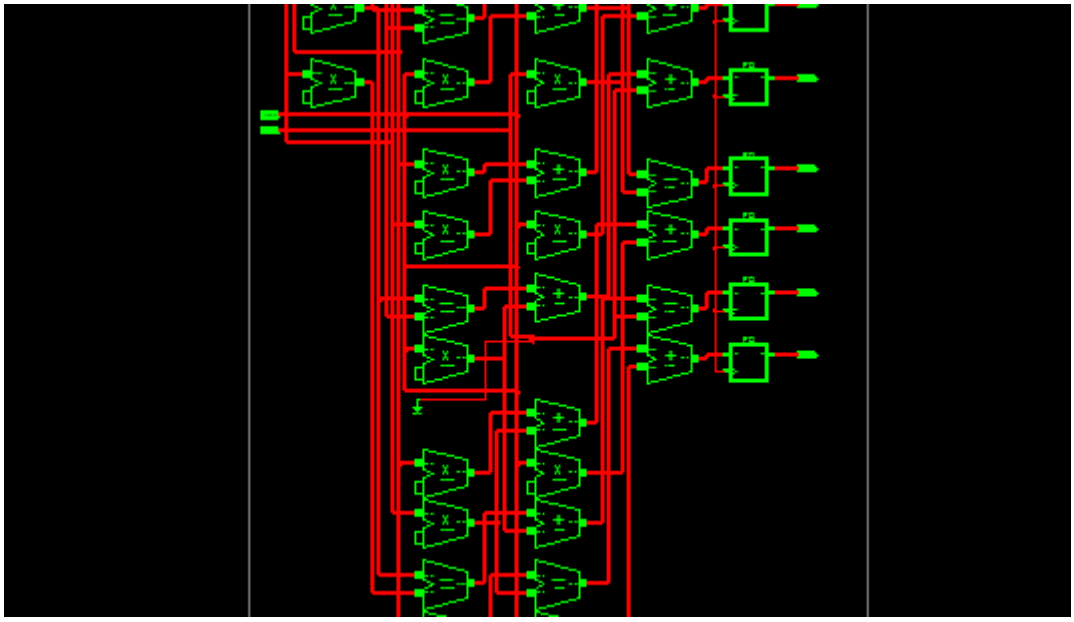


Figure 12:

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