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A TCAD Simulation Study of Cylindrical Gate All Around (CGAA) MOSFETs

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Abstract

Due to aggressive scaling of transistors SCEs has become the limiting factor for further scaling of the conventional MOSFETs. To overcome this limitation a large number of new device architectures have been proposed. One of such device structures is cylindrical gate all around (CGAA) MOSFET that seems to be most suitable to be studied further for different applications point of view. In this paper we report the suitability analysis of CGAA MOSFETs for low voltage, low power and analog applications. We report many interesting findings through 3D TCAD simulations of CGAA MOSFETs.

Index terms— Cylindrical Gate All Around (CGAA) MOSFETs, analog, low voltage, low power, short channel effects (SCEs), 3D TCAD.

1 Introduction

o keep pace with the Moore's law the CMOS transistors has witnessed aggressive scaling in the last decade. Due to this scaling the device sizes has become very small and many secondary effects, widely known as short channel effects (SCEs) and hot carrier effects (HCEs) plays important role in the device characteristics.

In an ever increasing need for higher current drive and better short-channel characteristics, siliconon-insulator MOS transistors are evolving from classical, planar, single-gate devices into three-dimensional devices with multiple-gates (double-, triple-or quadruple-gate devices). Multiple Gate Field Effect Transistors show great promise as an alternative to planar CMOS. They are known for their excellent immunity against SCEs due to better control of the channel by the gates. Several designs depicted in Figure 1 have been proposed including planar, vertical, fin, tri-gate and gate all around that all make use of enhanced gate control due to the action of multiple electrodes surrounding the channel [3]. Volume inversion (full inversion of the silicon film) [4] is the basic phenomenon found in thin film Multi-gate MOSFETs.

Out of these, the multi-gate transistor seems to be very promising due to its larger control on the channel as compared to the conventional MOSFETs. Recently Intel has revealed 22 nm FinFET based processor to be used in next generation highly efficient applications. However, more techniques have to be investigated for even better solution for overcoming the limitation imposed on the conventional CMOS processes. The gate all around (GAA) MOSFETs controls the channel of the transistors from all sides and hence provides better control over the channel than any other configuration. To look into various aspects of this transistor a 3D TCAD simulation has been carried out and compared for the different parameters.

II.

2 Device Structure Generation

The device has been generated using the structure editor of Sentaurus TCAD of Synopsys. The channel region is lightly doped (1.0E+16/cm -3 , Boron) so that there is almost no degradation of mobility due to doping. Gate oxide chosen is silicon dioxide (SiO2) with thickness of 1 nm, to stop the gate tunneling current. The source and drain regions are heavily doped (1.0E+20/cm -3 , Arsenic) and a mid-gap metal gate (work function 4.6 eV)

has been taken of varied gate height. A spacer region has been used between the source and channel region for the purpose of reducing the source/drain effect on the channel. A spacer oxide (SiO2) has been used in between gate and source/drain. The device has been simulated for its DC characteristics (threshold voltage) and analog characteristics (transconductance). A typical GAA MOSFET considered for simulation study is shown in the Figure 2. For comparison of the variation of different device parameters taken is given in Table 1.

3 Results And Discussions

These MOSFETs has been simulated for the suitability of their use at lower operating voltages. This has become important nowadays because of the quest for low power devices for longer battery life. The simulation results obtained from above devices confirms the suitability of these for low voltage applications F ig. 3 : Variation of the Vt1 for different gate lengths and different structures Figure **??** shows the variation of the Vt1 parameter extracted with inspect tool of the Sentaurus TCAD tool. Vt1 is the threshold voltage extracted at a drain current I d =0.1 µA/µm. It can be observed that the Vt1 is lower for large gate metal height and scales down with the gate length. Also Vt1 increases with the increase of the source/drain extension regions and scale downs with the gate length.

Figure **??** shows the variation of the threshold voltage (V th) extracted by using the maximum slope intercept of the I d -V gs characteristics. It varies very similar to the V t1 but there is a sharp reduction in the threshold voltage at lower gate lengths. This is due to the reduction in charge carriers to be controlled by the gate. Due to lower threshold voltages of scaled CGAA MOSFET, it may better suit for the low voltage applications. Figure **??** shows the variation of the output drain resistance of the CGAA MOSFET. Output drain resistance is almost same for different lengths of source/drain spacer region and scales down with the gate length. This is; however, lower for the larger gate metal height.

IV.

4 CONCLUSION

The 3D simulations were carried out for varied range of gate lengths and source/drain extension regions. It has been found that the CGAA MOSFET has very good SCE immunity and is suitable to be used for low voltage low power applications. The transconductance is significantly larger and output resistance is lower at smaller gate lengths which mean it is also suitable for analog applications as well. [1]

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Figure 1: TFig. 1 :

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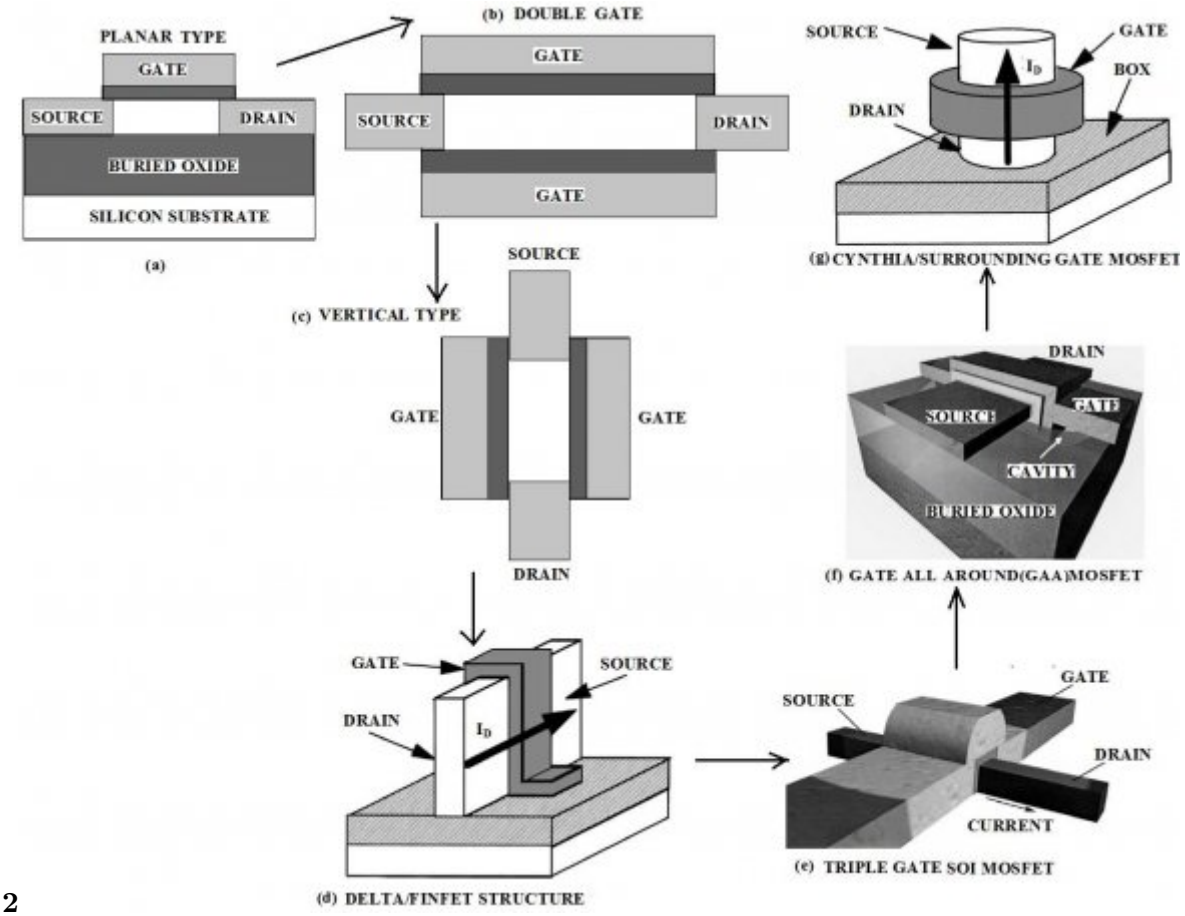

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Figure 2: Fig. 2 :

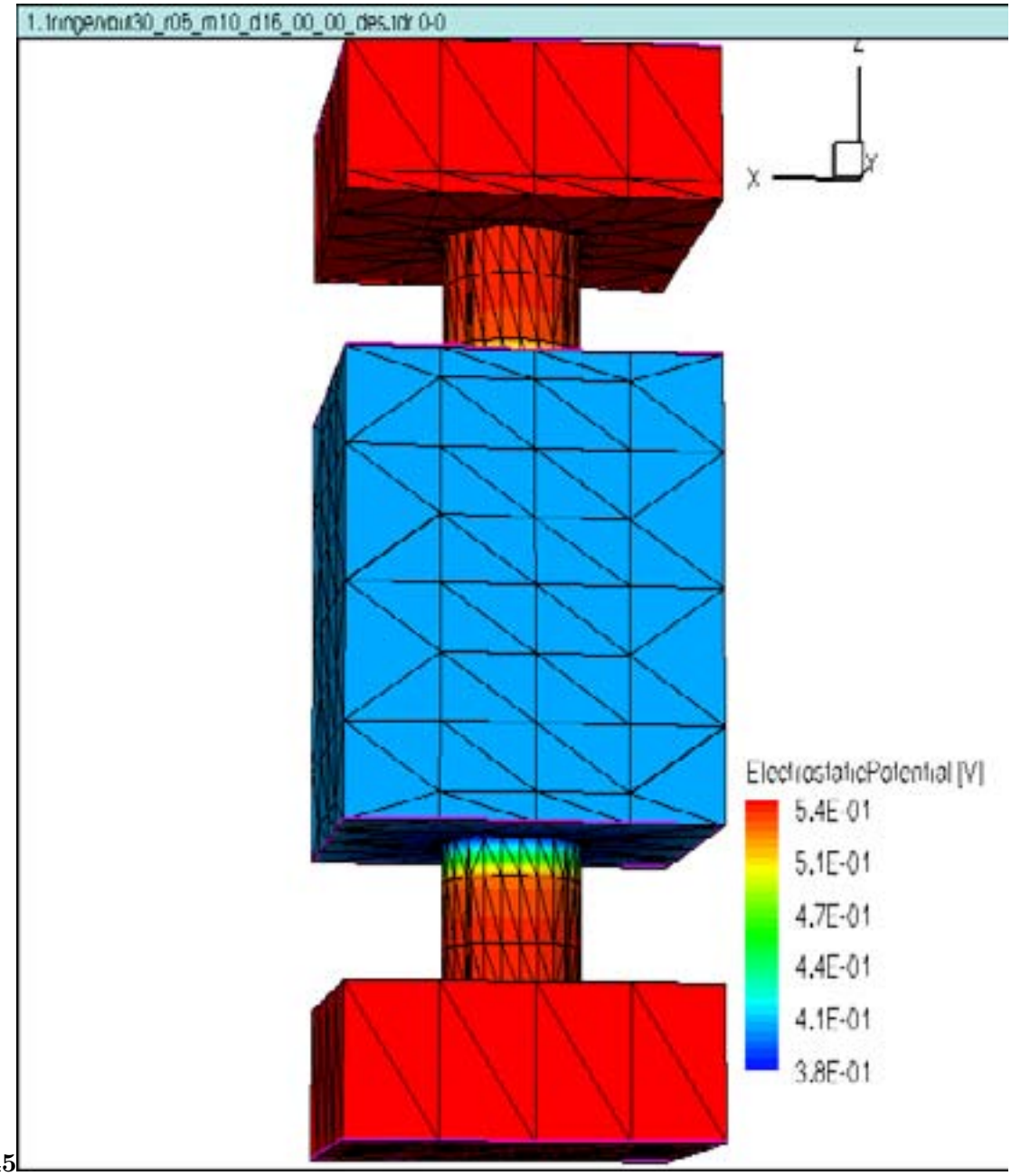

Figure 3: Fig. 4 :Figure 5

1

Structure	Gate length	Source/Drain extension	Gate height (4.6 eV)	Channel radius	Source/Drain doping	Channel doping	Gate Oxide
2 nm gate height	16 nm 30 nm 50 nm	10 nm	2 nm	10 nm	1E+20 (Arsenic)	1E+16 (Boron)	1 nm (SiO_2)
10 nm gate height	16 nm 30 nm 50 nm	10 nm	10 nm	10 nm	1E+20 (Arsenic)	1E+16 (Boron)	1 nm (SiO_2)
22 nm spacer length	16 nm 30 nm 50 nm	22 nm	2 nm	10 nm	1E+20 (Arsenic)	1E+16 (Boron)	1 nm (SiO_2)

[Note: A TCAD Simulation Study of Cylindrical Gate All Around (CGAA) MOSFETs]

Figure 4: Table 1 :

.1 ACKNOWLEDGEMENT

[IEEE Electron Device Letters (1987)] , *IEEE Electron Device Letters* September 1987. 8 p. .

[A TCAD Simulation Study of Cylindrical Gate All Around (CGAA) MOSFETs] *A TCAD Simulation Study of Cylindrical Gate All Around (CGAA) MOSFETs*,

[Balestra et al.] *Double-Gate Silicon-on-Insulator transistor with volume inversion: A new device with greatly enhanced performance*, F Balestra , S Cristoloveanu , M Menachir , J Brini , T Elewa .

[Gupta and Baishya (2012)] 'Modeling and Simulation of Triple Metal Cylindrical Surround Gate MOSFETs for reduced Short Channel Effects'. S K Gupta , S Baishya . *International Journal of Soft Computing and Engineering (IJSCE)* May 2012. 2 (2) p. .

[Colinge ()] 'Multi-gate SOI MOSFETs'. P Colinge . *Microelectronic Engineering* 2007. 84 (9) p. .

[Conti and Turchetti ()] 'On the Short-Channel Theory for MOS Transistor'. Massimo Conti , Claudio Turchetti . *IEEE Transactions on Electron Devices* 1991. 38 (12) p. .

[Gupta et al. ()] 'Simulation and Modeling of Double Material Double Gate Surround Gate (DMDG-SG) MOSFETs'. S K Gupta , Kaushik Guha , S Baishya . *ICGST Journal of Programmable Devices, Circuits, and Systems*, 2012. 12 p. .