PWM Strategies for Multilevel Inverter and DC Link Capacitor Voltage Balancing For an Induction Motor Drive

By Mr. Srinivas Dasam & Dr. BV Sankerram

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PWM Strategies for Multilevel Inverter and DC Link Capacitor Voltage Balancing For an Induction Motor Drive

Mr. Srinivas Dasam[α] & Dr. BV Sankerram[σ]

Abstract - Multilevel PWM techniques are extensions of two-level PWM methods; the multiple levels in these inverters offer extra degrees of freedom and greater possibilities in terms of device utilization and effective switching frequency. Though the SPWM and its variations are popular PWM techniques in multilevel inverters, implementing them in a digital platform is tedious, as the pulse-widths can only be defined by transcendental equations. A dc link capacitor voltage balancing scheme is proposed for an induction motor drive. The motor is fed from with three-level inverters generating a five level output voltage structure. The proposed inverter vector locations exhibit multiplicity in the inverter switching combinations which is suitably exploited to arrive at a capacitor voltage balancing scheme. This allows the use of a single dc link power supply for the combined inverter structure. The lower order harmonic components in the output voltage waveform are eliminated by raising the carrier frequency.

I. Introduction

Three-level inverters have attracted the attention of researchers since their introduction by Nabae et at. [1] in 1981. Though simple and elegant, neutral-clamped circuit topology has a few disadvantages. Neutral point fluctuation is commonly encountered as the capacitors connected to DC-bus carry load currents. Also, there is ambiguity regarding the voltage rating of the semiconductor devices, which are connected to the neutral point. This calls for a conservative selection of devices for reliable operation, which, however, increases cost. Various alternative circuit topologies have been suggested in the literature. H-bridge topology [2], [3] eliminates the problem of neutral fluctuation, but requires three isolated power supplies. Soh and Hyun [4] have suggested an improvisation of the conventional neutral clamped inverter in which a capacitor is connected across the neutral clamping diodes to ensure dynamic balancing of the voltage across the DC bus capacitors. This method alleviates the problem but does not eliminate it. Three-level inversion may also be achieved with two 2-level inverters, driving an open-end winding induction motor from either end [5], [6]. The inverters in this case require isolated power supplies to eliminate the harmonic currents of the triplen order in the individual motor phases Recently, Somasekhare t al. [7] have suggested an open-end winding induction motor drive, which obviates transformer isolation. But the DC bus utilization is slightly lower in this scheme when compared to the schemes proposed by Stemmler and Guggenbach [5] and Shivkumar et al. [6] The DC link capacitors in this circuit do not carry the load currents and hence the voltage fluctuations in the neutral point are absent. Also, the circuit configuration needs two isolated power supplies compared to H-bridge topology, which requires three isolated power supplies to achieve 3-level inversion. However, the power semiconductor switches in one bank (three in number) in one of the inverters of this circuit have to be rated for the full DC link voltage.

a) Proposed 3-level inverter configuration

In the proposed 3-level inverter topology circuit, the cascade connection of two 2-level inverters accomplishes 3-level inversion (Fig. l). The output phases of Inverter 1 are connected to the DC input points of the corresponding phases in Inverter2. Each inverter is powered with an isolated DC power supply, with a voltage of $\sim$j2 (Fig. l) when i) the top switch of that leg in Inverter2 is turned on, and ii) the bottom switch of the corresponding leg in Inverter1 is turned on.
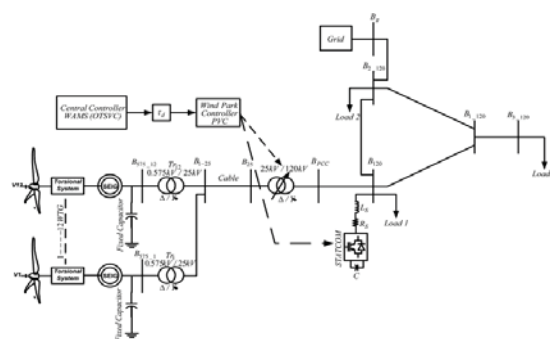

Fig.1 : Cascade connection of two 2-level inverters accomplishes 3-level inversion

Thus, the DC input points of individual phases of Inverter2 may be connected to a DC link voltage of $\sim$j2 by turning on the top or the bottom switch of the corresponding phase leg in Inverter l. Additionally, the pole voltage of a given phase in Inverter2 attains a voltage of zero, if the bottom switch of the

Author α : Assoc. Professor, kits, A. P., India.
E-mail : srinu_vaseee@yahoo.in
Author σ : Professor, jntuh, A. p., India

corresponding leg in Inverter2 is turned on. In this case, the DC input point of that phase for Inverter2 is floating as the top and bottom switches are switched complementarily in any leg in a 2-level inverter. This means that individual inverters are operated with a DC link voltage of 150 V. The motor is run in open loop using the V If control scheme. To demonstrate the working principle of this inverter scheme, space vector, modulation has been employed, which was implemented using look-up table approach. The space vector combinations at each space vector location have been chosen in such a way that both the inverters are switched with only one transition during the subinterval period.

II. Three-Level Inverter Scheme with Common-Mode Voltage Elimination for an Induction Motor Drive

A three-level inverter configuration with common mode voltage elimination is already presented in [10]. Only those switching combinations, which generate zero common mode voltage in the inverter poles, are used to switch the three-level inverters from both sides, thus resulting in zero common mode voltage across the machine phases [10]. Thus, appropriate selection of switching states, of individual three-level inverters, result into the total elimination of alternating common mode voltage from the inverter pole voltages as well as common mode voltages from the phase windings of the induction motor [10]. As the common modes voltages are absent in this scheme, individual three-level inverter structure can be supplied from single dc link as shown in Fig.1. The three-level structure is realized by cascading two conventional two-level inverters, resulting in a simple power bus structure for the proposed power circuit [9], [10]. The unbalance in the dc link capacitor voltages for the proposed open-end winding induction motor drive.

III. Switching Combinations and their Effect on dc Link Capacitor Voltages

As explained in the previous section, the inverter space vector locations have multiple switching combinations of inverter-1 and inverter-2 voltage space vectors (Fig.2). The central voltage location being referred as zero voltage vector (ZV), the voltage vector locations at the periphery of inner hexagon are referred as small voltage vectors (SV), the intermediate voltage vectors on outer periphery are referred as middle voltage vectors (MV), while the largest voltage vectors on outer periphery are referred as large voltage vectors (LV).

a) Back-to-Back Intertie

When interconnecting two diode-clamped multilevel inverter to-gather with a "dc capacitor link," as shown in Fig.2 the left-hand side converter serves as the rectifier for utility interface, and right-hand side converter serves as the inverter to supply the ac load. Each switch remains switching once per fundamental cycle. The result is a well-balanced voltage across each capacitor while maintaining the staircase voltage wave, because the unbalance voltages across each other tend to compensate each other. Such a dc capacitor link is categorized as the "back-to-back intertie." The purpose of the back-to-back intartie is to connect two asynchronous systems. It can be treated as 1) a frequency changer, 2) a phase shifter, or 3) a power flow controller. The power flow between the two systems can be controlled bidirectionally.
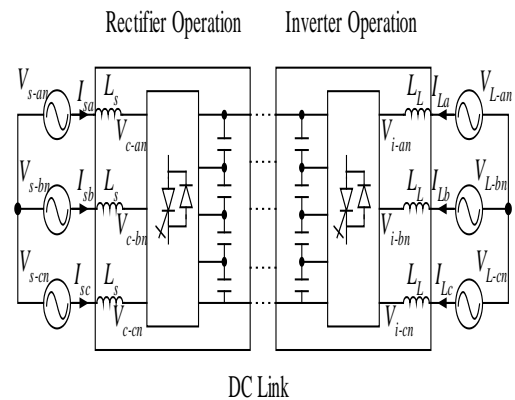

Fig.2 : General Structure of a back-to-back intertie system using two diode-clamped multilevel inverter.

b) Utility compatible Adjustable Speed Drives

An ideal utility compatible system requires unity power factor, negligible harmonics, no EMI, and high efficiency. By extending the application of the back-to-back intertie, the multilevel inverter can be used for a utility compatible adjustable speed drive (ASD) with the input from the utility constant frequency ac source and the output to the variable frequency ac load. The major differences, when using the same structure for ASD's and for back-to-back intertie, is the control design and size of capacitor. Because the ASD need to operate at different frequencies, the dc link capacitor needs to be well-sized to avoid a large voltage swing under dynamic condition.

c) Converter Topology

Figure.3 shows the two leg FCMLI topology for obtaining the different levels of voltage across the load. Although the dc source voltage sources are shown to be two, it is basically the same source. Initial values of capacitor voltages are considered to be the same and are given by a ratio of the dc source voltage V_{dc}. Switches S & S' on each leg are complementary to each other. These switching states are considered as depicted in Table
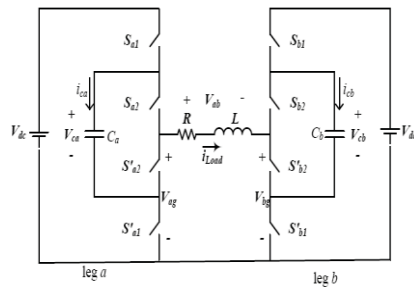
Fig.3 : FCMLI topology

Table1 : Switching states to determine state indicator

S1	S2	State
ON	ON	3
ON	OFF	2
OFF	ON	1
OFF	OFF	0

Voltage V_{bg} on *leg b* is 180 degrees out of phase with the voltage V_{ag} on leg a. Hence, the resultant voltage V_{ab} across the load is a multi level stair case waveform as shown in below figure
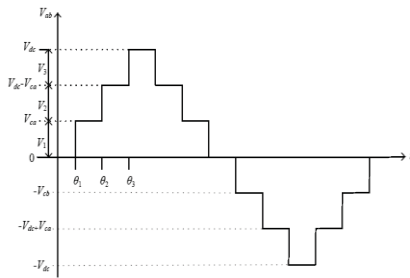

Fig.4 : Seven-level staircase voltage V_{ab}

Now that different voltage levels are obtained, the capacitor currents in terms of the load current can be tabulated as in Table2.

Table2 : Output voltages and capacitor currents

State	V_{ag}	V_{bg}	i_{ca}	i_{cb}
3	V_{dc}	$-V_{dc}$	0	0
2	$V_{dc}-V_{ca}$	$-V_{dc}+V_{cb}$	i_{Load}	$-i_{Load}$
1	V_{ca}	$-V_{cb}$	$-i_{Load}$	i_{Load}
0	0	0	0	0

$$V_{ab}(t) = \sum_{n=1,3,5}^{\infty} \frac{4}{n\pi} (V_1 Cosn\theta_1 + V_2 Cosn\theta_2 + V_3 Cosn\theta_3) Sin(n\omega t)$$

Where 'n' is the order of the harmonic and 'w' is the angular frequency. The voltage levels of the dc

sources are equal and labeled to be V_{dc}. Also, the voltage of the capacitors is same and intended to be regulated at the modulation index in general is defined as:

Modulation Index M: V_m/V_{dc}

Where, *Vm* is the magnitude of the fundamental component of the output voltage.

Theta Calculations

Considering only the fundamental component and eliminating the 3rd and the 5th order harmonics, the following equations are used to calculate $\theta 1$, $\theta 2$, and $\theta 3$ for different values of the modulation index *'M'*. Here *'p'* is considered to be three.

$$V_{dc} * M = \frac{4}{\pi} \frac{V_{dc}}{3} (Cos\theta_1 + Cos\theta_2 + Cos\theta_3)$$

$$\frac{4}{3\pi} \frac{V_{dc}}{3} (Cos3\theta_1 + Cos3\theta_2 + Cos3\theta_3) = 0$$

$$\frac{4}{5\pi} \frac{V_{dc}}{3} (Cos5\theta_1 + Cos5\theta_2 + Cos5\theta_3) = 0$$

IV. Proposed Scheme for dc Link Capacitor Voltage Balancing

The inverter voltage vectors belonging to ZV, NSV, MV, and LV groups can be effectively used to maintain the voltage balance across the dc link capacitors. The input to the voltage-balancing scheme can be either the difference in the capacitor voltages, or the load current drawn from middle node, as the voltage unbalance can be determined. Each inverter voltage vector locations from groups NSV and MV have two switching combinations.

a) *Hysteresis Controller Based Closed Loop DC Link Balancing Scheme*

With the voltage-balancing scheme implemented in the above manner, a gradual deviation in the dc link voltages is observed. The possible reasons for this are, the use of the asynchronous PWM, the unequal time durations of the MV and NSV inverter vectors in consecutive switching intervals, unbalanced load currents etc. As discussed in the previous section, the switching combinations belonging to USV and LSV group can charge the lower and the upper capacitor, respectively. Thus, if the difference in the two capacitors of the dc link is monitored, the switching combinations from USV or LSV groups can be selected for inverter switching, which will bring back the deviation in the capacitor voltages to zero. This is done using a hysteresis controller. The input to the controller is the difference between the dc link capacitor voltages; the normal control band is set depending upon the maximum deviation that can be allowed in the dc link voltages. The controller outputs, 0 if the is within the

normal band, 1 if is greater than the control band and 1 if the is less than the control band. The schematic of the closed loop voltage balancing scheme is shown in Fig. 5. The output of the controller along with "SEQ" signal is used to select the appropriate value of the signal "state," which is given to a digital logic.
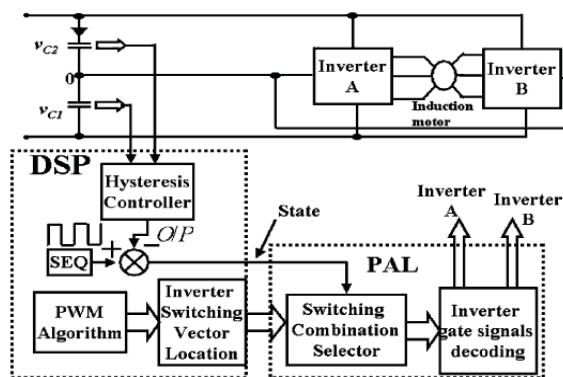

Fig5 : Hysteresis Controller Based Closed Loop DC Link Balancing Scheme

V. Dc link Capacitor Voltage Balancing During Inverter Operation in Over-Modulation and 12-Step Mode

It is to be noted that only the inverter vectors belonging to USV or LSV groups have strong capability to charge/discharge the dc link capacitors. During motor operation in over-modulation range, the inverter vectors belonging to MV and LV groups are switched for maximum duration, in a switching interval, as compared to the inverter voltage vectors belonging to SV group. The extreme case is the 12-step operation, wherein the inverter vectors from the SV group are not switched at all. Under steady state and dynamic operation, in over-modulation, the controller can maintain the capacitor voltage balance by switching MV and LV vectors. The SV vectors are switched for less time duration, the time required to bring back the capacitor voltages to the balanced state, is more during over modulation operation. In extreme case, the inverter vectors from SV group are not switched in 12-step mode. If there is mismatch in the capacitor voltages due to the asynchronous PWM or asymmetric loads, the capacitor voltages are balanced by reducing the modulation index momentarily. This allows the switching of the inverter vectors belonging to SV group and the dc link capacitor voltages are brought back to the balanced state as shown in the simulation results of Fig. 6. Thus while, USV vectors were having charging effect on C1 and discharging effect on C2 in motoring mode, they have discharging effect on C1 and charging effect on C2 in regenerative mode. Thus, the controllers need to sense the power direction, to suitably switch the switching combinations belonging to the vector group,

which will reduce the error in the dc link capacitor voltages. Determining the operating mode (i.e., motoring/generating) requires current sensing. The determination of current direction for currents drawn from dc link involves hardware sensors or can be judged from direction of power flow
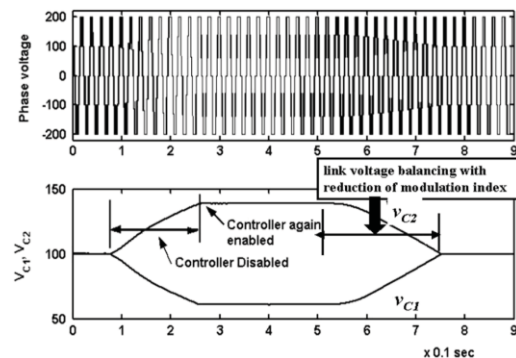

Fig. 6 : DC link balancing with momentary reduction in modulation index.

If the motor is operating in regenerative mode, the actions taken by the controller will worsen the voltage balance. An additional hysteresis comparator is used to sense this change. The control band of this comparator is placed above the control band of the main inner comparators. Thus, with motor operating in regenerative mode, the outer comparators of hysteresis controller gets activated if the dc link voltage unbalance exceeds the outer comparator settings and the switching combinations belonging to the USV or LSV vector group, which reduces the voltage unbalance, are selected for inverter switching. As shown in simulation results of Fig.6, the motor is initially operating in motoring mode and the load torque is made negative thus driving the motor in regenerative mode. The voltage balancing controller is disabled which will cause rapid growth in dc link unbalance. When the voltage-balancing scheme is enabled again, the capacitor voltages are brought back to the normal value, similar to the case with motor operating in motoring mode.
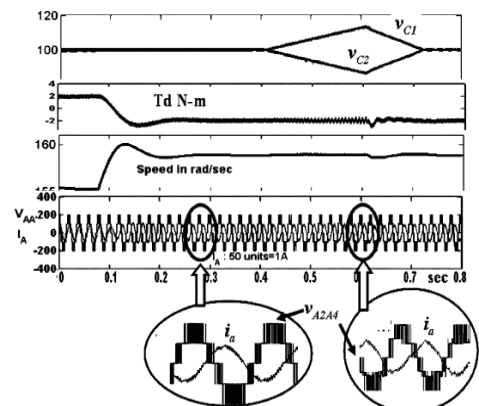

Fig.7 : Capacitor voltages when the closed loop dc link voltage balancing scheme is turned off in regenerating mode

VI. SIMULATION RESULTS

The performance of these methods is studied through Matlab simulation.. It is clear that there is a reduction in THD.
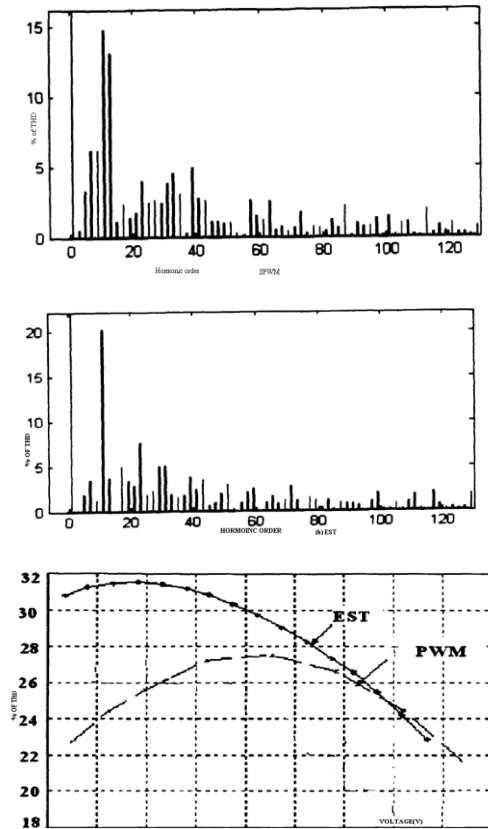

Fig.8a,b,c : Capacitor voltages for the **closed loop dc** link voltage

The three-level structure is realized by cascading the conventional two two-**level inv**erters, resulting into simple power bus structure for the proposed scheme. Thus, the proposed inverter structure does not require any clamping diodes which are required in NPC inverter topology. The proposed scheme has more multiplicity in the inverter voltage vector locations as compared to conventional single inverter fed drive which are effectively used to balance the dc link capacitor voltages without disturbing the SVPWM modulation. Thus, a single front-end rectifier of rating nearly half to that of a conventional two-level inverter can be used, with two capacitors for splitting the dc link voltage. The proposed capacitor voltage balancing scheme is based on altering the switching combinations of the inverter voltage vectors, having exactly opposite affect on the capacitor voltages, for consecutive sampling durations. A simple closed loop hysteresis controller is used to balance the dc link capacitor voltages throughout the modulation range of the drive. With these values of firing angles, the capacitor voltages, the output voltage and the load

current at different values of power factor were observed under constant power operation of 200 W by varying the load, using MATLAB Simulink. The values of the load resistance and inductance under different power factor conditions and modulation indices are given in following Tables Load resistance (R) and inductance (L) at different power factors when M=0.7

Table3 : Load resistance (R) and inductance (L) at different power factors when M=0.7

Power Factor	R (Ω)	L (mH)
0.3	6.1224	3.09
0.4	10.884	3.969
0.5	17.006	4.68
0.6	24.48	5.196
0.7	33.33	5.412
0.8	43.537	5.196
0.9	55.102	4.24

These values are found from the power calculations and the power factor formulae given by,

$$P = \frac{V_m^2}{R^2 + L^2\omega^2}\frac{R}{2} = 200$$

$$tan\Phi = \frac{L\omega}{R}$$

where, *'P'* is the output power, „ " is the power factor angle and *'V_m'* is the magnitude of the fundamental component of the output voltage obtained from the above equation. The fundamental frequency is considered to be 1 kHz. The simulation results showing the capacitor voltages, load current and the output voltage for M=0.7 and M=0.877 at a power factor of 0.8 are shown in Figs.9 to 14 respectively. Capacitor voltage V_{cb} is similar to that of V_{ca}, voltage across the capacitor *Ca* for both the modulation indices.
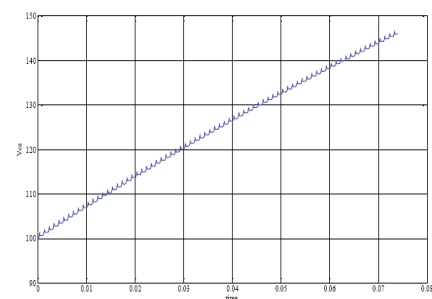

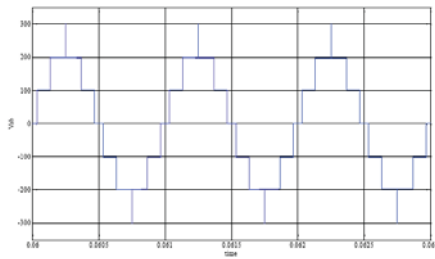*Fig. 9 :* Capacitor voltage *Vca* at *M*=0.7 & PF=0.8

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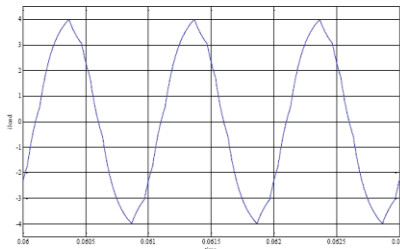*Fig. 10 :* Output Voltage *Vab* at *M*=0.7 & PF=0.8
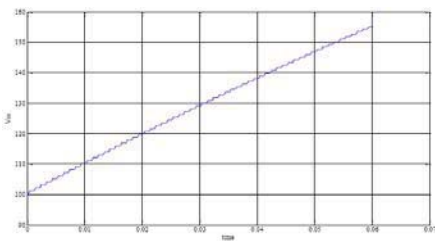

Fig. 11 : Load current *iload* at *M*=0.7 & PF=0.8

Fig.12 : Capacitor voltage *Vca* at *M*=0.877 & PF=0.8
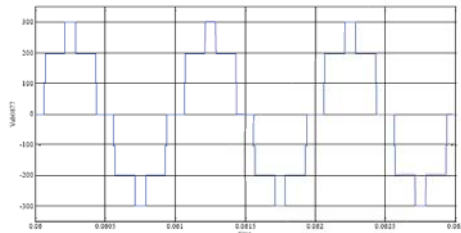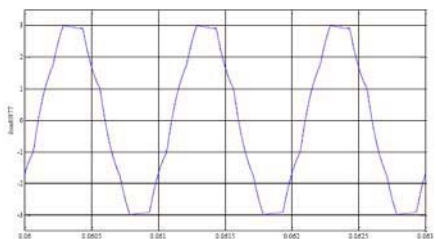

Fig. 13 : Output Voltage *Vab* at *M*=0.877 & PF=0.8

Fig. 14 : Load current *iload* at *M*=0.877 & PF=0.8

Fig. 15 : Output voltage *Vab* at *M*=0.7 & PF=0.7

Fig.16 : Load current *iload* at *M*=0.7 & PF=0.7
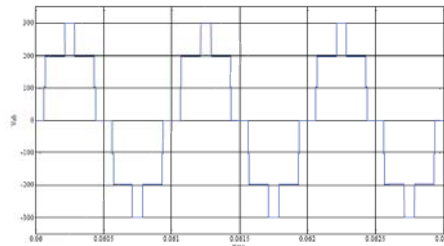
Fig.17 : Output voltage *Vab* at *M*=0.877 & PF=0.7
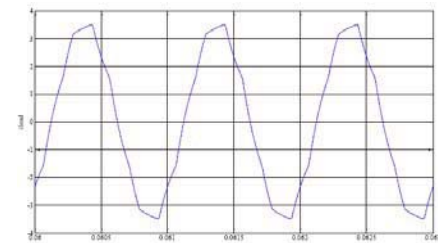
Fig.18 : Load current *iload* at *M*=0.877 & PF=0.7

Next aspect that was looked into was the effect of power factor on output voltage and load current. Figures15 to 18 shows the same at power factor 0.7 for two different modulation indices *M*=0.7 and *M*=0.877.
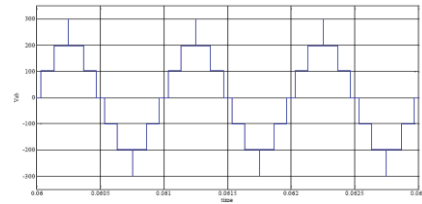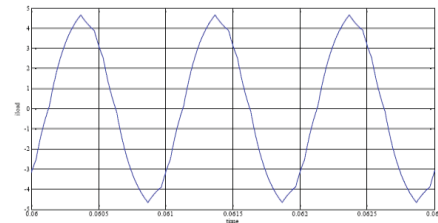
References Références Referencias

1. A. Nabae, I. Takahashi, and H. Akagi, "A new neutral point clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

2. H. L. Liu, N. S. Choi, and G. H. Cho, "DSP based space vector PWM for three-level inverter with DC-link voltage balancing," in *Proc. IEEE IECON Conf.*, 1991, pp. 197–203.

3. R. S. Kanchan, P. N. Tekwani, M. R. Baiju, K. Gopakumar, and A. Pittet, "Three-level inverter configuration with common mode elimination for an induction motor drive," *Proc. Inst. Elect. Eng.*, vol. 152, no. 2, pp. 261–270, Mar. 2005.

4. G. Sinha and T. A. Lipo, "A four level inverter based drive with a passive front end," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 285–294, Mar. 2000.

5. R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, "Space vector PWM signal generation for multi-level inverters using only the sampled amplitudes of reference phase voltages," in *Proc. Inst. Elect. Eng.*, Mar. 2005, vol. 152, no. 2, pp. 297–309.

6. R. S. Kanchan,P. N. Tekwani,K. Gopakumar*, "*Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC Link Capacitor Voltage Balancing for an Open-End" Winding Induction Motor Drive IEEE transactions on power electronics, vol. 21, no. 6, november 2006

7. S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Proc. IEEE IAS Conf.*, 1993, pp. 965–970.

8. Y. Lee, B. Suh, and D. Hyun, "A novel PWM scheme for a three-level voltage source inverter with GTO Thyristors," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 260–268, Mar./Apr. 1996.

9. A. Newton and M. Sumner, "Neutral point control for Multi-level inverters: Theory, design and operational limitations," in *Proc. IEEE IAS Conf.*, New Orleans, LA, Oct. 5–9, 1997, pp. 1336–1343.

10. N. Celanovic and D. Boroyevich, "A comprehensive study of neutral point voltage balancing problem in three-level neutral point clamped voltage source PWM inverters," *IEEE Trans Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

11. M. C. Klabunde, Y. Zhao, and T. A. Lipo, "Current control of a three level rectifier inverter drive system," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 57–65, Jan. 1996.

12. R. Rojas, T. Ohnishi, and T. Suzuki, "An improved voltage vector control method for neutral point clamped inverters," *IEEE Trans Power Electron.*, vol. 10, no. 6, pp. 666–672, Nov. 1995.

13. M. R. Baiju, K. K. Mohapatra, V. T. Somasekhar, K. Gopakumar, and L. Umanand, "A five-level inverter voltage space phasor generation for open-end winding induction motor drive," *Proc. Inst. Elect. Eng.*, vol.150, no. 5, pp. 531–538, Sep. 2003.

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