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Modeling of Dc Link Capacitor Voltage Balance in 3-Level Inverter Using Space Vector Modulation Technique

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Abstract

A new simplified space vector PWM method for a three-level inverter is proposed in this paper. The three level inverter has a large number of switching states compared to a two-level inverter. In the proposed scheme, three-level space vector PWM inverter is easily implemented than as conventional two-level space vector PWM inverter. This paper presents a novel DC link balancing scheme for a back-to-back system with three-level diode clamped topologies. The proposed algorithm is improvement of the variable switching frequency control strategy formerly introduced with the three-level back-to-back system and it relays on measurement of adjacent capacitor voltages which provide information about the potential variation in consecutive nodes of the three-level DC link network, Therefore, the proposed method can also be applied to multilevel inverters. In this work, a three-level inverter using space vector modulation strategy has been modeled and simulated.

Index terms— Multi level Inverter, voltage balance, switching states, Dc-link, SVM, power factor

ecently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them [1][2]. The output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion. In recent years, beside multilevel inverters various pulse width modulation (PWM) techniques have been also developed. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently. This technique results in higher magnitude of fundamental output voltage available as compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states. One of the advantages of multilevel inverters is that the voltage stress on each switching device is reduced. In addition, multilevel waveforms feature have less harmonic content compared to two level waveforms operating at the same switching frequency. In this paper, modeling and simulation of a multilevel inverter using cascaded inverters with separated DC sources have been performed with R-L load using Simulink/ MATLAB package program. In multilevel inverters, it is easy to reach high voltage levels in high power applications with lower harmonic distortion and switching frequency, which is very difficult to get this performance with conventional two level inverters. Minimum level number of a multilevel inverter is three and three-level inverter structure is chosen in this work.

1 a) multilevel concept

This paragraph has the aim to introduce to the general principle of multilevel behavior. Considering Figure 1.), the voltage output of a 3-level inverter leg can assume three values: 0 , E or 2E . In Figure 1.1c) a generalized n-level inverter leg is presented. Even in this circuit, the semiconductor switches have been substituted with an ideal switch which can provide n different voltage levels to the output. In this short explanation some simplifications have been introduced. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice there are no such limits, then the voltage levels can be different. This introduces a further possibility which can be useful in multiphase inverters, as it will be shown in the following. A three-phase

inverter composed by n-level legs will be considered for the analysis. Obviously the number of phase-to-neutral voltage output levels is n. The number k of the line-toline voltage levels is given byk = 2n 1**(1)**

Considering a star connected load, the number p of phase voltage levels is given byp = 2k 1**(2)**

For example, considering a 5-level inverter leg, it is possible to obtain 9 line-to-line voltage level (3 negative levels, 3 positive levels and 0) and 17 phase voltage levels. Higher is the number of levels better is the quality of output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic distortion of the generated voltage, but a more complex control system is required, with the respect to the 3-level inverter. 3-level diode-clamped leg is shown it is easy to extend the scheme to a generic n-level configuration. The DC bus voltage is split in two and four equal steps respectively by capacitor banks. In this way, no extra DC sources are needed with respect to the standard 2-level inverter. The voltage between two switches is clamped through the diodes in the middle of the structure, called clamping diodes. Anyway, to better understand how a diode-clamped works, it is preferred to use series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor. For a generic n-level diodeclamped the diode reverse voltage is given by (3)Vr = E/n-1**(3)**

In 3-level diode-clamped it is 2

Vr = E/2 this voltage drop is also the reverse voltage each switch has to block. Now it is clear that increasing the levels means a reduction of the stress over the components, considering the same DC bus voltage. Unfortunately, higher is the number of levels higher is the number of components. Increasing of one level involve the use of one capacitor, two switches and a lot of diodes more. In fact the number of clamping diodes used in diode-clamped is related to the Focusing the attention to the 3-level leg, it is possible to find the relationship between the state of the switches and the output voltage AO V. Before all consideration, a right switches configuration must avoid every kind of shortcut. So, it is simple to understand that all the switches cannot be simultaneously turned on.

Table1 : The relationship between the state of the switches and the output voltage Switches stateT 1 T 2 T 1 1 T 1 2 V AO 1 1 0 0 E 0 1 1 0 E/2 0 0 1 1 0 1 0 0 1 Undefined

Fig2 : Three-level Capacitor-Clamped Multilevel inverter There are also other dangerous configurations, but they can be avoided switching 1 T and 1 T in a complementary way. The same has to happen for 2 T and 2 T . Considering these conditions there are only four possible configurations a 3-level diode-clamped leg can assume and they are shown in Table **??** with the agreement to identify switches on-state with 1 and off state with 0. Not all the four configuration leads to a proper leg output voltage, because when 1 T in on and 2 T is off there is no defined path for the load current because whether 2 T or 1 T are not conducting, so the current flows throughout the free-willing diodes and the output voltage de pendson it. As it is possible to see from Table1. There are no intra-phase redundant states in 3-level diode-clamped.

A schematic drawing of a multilevel inverter using cascaded inverters with separated DC sources is shown in Fig. **??** The principle of SVPWM method is that the command voltage vector is approximately calculated by using three adjacent vectors. The duration of each voltage vectors obtained by vector calculations; where V1, V2, and V3 are vectors that define the triangle region in which V* is located. T1, T2 and T3 are the corresponding vector durations and Ts is the sampling time. In a three-level inverter similar to a two-level inverter, each space vector diagram is divided into 6 sectors. For simplicity here only the switching patterns for Sector A will be defined so that calculation technique for the other sectors will be similar. Sector A is divided into 4 regions as shown in Fig. 3 where all the possible switching states for each region are given as well. SVPWM for three-level inverters can be implemented by considering the following steps; Voltage unbalance problem appears as the result of non-uniform switching of the semi-conductors from bottom and upper inverter's groups. Potentials difference on capacitors produce current in zero -point of the inverter (point between condensers of the bottom and upper group), which from one side causes supercharging one of the capacitances and from second unloading the other one (this phenomena takes place, when inverter's zero -point is separated from source neutral line). During following cycles of modulation, voltages on capacitors attain different levels in result of that compensated current is not shaped correctly. One from methods of assurance of stabilization is interference in switching strategy of the semiconductors [5]. One can reach this adding suitable constant component to reference current for every from three phases separately (this does not cause changes on effective exit voltages and currents of the inverter). This suitable constant component one can receive from measured voltages difference UC1 and UC2 on each capacitor. Second method of voltage stabilization is addition the same constant component to two triangular courses (Fig. 3.). This gives finally the same effect but permits to obtain better formation of compensating currents. Fig7 gives simulation result for selective harmonic elimination method where for eliminating 3 rd and 5 th harmonic, switching angles are selected as 3 = 12 and 5 = 48 as discussed in 2.4 section. FFT for this method is given Fig. **??** In SPWM method of modulation for multilevel inverter numbers of carriers are used. Arrangements of these carriers come with different variants as explain in 8 which calculate exact instant of crossing of reference sine waveform with carrier signal and modify sampled value of reference signal based on this information to achieve performance same as that with natural SPWM. Results obtain from MATLAB simulations validate the proposed scheme which give better performance of proposed scheme over the other scheme on the basis of output phase delay and output THD. The proposed control algorithm used in the three level inverter can be easily applied to multilevel inverters. It has been shown that high quality waveforms at the output of the multilevel inverter can be obtained even with 1 kHz of low switching frequency.

1

Figure 1: Fig. 1 :

I.

Figure 2:

3 I

Figure 3: Fig. 3 :

1 NTRODUCTION

Figure 4: 1 .

4 N

Figure 5: Fig3 4 .

3345 II.

Figure 6: 3 .Table 3 :Fig. 4 :Fig. 5 :

6 A

Figure 7: Fig. 6 :

Figure 8: Fig. 7 :

Figure 9: Fig. 9 Fig. 8 :

Figure 10: Fig9

Figure 11: Fig. 9 :

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