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MTCMOS Design Methodologies and Charge Recycling Process

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Abstract - MTCMOS (Multi Threshold CMOS) technology provides a solution to the high performance and low power design requirements of modern designs. Low Vth and high Vth transistors are used in MTCMOS technology. Low Vth transistors are used to implement the desired functions. High Vth transistors are used to cut off the leakage current. The MTCMOS circuits ,however suffer from high energy overhead during the transitions between the active and stand by modes In this paper we (i) propose a new special flip flop which keeps a valid data during the sleep mode, (ii) develop a methodology which takes in to account the new design issues related to the MTCMOS technology. (iii).propose two adaptive MTCMOS schemes to address the growing leakage and delay spreads found in modern high performance designs. (IV) Propose a technique to lower the energy overhead during the transitions between the active and standby modes. The charge stored at the virtual lines is recycled during the active-to-sleep-to-active mode transitions with the proposed technique.

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MTCMOS Design Methodologies and Charge Recycling Process

P.Sreenivasulu [α], Krishnna veni [σ] & Dr. K.Srinivasa Rao [ρ]

Abstract - **MTCMOS (Multi Threshold CMOS) technology provides a solution to the high performance and low power design requirements of modern designs. Low V_{th} and high V_{th} transistors are used in MTCMOS technology. Low V_{th} transistors are used to implement the desired functions. High V_{th} transistors are used to cut off the leakage current. The MTCMOS circuits ,however suffer from high energy overhead during the transitions between the active and stand by modes In this paper we (i) propose a new special flip flop which keeps a valid data during the sleep mode, (ii) develop a methodology which takes in to account the new design issues related to the MTCMOS technology. (iii).propose two adaptive MTCMOS schemes to address the growing leakage and delay spreads found in modern high performance designs. (IV) Propose a technique to lower the energy overhead during the transitions between the active and standby modes. The charge stored at the virtual lines is recycled during the active-to-sleep-to-active mode transitions with the proposed technique.**

Keywords : MTCMOS, CPFF, energy recycling, gated power, gated ground, sleep switch, sub threshold leakage.

I. Introduction

In digital convergence era, Multi threshold CMOS is an important technology that provides high performance and low power operations by using both high and low threshold voltage transistors. MTCMOS technology is a very efficient technology for low power and high performance. However, MTCMOS has a serious problem that the stored data of latches and flip flops in logic blocks cannot be preserved when the power supply is turned off (sleep mode). Therefore extra circuits are provided for holding the stored data. This will effect the performance, area and the leakage current of the logic circuits in the sleep mode cannot be sufficiently suppressed. To avoid such undesirable leakage, Variable Threshold CMOS has been reported. Adaptive MTCMOS by using variable footer length is used for dynamic leakage and frequency control which was discussed in section 3.

A popular low leakage circuit technique is the multi threshold Voltage CMOS (MTCMOS). MTCMOS circuits selectively connect/disconnect the low threshold voltage (low-Vt) logic gates to/from the power supply or the ground via active/cut-off high threshold voltage (high-Vt) sleep transistors. This technique is also known as "power gating". The power gating technique can be applied as either gated-ground or gated-VDD, as shown in fig 1.

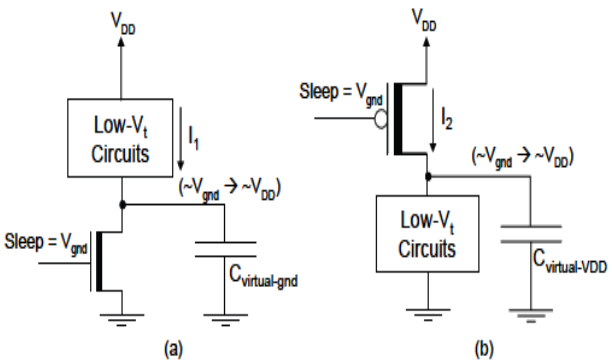

Fig.1 : MTCMOS circuits during the energy consuming mode transitions (a) Gated-ground circuit during the active-to-sleep mode transition. (b) Gated-V_{DD} circuits during the sleep-to-active mode transition. High V_t transistors are represented with a thick line in the channel region.

The leakage current produced by an MTCMOS circuit is significantly reduced by turning off the high-Vt sleep transistors in the standby mode. However, the active-to-sleep-to-active mode transitions consume a significant amount of additional energy in the conventional MTCMOS circuits. The energy dissipation occurs while charging and discharging the parasitic capacitances of the virtual lines and the sleep transistors. The virtual power and ground lines have high capacitance due to the wire parasitics, the large number of transistors sharing a common sleep transistor, and the decoupling capacitors attached to these supply rails for voltage stabilization against bouncing. Furthermore, the sleep transistors are typically large in size for satisfying the performance requirement, thereby further increasing the parasitic capacitance of the virtual lines. The energy consumed during the mode transitions is, therefore, significant in the standard MTCMOS circuits. In this paper, a new charge recycling MTCMOS circuit is proposed for low energy switching between the active and idle modes of operation.

This paper is organised as follows. Section 2 introduces MTCMOS design issues like the data preserving flip flop, the short circuit current due to

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floating inputs. Section 3 introduces adaptive MTCMOS by using variable footer strength for dynamic leakage and frequency control. Section 4 introduces the charge recycling MTCMOS circuit, Conclusions are offered in section 5.

II. Preliminaries

a) The principles of the MTCMOS

The MTCMOS circuit technology can achieve a lower threshold voltage, and therefore higher performance as well as smaller standby leakage current. Basic circuit scheme of MTCMOS is shown in fig 2.

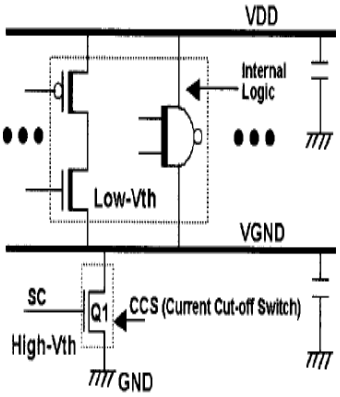

Fig 2 : Schematic Diagram of MTCMOS

The functional logic gates are implemented by using low V_{th} transistors that are powered by the supply line (VDD). A VGND is connected to the real ground line (GND) through a high Vth transistor switch Q1. MTCMOS designs have two operating modes, active and sleep. In sleep modes SC goes to low, and Q1 is turned off. In this state, the leakage current flows to GND through Q1. Due to its low leakage characteristic, the leakage current from the low V_{th} logic gates is almost completely suppressed. The high V_{th} transistor, Q1 acts as a switch that cuts off the leakage current from logic gates in sleep mode. Hence, it can be called as current cut off switch (CCS) The MTCMOS suffer from ground bounce which will decrease the performance or mal function. In order to avoid this channel width is increased but it increases the area and leakage current.

b) MTCMOS Design Issues

i. *Special cells for MTCMOS Design*

a. Complementary Flip Flop (CPFF)

MTCMOS is a very effective scheme that uses high V_{th} low leakage transistors to switch on and off the power supplies to low V_{th}, high speed logic blocks. However due to the lack of data preserve ability of standard latches and flip flops, extra circuits must be provided. These will degrade the performance, power and the area. The fig 3 gives the MTCMOS data preserving complimentary pass transistor flip flop.

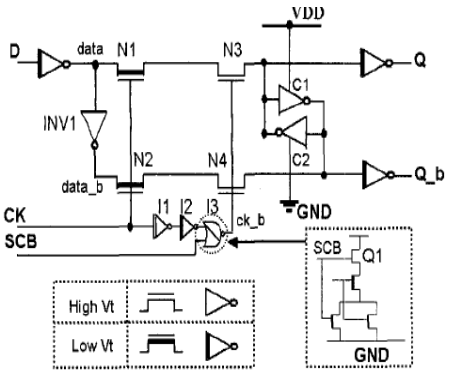

Fig 3 : Complimentary Pass transistor Flip Flop(CPFF)

CPFF operates as follows:

Clock 'low': Since N1 and N2 are turned off and N3 and N4 are turned on, the static latch C1-2 holds the previous state. The new state on the complimentary inputs to the latch, **data** and **data_b** should be ready for sampling.

Clock 'High': At the rising edge of the clock, N1 and N2 are turned on while N3 and N4 stay on for a short interval that is determined by the delay of the inverter chain .During this interval data and data_b are passed through N1, N3 and N2, N4 respectively, and sampled in to the latch. After the short sampling interval, N3 and N4 are turned off, and Q and Q_b are decoupled from the data input.

Sleep mode: In the sleep mode SCB goes high, ck_b becomes low, and high Vth NMOS pass transistors, N3-4 are turned off so that the stored in C1-2 can be retained. At the transition from sleep mode to the active mode, SCB is set to low a little later than the power up. This delay prevents the destruction of data on the latch, C1-2 by delaying the turn on of N3-4 until the input data becomes valid.

c) Floating Input Induced Short-Circuit Current

Some of IPs like processors, memories may not be implemented by MTCMOS technology. These non-MTCMOS are directly powered by VDD and GND, and therefore vigilant even in the sleep mode. However, since the output nodes of all MTCMOS gates get floating as VGND gets floating in the sleep mode, the floating inputs to the vigilant IPs can cause very large short circuit current that flows from VDD to GND as shown in fig.4.

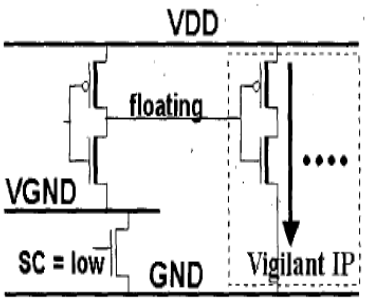

Fig .4 : Floating Input Induced Short-Circuit Current

To eliminate this leakage current, we insert a data holding circuit that is composed of a tri state buffer and a level holder at the output port of an MTCMOS logic gate which is the input to vigilant IP as shown in fig 5. This data holding circuit is a vigilant cell and called Floating prevention circuit.

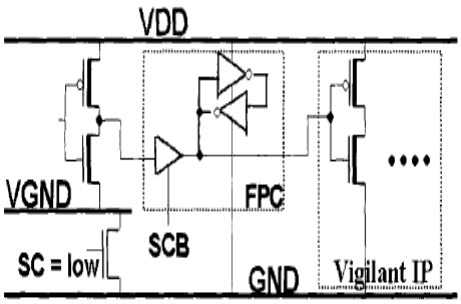

Fig 5 : Floating Prevention Circuit

III. Adaptive MTCMOS

In a modern typical worst case design style, incorporating MTCMOS in to a design requires that the design still meet timing when the logic block is at the slow process corner. By incorporating process monitoring capability on the die, the strength of the footer device can be modulated to slow down dies that are not at the slow corner, representing the vast majority of parts. In doing so, the leakage power consumption of these nominal and fast dies is reduced. The key motivation behind the following two MTCMOS schemes is to enable simple methods of compensating for process variation.

a) Variable Gate Voltage MTCMOS

This design applies a variable gate to source voltage on the footer device shown in fig 6.

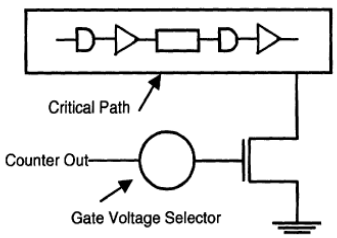

Fig. 6 : Block diagram of VGV-MTCMOS

If the process is tilted towards the fast corner, then the applied gate voltage on the footer device is lowered. Consequently, the amount of current that the device can sink is reduced, slowing down the circuit block to its nominal delay point. Moreover, since the footer device is now only weakly on, its resistance increases which then increases the average ground bounce on the virtual ground line. This rise in the average ground bounce reduces the leakage power consumption in the steady state devices in the circuit block.

When the process is tilted towards the slow corner, the footer device is fully turned on and the circuit block behaves as it would in the nominal base slower corner case.

b) Variable Width MTCMOS

The Variable width MTCMOS design uses several footer devices that can be turned on or off individually as shown in fig7.

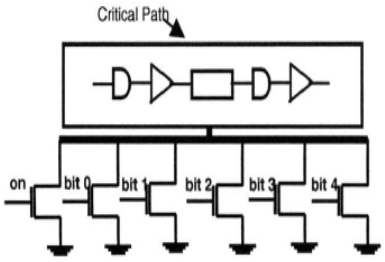

Fig 7 : Diagram of VW-MTCMOS

The Variable-Width MTCMOS (VW-MTCMOS) design incorporates several footer devices that can be turned on or off individually, as shown in fig 7. As the process tilts from one corner to the other, a different number of footers can be turned on or off to provide a varying level of current sinking capability. In standby mode, all footers are turned off as in the normal case for power gating.

For a die at the fast corner, the number of footers on during the active mode is decreased, reducing the pull down width. This reduces the current sinking capability of the footer and increases the delay of the circuit. At slow corner more footers will turn on and equivalent resistance is small between VGND and real GND.

Both GV-MTCMOS, VWMTCMOS reduces runtime leakage via the same ground bounce mechanism. As the process tilts towards the fast corner, the block becomes leakier due to shorter channel lengths and corresponding shifts in V_{th}. In this case, fewer footers are on, creating a greater resistance between the virtual ground and real ground lines which in turn raises the ground bounce. The rise in average ground bounce reduces the leakage of the block as described previously.

IV. Charge Recycling MTCMOS

A new low energy MTCMOS circuit technique based on charge recycling between the virtual power and ground lines is presented in this section. The technique is shown in fig 8. Both "gated-ground" and "gated-VDD" techniques are employed in a charge recycling MTCMOS circuit. Charge stored at the virtual ground and power lines are recycled through a high-Vt NMOS pass transistor during the mode transitions as shown in Fig. 8. The steady-state voltage difference between the virtual power and ground lines is close to VDD in both the active and the standby modes, thereby potentially producing a high sub threshold leakage current through the pass transistor.

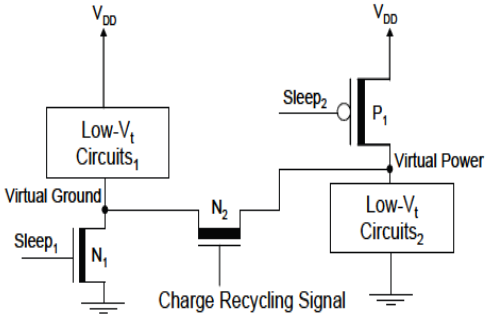

Fig 8 : The schematic of a charge recycling MTCMOS circuit. A pass transistor recycles charge between the virtual ground and power lines. High Vth transistors are represented with thick line in the channel region.

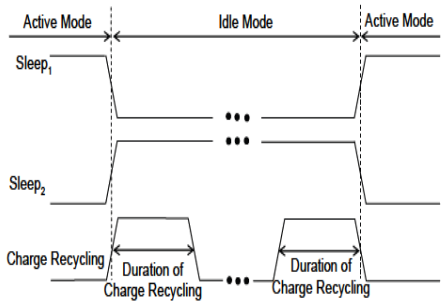

Fig 9 : The signal wave forms representing the operation of a charge recycling MTCMOS circuit during the mode transitions.

A charge recycling MTCMOS circuit operates as follows. In the active mode, the sleep transistors N1 and P1 are turned on. The pass transistor N2 is cut-off. The steady-state voltages of the virtual ground and virtual power lines are close to Vgnd and VDD, respectively. When the circuit enters the idle mode, the NMOS and PMOS sleep transistors (N1 and P1) are both cut off. The pass transistor is turned on for charge recycling. The node voltages at the beginning of the active-to-sleep mode transition are illustrated in Fig 9. Charge is transferred from the virtual power rail to the virtual ground rail through the pass transistor. The charge recycling process continues until the voltages of the virtual rails are equalized. Ilvt-1 and Ilvt-2 are higher than the leakage currents Ihvt-1 and Ihvt-2 produced by the NMOS and PMOS sleep transistors, respectively, until the steady state virtual rail voltages are reached. After the pass transistor is cut-off, therefore, the virtual ground line continues to be charged to a higher steady-state voltage by the leakage current (Ilvt-1) produced by the low-Vt circuitry1. Alternatively, the virtual power line is discharged to a lower steady-state voltage by the leakage current (Ilvt-2) produced by the low-Vt circuitry2. Since the pass transistor transfers a significant amount of charge from the virtual power line to the virtual ground line, the energy drawn from the power supply for charging the virtual ground line to ~VDD during the active-to- sleep mode transition ($E_{active\text{-}to\text{-}sleep}$) is reduced.

During the sleep-to-active mode transition, shortly before the sleep transistors are activated, the pass transistor is turned on as shown in fig 9. The pass transistor transfers charge from the virtual ground line to the virtual power line as shown in Fig. 11. There is a continuous current path through the low-Vt circuits1, the pass transistor, and the low-Vt circuits2 as illustrated in Fig. 11.

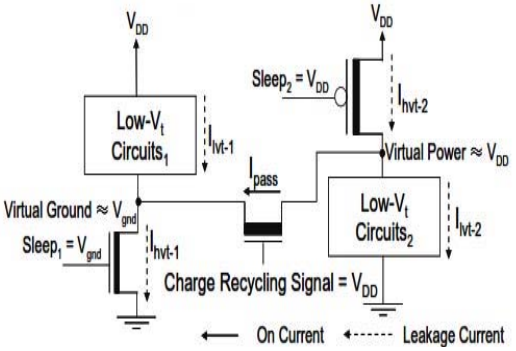

Fig. 10 : The charge recycling MTCMOS circuit at the beginning of the active-to-sleep mode transition. The pass transistor is turned on. High- V_t transistors are represented with a thick line in the channel region

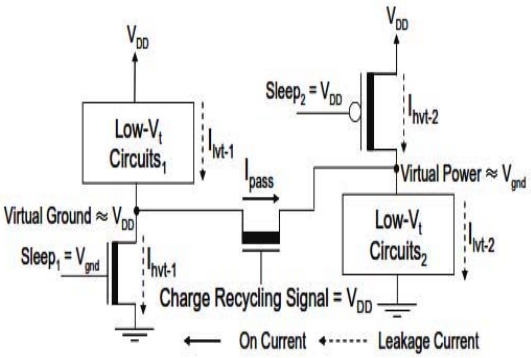

Fig. 11 : The charge recycling MTCMOS circuit at the end of the sleep mode. The pass transistor is turned on for charge recycling prior to the full reactivation of the circuit. High- V_t transistors are represented with a thick line in the channel region

After the charge recycling process is completed, the pass transistor is cut-off. The NMOS and PMOS sleep transistors are turned on for reactivating the circuit. The virtual ground line is discharged to a low voltage ($\approx V_{gnd}$) by the on-current of the high-V_t NMOS sleep transistor. Alternatively, the virtual power line is charged to a high voltage ($\approx$ VDD) by the active high-V_t PMOS sleep transistor. Since the pass transistor transfers a significant amount of charge from the virtual ground line to the virtual power line, the energy drawn from the power supply while charging the virtual power line to ~VDD for reactivating the circuit ($E_{sleep\text{-}to\text{-}active}$) is reduced.

The total energy overhead ($E_{overhead}$) due to a full cycle of mode transitions with a charge recycling MTCMOS circuit is

$$E_{overhead} = E_{virtual\ rails} + E_{sleep\ transistor} + E_{pass\ transistor}$$

$$E_{virtual\ rails} = E_{active\ to\ sleep} + E_{sleep\ to\ active}$$

The total energy overhead is significantly reduced with the proposed MTCMOS technique by suppressing $E_{virtual\text{-}rails}$ as compared to the $E_{virtual}$ consumed by the conventional MTCMOS circuits.

V. Conclusions

MTCMOS driven techniques such as the CPFF to preserve the data in the sleep mode, the FPC to prevent short circuit current are integrated in to the conventional design flow using the commercially available tools. Two new adaptive MTCMOS design techniques were introduced that reduce leakage and spread of delay. A new charge recycling circuit technique is presented for suppressing the energy overhead of mode transitions in MTCMOS circuits. The proposed technique employs both the "gated-ground" and the "gated-VDD" types of MTCMOS circuits. A pass transistor is utilized for charge recycling between the virtual power and ground lines at the beginning and shortly before the end of the sleep mode.

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