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Method to Minimize Data Losses in Multi Stage Flip Flop

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Abstract - In complex digital circuits the clock arrives at next stages before the data pulses arrives to the next stage. The clock pulse must be inserted to activate the digital circuits at any stage starting from first stage. But due to unsynchronization between clock pulse and data there is a chance of miss hitting in the next stages. This leads improper data transmissions in complex systems. It creates data losses in transmission. In the present work a gate controlled clock scheme is proposed to increase data hitting ratio.

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Method to Minimize Data Losses in Multi Stage Flip Flop

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Abstract - In complex digital circuits the clock arrives at next stages before the data pulses arrives to the next stage. The clock pulse must be inserted to activate the digital circuits at any stage starting from first stage. But due to un-synchronization between clock pulse and data there is a chance of miss hitting in the next stages. This leads improper data transmissions in complex systems. It creates data losses in transmission. In the present work a gate controlled clock scheme is proposed to increase data hitting ratio.

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I. Introduction

In light weighted circuits, contain fewer flip flops the problem may not arise. But the circuits with complex logic circuit with large number of flip-flops may face these types of problems. Because the complex logic circuits cause some delay to propagate the data from one flip flop to other flip flop or from one stage to other stage. In the present paper flip flops and delay logics are considered to describe the problem. Delay elements are often added to improve performance of a wave-pipelined circuit by reducing the delay difference of the longest and the shortest paths [1]. Unfortunately, precise delay elements that realize the exact delay needed is difficult to obtain. Instead simple logic gates are used for delay balancing, thereby providing more feasible and accurate circuit path delay control under the Min/Max delay model. A heuristic is developed to insert a sufficient number of latches into a combinational circuit to achieve a specified clock cycle time. There are already some existing methods effectively working to improve the data quality in terms of accuracy in propagation [2][3][4][5]. T. Feng proposed new wave pipeline design to achieve faster Clock Cycle Timing (CCT) [2] than the conventional pipeline methods. The author T Feng4drt wave pipeline can achieve at least a 48% performance enhancement on clock cycle time compared with the conventional wave pipeline.

This paper presents a new design method for combinational circuits with focus on circuit speed optimization. Today's high speed circuit and advanced fabrication technology facing seviour problem from delay uncertainty an extremely important issue in circuit design. The proposed method the speed optimization achieved with better Clock cycle scheme. By this intrinsic advantage of the proposed method over conventional methods, the proposed new scheme can achieve a better clock cycle than conventional methods.

The percentage of propagation error can be bringing to minimum level which is almost zero with the enhanced technology. In the conventional pipeline system it is facing problems due to improper synchronization of clock pulses. This is a universal problem in all the digital systems mostly called clock skew. The system clocking must be such that the output data is clocked after the latest data has arrived at the outputs and before the earliest data from the next clock cycle arrives at the outputs. In the present work a new system is proposed in the path of the clock to remove or reduce the clock skew. There are already few methods effectively working on clock skew such as wave-pipelining [5][6] and Me-synchronous pipeline [3] methods. The equalization of path delays comes as a new challenge for the design of wave-pipelined systems. Different clock signal paths can have different delays for a variety of reasons [7]. Differences in delays of any active buffers within the clock distribution network may cause un-synchronization of data and clock in double buffer method and wave pipeline method. And it is difficult to identify exact delay value without which the pipe line cannot perform 100% propagation.

II. Enhanced Method

In the present method simple logic gates are used in clock path to achieve higher data rates and accurate data propagation. In the present circuit the clock pulse applied to the next flip flop only when the first flip flop is ready to transmit the data wave to the next flip flop. In the present work an 8bit four stage circuit is built to test the data rates. In simple combinational circuits with little number of latches, the data propagation path is almost equal to the clock propagation path as shown in figure1. The output will follow 100% with the input. But when the stages increase in the combinational circuit with more logics and latches the propagation length of the data path will be long when compared with clock path as shown in figure2. In this crucial period it is difficult and highly impossible to get exact input data match with the output in conventional circuits.

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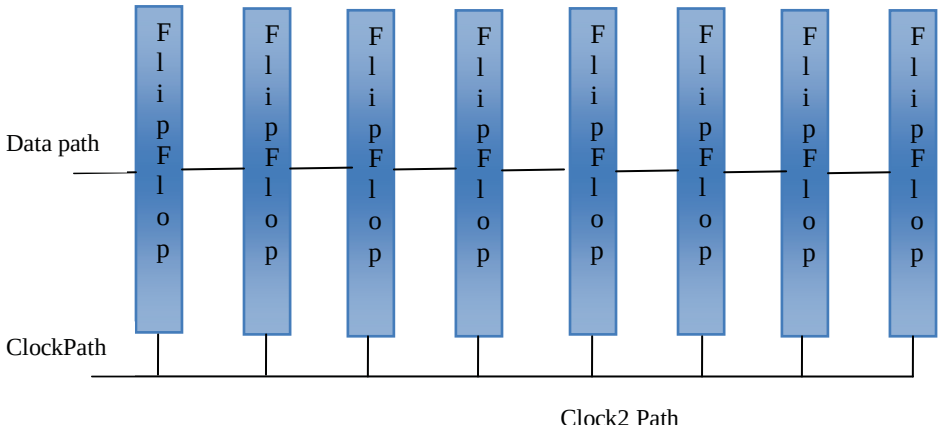

Figure 1 : Simple Combinational Circuit.

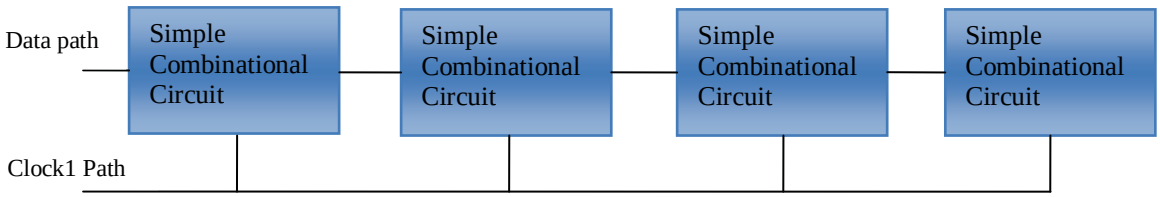

Figure 2 : Complex circuits having more logic.

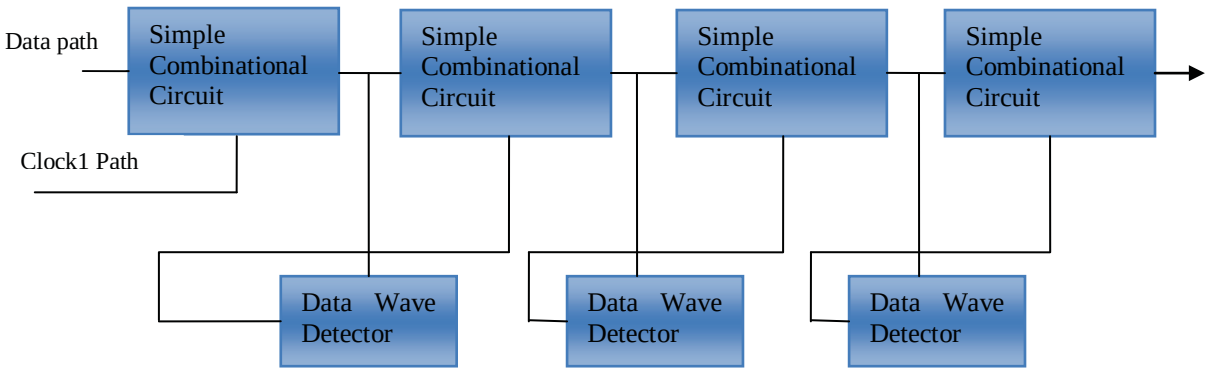

Figure 3 : The proposed Method with new clock Scheme.

The problem can be solved with new method as shown in figure 4. As the clock1 set the first stage of the circuit the data will be fed to the first stage. When the first stage data arrives at the output and ready to send to second stage the data wave detector detects the data pulse at output of the first stage and enables the second stage by clock2. Then only the first stage output will be forwarded to the next stage. Without clock2 the stage1 data cannot be transmitted to second stage, although it is arrived at output. The width of clock pulse maintained less when compared with data pulse to detect individual data pulse. The hardware connections for the same are shown in figure4 and the simulations results are shown in figure5. While the data passing from one stage to next stage, the second data travels through the internal logic of the circuit.

$$T_{wclk.n} \leq D_{wclk.n}$$

$$D_{prop.delay} \geq (T_{clk\_set.n} + D_{trav(n->n+1)})$$

$$D_{prop.delay} = D_s + D_h + \Delta_{clk}$$

s

Where, $T_{wclk.n}$ = The width of Clock signal applied at nth stage

$D_{wclk.n}$ = The width of Data wave

$D_{prop.delay}$ = The time delay taken to propagate data

$T_{clk\_set.n}$ = The clock signal used to set nth stage

$D_{trav(n->n+1)}$ = Delay produce in travelling data from nth stage to (n+1) stage

D_s = Data set time at each component of the individual stage

D_h = Data hold time in each component of the individual stage

Δ_{clk} = Clock skew

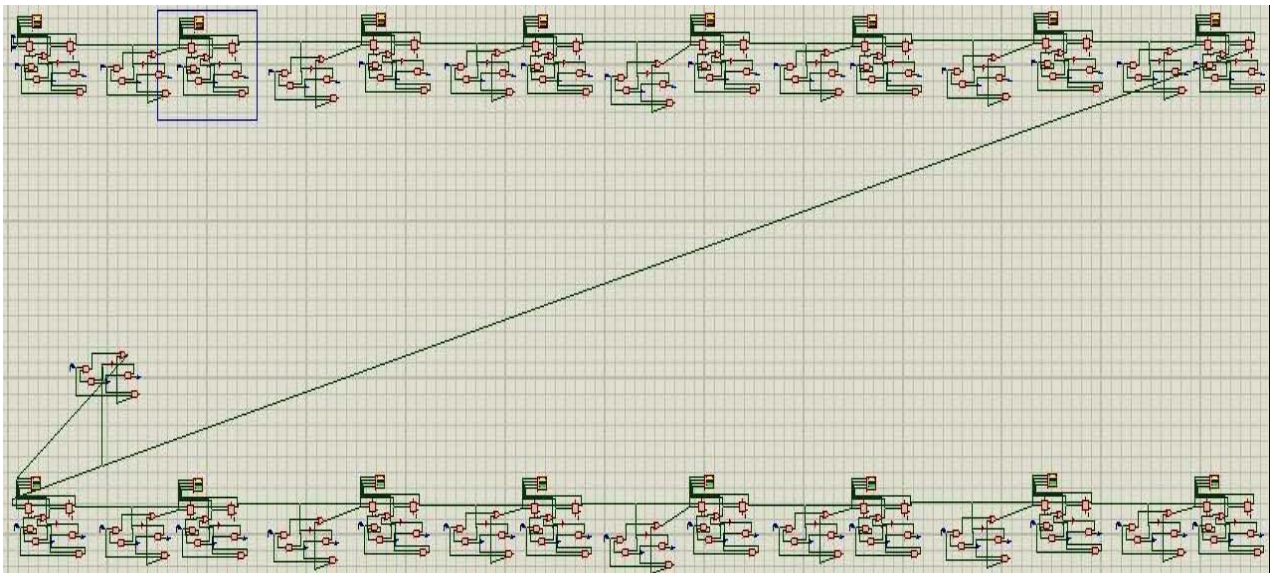

Figure 4 : Hardware Circuit Design of Eight bit Four Stage Circuit.

III. Results

The hardware is tested and simulations are verified in the software Proteus. In the figure 5 the yellow colour pulse represents clock1 and blue colour represents clock 2 applied at each stage. The input data is represented with green colour and output data is represented with pink colour at each stage of the designed circuit. In this diagram the first green and pink colour waves represent the input and output of the individual flip flop of first stage of the circuit. In the first stage the data input and output are in same phase. They appear at same clock pulse in the timing diagram. But in the second stage it is different. The second green and pink colours follow different clock phases unlike first green and pink colours. That means in the second phase the input and output appear in different phases of the clock. Because the data arrived at second stage input is after crossing logic circuit between two stages. So it took one clock pulse to come input pin of the second stage. And the clock pulse clock2 arrives after one clock pulse. So the output appears after one clock pulse after the input appears at second stage. That is the output will appear at second stage after two clock pulses after the first input appear at first stage. At the same time, while the second stage processing the first data wave the first stage receives the second data wave. That means while processing the one data wave the circuit can fetch second data wave. In the same way while the third stage processing the first data and second stage processing the second data wave the first stage will try to fetch the third wave.

Figure 5 : The Simulation results of Eight bit Four stage combinational Circuit.

IV. Conclusion

A new clock scheme is implemented for higher data rates. Parallel processing can be done with new clock system. High speed data can be read through the stages by simultaneous operations, fetching and processing through logic circuit. In the circuit the clock skew is almost minimized when compared to old methods. An eight bit four stage combinational circuit is designed to achieve accurate data.

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