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Why SEMI Standard E163 Should be Followed for the Protection of Extremely Electrostatic-Sensitive Semiconductors and Similar Devices During Manufacturing, Packaging and Handling

By Gavin C Rider

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Keywords: ESD; EFM; ESDS; EES; field induction; device damage; equipotential bonding; grounding.

Abbreviations:

ACLV: Across Chip Line width Variation (in the lithography process);
AMHS: Automated material handling system
CD: Critical Dimension (of features in a reticle);
CDM: Charged Device Model (of electrostatic discharge);
EES: Extremely Electrostatic Sensitive;
EFM: Electric Field induced Migration;
EMI: Electro Magnetic Interference;
EOS: Electrical Overstress (of devices);
ESD: Electrostatic Discharge;
ESDS: ESD Sensitive (of devices);
HBM: Human Body Model (of electrostatic discharge);
IRDS: International Roadmap for Devices and Systems;
ITRS: International Technology Roadmap for Semiconductors;
SEMI: Global semiconductor industry association (previously Semiconductor Equipment and Materials International)
TDDB: Time dependent dielectric breakdown (in semiconductor devices)
WIP: Work in progress (e.g. partly-processed wafer lots).

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I. Introduction

It has been well known for centuries that when certain dissimilar materials rub against one another especially insulating ones in a dry atmosphere – there is a generation of electric charge. This charge is referred to as "static electricity" and the process is called triboelectric charging. If an object that has been charged in this way comes close to another object, a spark can jump between them, which is known as an electrostatic discharge or ESD. Most people are very familiar with this effect since the development of man-made fibres used in clothing and carpets has introduced "the static problem" into homes and offices.

Semiconductor manufacturing environments are maintained at a relatively low humidity to prevent corrosion from taking place between wafer processing steps. The dry environment coupled with the continuous movement of machinery, materials and personnel makes the generation of static electricity very likely. If sparks take place when semiconductor devices are being manufactured or handled, the delicate structures within them can be destroyed by the current that flows into them through the spark. Machines can also malfunction if radiated energy from a spark induces errors in their control systems.

Methods have therefore been developed to reduce the likelihood of sparks occurring in the manufacturing environment or in any place where the devices are subsequently handled. To protect sensitive devices against a spark striking them if any of the safety procedures fail, protective circuitry is normally built into them. Electrostatic discharges exhibit different characteristics depending on where they originate, and

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the two main classifications for discharges that are likely to affect semiconductor devices are referred to as the Human Body Model and the Charged Device Model.

Devices are now designed, tested and certified to be able to withstand discharges of a specified strength from either of these sources. The environments in which semiconductor devices are handled are controlled so that any electrostatic risk that might be created will be below the level that could cause the devices to be damaged. There are international standards in place defining how such environments should be controlled and how the operations within them should be conducted. An example is ANSI ESD S20.20 [1].

II. The Control of ESD in Semiconductor Manufacturing

The standard principles that have been applied for controlling ESD in semiconductor manufacturing are probably familiar to most people working in the industry, as anyone working with semiconductor devices will be trained in how to avoid static-related problems:

1. Eliminate all non-essential insulators because they can accumulate static electricity
2. Neutralize all essential insulators using methods such as air ionization
3. Connect all conductive objects to a common electrical potential, normally ground (which is known as “equipotential bonding”).
4. Personnel working within a factory are required to wear conductive clothing and to be connected to ground, either through conductive footwear or by a special grounding strap at a workstation.
5. Workstations are required to be grounded, to have static dissipative work surfaces and to have supplementary methods of charge neutralization, such as ionized air showers.

It is necessary to ensure that any material being transported within a factory is at the same electrical potential as its destination, to eliminate the possibility of an electrostatic discharge taking place when it is delivered. Hence it has become standard practice to ground objects while they are being moved, for example by employing drag chains on the carts used to carry wafers between processing stations, or by using a grounded AMHS. To avoid any risk of a high-power discharge taking place on connection to ground, resistive contact materials (otherwise referred to as “static dissipative”) are used. Wafer boats, chip trays and WIP transfer boxes are now generally specified to be made from static dissipative materials.

A focus in the design of automated equipment in semiconductor manufacturing in recent years has been to try and reduce the generation of static charge within the equipment anywhere near the handling path of the sensitive devices being manufactured. The presence of static charge is typically revealed during an electrostatic audit by detecting the electric field that the static charge produces.

Steady-state measurements can be performed using hand-held field meters, but inside fast-moving equipment such as pick-and-place machines it is necessary to use equipment with a fast response time, such as digital electrometers and storage oscilloscopes. However, as will be mentioned later, even some of the fastest field-recording equipment available is not able to detect all electrostatic risk. The limitations of the measuring equipment being used in any electrostatics audit must always be considered, since the failure to register electrostatic risk on a meter does not necessarily mean that there is no risk present.

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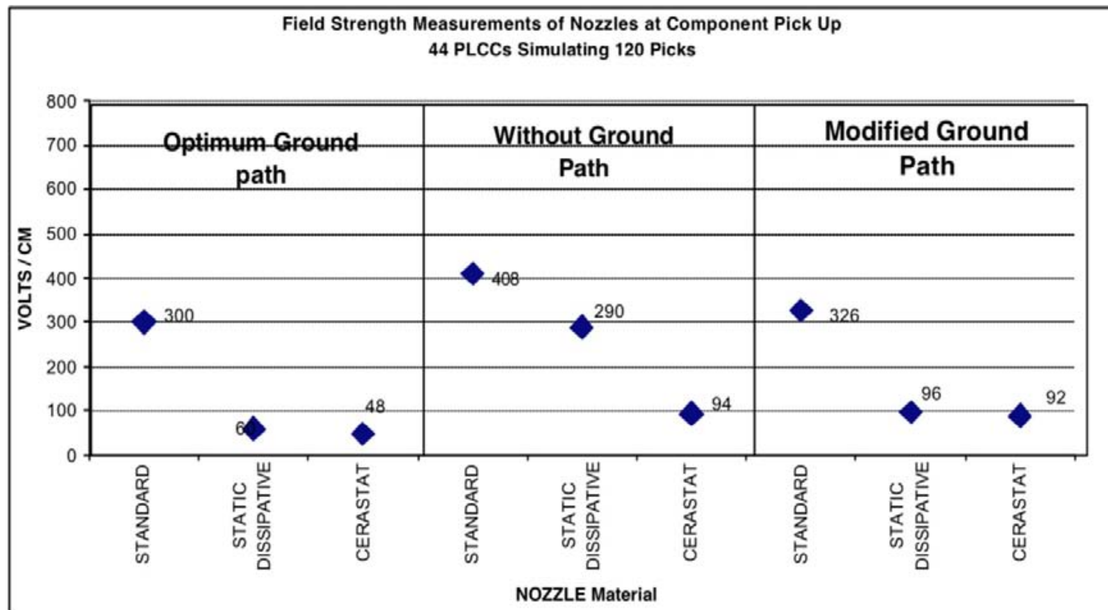

Figure 1: Reduction in the level of electric field generated within a piece of automated material handling equipment by optimizing the design of the ground path and changing the material of the vacuum nozzle used to pick and place the components. Reproduced from [2].

Figure 1 presents the result of a program of electrostatic risk reduction in automated handling equipment [2], showing that electric fields can be significantly reduced through suitable equipment design and material choices, but they are generally not eliminated completely. Hence, some electric field is always likely to be present in the environment around sensitive devices during their manufacture and handling. Furthermore, the author of this study states in his observations:

"the typical end user of components in their assembly work, whether Contract Electronic Manufacturing or Original Equipment Manufacturers, do not or cannot obtain accurate sensitivities of the components they are trying to handle with automated equipment".

This means that there is always likely to be some electrostatic risk present during semiconductor and electronic device manufacturing, but the degree of susceptibility to that risk is generally unknown.

III. An Overview of Reticle Electrostatic Damage Studies

Electrostatic damage to the lithographic reticles being used to print semiconductor device layers has always been a problem, but it became critical at the end of the 1990s when around 50% of the reticles being returned to mask manufacturers for repair had sustained ESD damage. Since damage to semiconductor devices was already known to be caused by ESD events during their handling, it was presumed that reticle damage was being caused in the same way; by the transfer of static charge to or from the reticle while it was being handled. Hence, it was decided that protection of the reticle would be best achieved by adopting the methods that were already being used for device protection. Guidance was therefore published stating that reticles should always be handled using grounded conductive tools fitted with static dissipative contact materials [3].

However, research into reticle electrostatic damage conducted at International Sematech and other independent sites identified that reticles are susceptible to ESD damage simply by being exposed to an electric field [4]. It was found that damage can be induced within a reticle pattern by an externally generated electric field, without any charge transfer taking place to or from the reticle and without the reticle even being touched. Measurements of the strength of electric field that would cause ESD in typical production reticles in this way led to further guidance being published through the SEMI Standards program and through the ITRS (now replaced by the IRDS) to limit the level of electric field to which reticles might be exposed.

The program of risk reduction undertaken in the areas where reticles were handled followed the general principles described earlier, including the replacement of insulating plastic with static dissipative alternatives. The insulating plastic pods and boxes that were being used to store and transfer reticles were replaced with static dissipative ones, to reduce the likelihood of the box generating an electric field by being tribocharged during handling. This change, when introduced alongside all the other static-reduction measures being taken in lithography areas, resulted in a significant drop in the amount of reticle ESD damage. Since the problem appeared to be understood and controllable, most research programs studying reticle electrostatic damage

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were closed down. The International Sematech research project into reticle electrostatic damage was ended in 2003.

Unfortunately, the belief that reticle electrostatic damage would no longer be a problem was short- lived. Shortly after the introduction of static dissipative plastic reticle pods and boxes it was found that they are not able to adequately protect a reticle from electric field, because electric field can penetrate static dissipative materials. Levit and Weil [5] had measured the penetration of electric field into a reticle pod from an electrode positioned outside, simulating the charged hand of an operator carrying it. They showed that the pod was only partially effective at shielding the reticle from the electric field, and that the shielding effectiveness dropped rapidly as the frequency of the applied field was increased. It took almost a second for the static dissipative plastic pod in their tests to fully screen a constant external field, but any field that changed within that time would not be fully screened. If the field changed more rapidly than about 25Hz, the shielding effect was very poor indeed. The static dissipative material used to make the pod was acting as a high-pass filter, allowing rapidly changing electric fields to reach the reticle inside the pod.

This particular characteristic of static dissipative materials had been studied more extensively by Chubb [6], who quantified the field-shielding effectiveness of various materials that were being used for packaging in electronic component handling, at frequencies up to 1GHz. Figure 2 shows his measurements of field transmission through a metallized plastic "shielding bag" and also through a static dissipative bag. In both cases the conductivity of the material was insufficient to fully screen the bag's contents from electric field, and the shielding efficiency of the static dissipative bag fell away rapidly as the frequency of the field was increased (note the logarithmic scale). The behaviour as a function of frequency shown in b) is a characteristic of all static dissipative plastic materials.

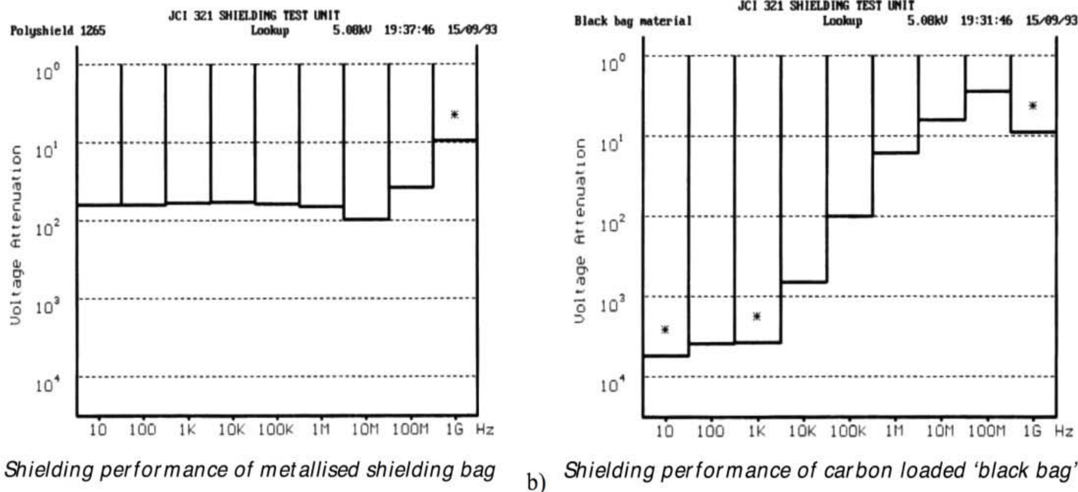

Figure 2: Chubb's measurement of the field penetration characteristics of different materials used to make static protective bags: a) Field attenuation by a metallised plastic bag; b) Superior field attenuation at low frequency by a carbon loaded (static dissipative) plastic bag, but inferior shielding at higher frequency.

Chubb noted:

"Electrostatic spark discharges involve current rise times and voltage collapse times down to below 1ns. Lower voltages shorter times. Transport packaging hence needs to provide >200:1 attenuation for frequencies to 1GHz."

The Sematech research had proven reticles to be extremely sensitive to field-induced damage, and they were known to require much more effective shielding from electric fields than packaged semiconductor devices, so Chubb's specification would not be sufficient for reticle protection. Based on Chubb's criteria and Levit's measurements of pod performance, reticles were certainly not going to be adequately protected from electric field by the static-dissipative reticle pods that had been developed in an effort to protect them.

Other research findings were published in December 2003 that also challenged the wisdom of the decision to end the Sematech project [7, 8]. It was shown that the predominant electrostatic risk to reticles is from field induction rather than conductive ESD as had previously been thought. Ironically, it was also shown that the grounding of reticles during handling – a practice that had recently been introduced to protect them – actually made the risk of field-induced damage worse rather than reducing it. Furthermore, a newly-identified form of field-induced reticle damage called EFM had been identified. Unlike ESD, which instantaneously causes very obvious damage to a reticle, EFM is a gradual degradation process that does not generate easily detectable damage, but it does interfere with the lithography process and cause yield

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loss. It progresses cumulatively, under levels of field-induction at least two orders of magnitude weaker than would be necessary to induce ESD (as determined for a typical production reticle in use at that time).

This new study, which had identified serious errors in the advice that had been given for reticle electrostatic protection, created disquiet in the electrostatics consultancy community. There was a great deal of scepticism expressed by ESD experts over the assertion that equipotential bonding increases the electrostatic risk to a reticle rather than reducing it. This had been identified through computer simulation, and it was believed by many electrostatics experts that the simulations were wrong, because the indications from the simulations were not in accord with their practical experience of ESD prevention in the semiconductor industry. However, the study's findings were subsequently confirmed by experimentation with production reticles and special test reticles [9], demonstrating that field induction is a subject that can confound even those who specialise in electrostatic protection and have many years of practical experience of it within the semiconductor industry. "Established wisdom" is not necessarily correct.

The evidence that static dissipative plastic reticle pods were probably not sufficient to protect reticles against field-induced damage, and the persistence of reticle electrostatic damage events in some facilities that were using them, led to efforts being made to increase the conductivity of the pod material. New "conductive" plastics were developed having carbon nanotubes embedded within the matrix to enhance electrical conduction, and a study conducted in 2006 [10] compared the field- shielding performance of a pod made with this new material against other types in widespread use. The results of the testing are shown in Figure 3.

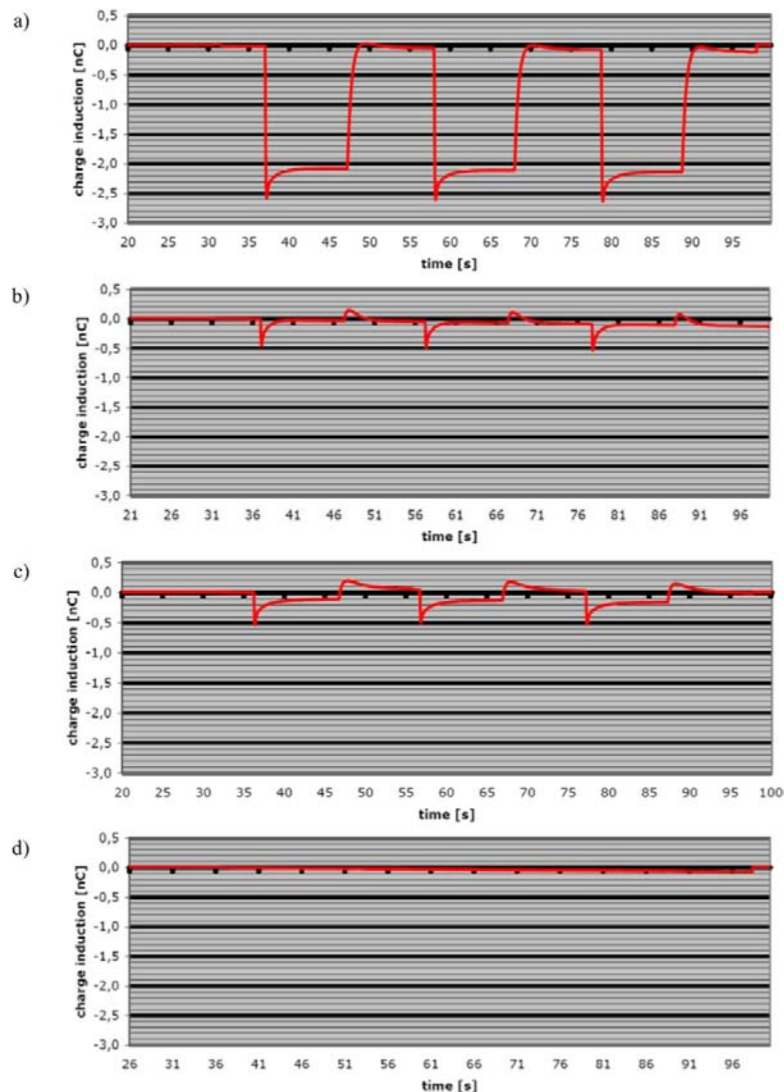

Figure 3: Helmholtz and Lering's measurement of field penetration into a variety of reticle pods with differing degrees of conductivity, from [10]. a) Applied field. b) ABS pod. c) PEI pod. d) Carbon nano tube loaded PEEK pods (two were tested and both were at the limit of detection).

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The tests showed that increasing the conductivity of the plastic reduced the field penetration into the reticle pod to the limit of electronic detectability. However, even this degree of shielding did not prevent field-induced ESD taking place in a test reticle inside the pod. If field penetration into such a reticle pod was sufficient to induce ESD in the reticle inside it, it would certainly not offer adequate protection against other forms of field-induced degradation such as EFM, which takes place under much lower electrostatic stress. The research by Helmholtz and Lering also confirmed that because the conductive plastic reticle pods had conductive paths connecting the reticle to the grounded load port (a supposedly protective design following the principles outlined earlier) field induction was enhanced and the rate of reticle damage was actually increased by it.

In 2008 further experimental research into EFM was published [11,12] confirming the initial interpretation of the reticle damage mechanism as the field-induced migration of chrome. This study fully quantified the effect and showed that reticles were even more sensitive to electric field than had been estimated five years earlier when EFM was first identified. The degradation characteristics were illustrated with an atomic force microscope image of a damaged reticle structure, overlaid with an electric field computer simulation to indicate the local electric field strength corresponding with the different damage effects observed. This image is reproduced in Figure 4.

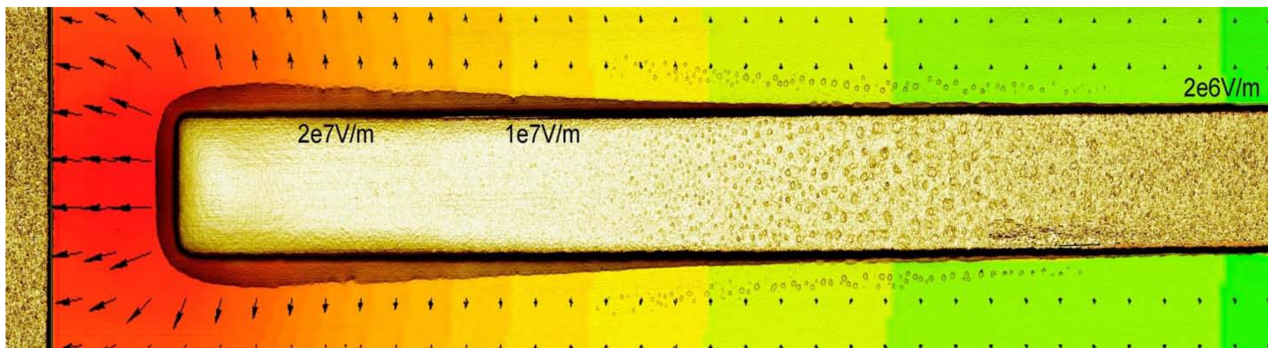

Figure 4: Composite atomic force microscope image of a field-damaged reticle structure, overlaid with a computer simulation to indicate the electric field strength corresponding to the observed damage effects, reproduced from [12].

Other research being conducted around the same time into reticle degradation in semiconductor production confirmed that as well as directly distorting the reticle features through chrome migration, EFM could also cause ACLV in the printed pattern by reducing the light transmission of the clear areas of the mask [13]. Device yield had been impacted by this subtle form of reticle degradation, even though the reticle had passed regular inspections with no defects being detected. It required the use of highly specialised surface analysis and destructive failure analysis techniques to unambiguously identify the cause of the yield loss as chrome migration [14]. This difficulty with first detecting and then correctly diagnosing such subtle reticle degradation effects perhaps explains why, more than fifteen years since its discovery, EFM is rarely being identified as a reticle damage mechanism in modern semiconductor production fabs – even though it is almost certainly happening.

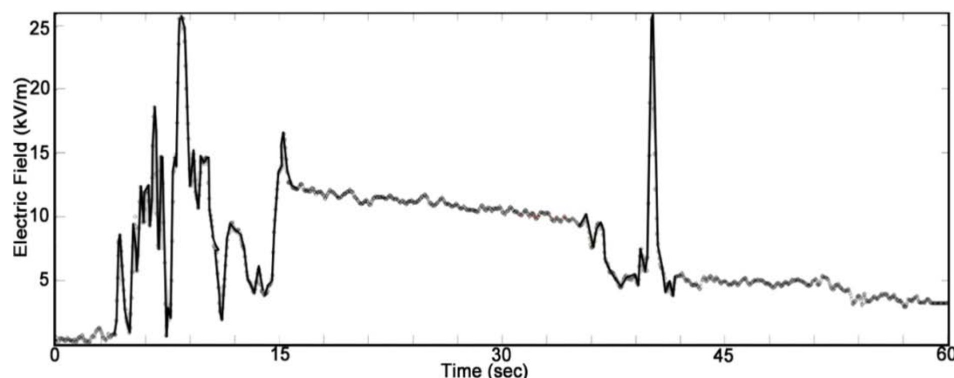

Figure 5: Measurement of a reticle's exposure to electric field while being carried in a static dissipative single reticle pod in a semiconductor production facility equipped with all the standard ESD countermeasures, including air ionizers.

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A new sensor device had been developed following the discovery that reticles are extremely sensitive to electric field. This self-contained recording device had the same form factor as a normal six-inch reticle and it could record the electric field to which the sensor was exposed under the same conditions that would be experienced by a standard production reticle [15]. This sensor device has been extremely valuable in allowing hidden areas of electrostatic risk within semiconductor fabs to be identified. One of the first measurements made was of a normal handling sequence in a production facility using a static-dissipative single reticle pod. The measurement, which is shown in Figure 5, reveals that a reticle carried in a static dissipative reticle pod is repeatedly exposed to electrostatic stress from transient electric fields. The level of field penetration into the reticle pod was confirmed to be sufficient to cause cumulative damage in production reticles, following the earlier quantification of reticle sensitivity to EFM [11,12]. Another test carried out with the sensor reticle revealed that static dissipative reticle pods actually generate significant electric field transients through tribocharging during normal use, something that had previously been believed not to happen with static dissipative materials, mainly because of an inappropriate testing methodology using field meters with insufficient temporal response.

The most recent assessment of all the effects that can be produced by field induction in reticles [16] identifies the heightened risk posed by rapidly changing and transient electric fields, and concludes that very short-duration field transients and rapidly changing electric fields up to gigahertz frequencies and beyond would be capable of causing cumulative reticle damage. This is because electric fields cause charge displacement within the reticle pattern every time the field conditions within the reticle change. Rapidly oscillating, pulsed or transient fields are particularly hazardous, because one field cycle produces two charge displacements, once as the field increases and again as it decreases.

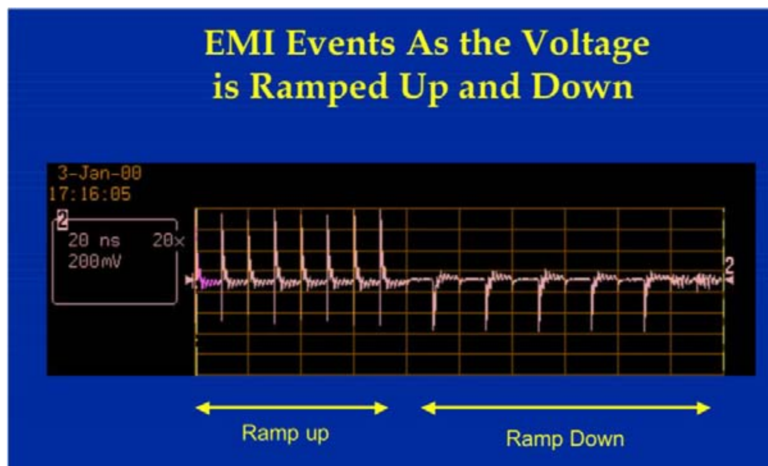

Figure 6: Measurement of multiple sequential ESD events induced within an electrically isolated reticle as the voltage on a nearby electrode is first increased and then decreased, from [17]. The opposite polarity of the signals as the field is removed indicates that the displaced charge that caused the initial series of ESD events is returning to its original location within the reticle and causing further ESD damage.

This characteristic was demonstrated during the field induction experiments conducted by Montoya et al [4,17]. Spark discharges induced within the reticle pattern by a high potential applied to an electrode held just above the reticle were detected using an RF loop antenna connected to a storage oscilloscope, as shown in Figure 6, which is from their presentation at the Sematech ESD Symposium of 2000. As the voltage on the electrode was increased, sequential discharges were detected within the reticle. Then, as the voltage was removed, discharges of opposite polarity were observed as the displaced charge within the reticle returned to its original location.

Extremely rapid field transients that are capable of being generated and transmitted by static dissipative and conductive plastics are responsible for the ESD damage in the test reticle reported by Helmholtz and Lering [10], yet neither their fast recording oscilloscope nor this new sensor reticle would have had sufficient sensitivity and response time to detect the threat they pose. There remains a significant level of electrostatic threat that can damage reticles but cannot be detected electronically.

The movement of charge that contributes to the reticle damage is induced entirely within the reticle pattern; the reticle remains electrically neutral throughout the process. The reticle inherently amplifies any electric field that is present in its environment by up to several orders of magnitude, the degree of amplification depending on the arrangement of the

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isolated conductors in the image. This field amplification results from the movement of electrons within the reticle's conductive structures so it happens almost instantaneously, and it explains why undetectable amounts of electric field penetrating a reticle pod [10] could be sufficient to induce ESD and other forms of cumulative damage. This field amplification characteristic is illustrated by the computer simulation of Figure 7.

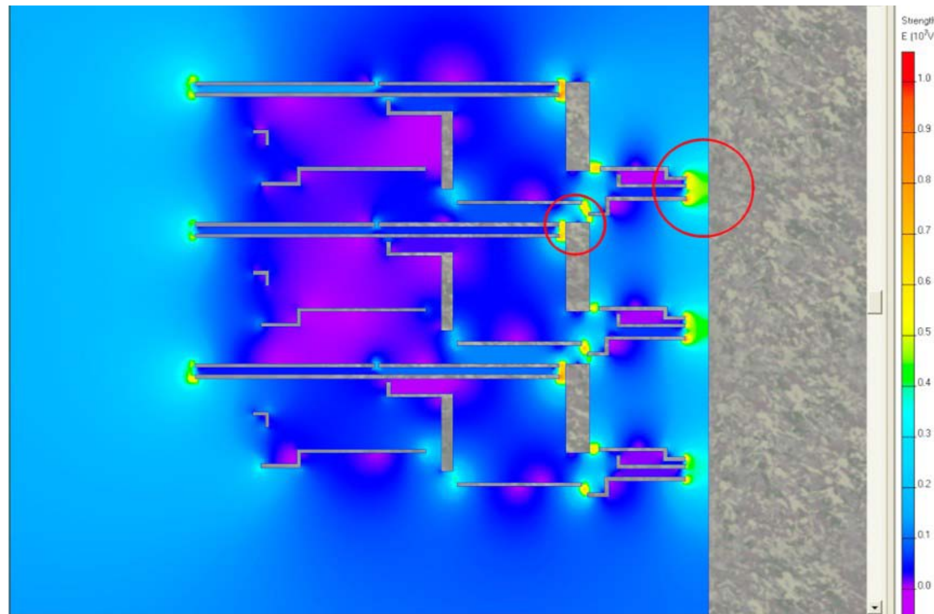

Figure 7: Two-dimensional finite element simulation of the interaction of an electric field with a reticle. The grey structures represent isolated conductive lines, with the large grey block on the right representing the border around the image area. A uniform electric field with a strength represented by the mid-blue tone at the left of the image is applied from left to right. The field strength is reduced in some areas but amplified at the ends of long lines, particularly between closely adjacent features near the edge of the image (circled).

The field amplification is a function of the orientation of the reticle pattern relative to the electric field, so simply moving the reticle without changing the electric field it is exposed to will also change the field conditions within the reticle pattern, with a corresponding risk of the reticle being damaged. A similar situation occurs if conductive objects such as robotic arms are moved within the vicinity of a reticle in the presence of an electric field, because such objects perturb the electric field around and within the reticle. The perturbation of electric field by conductive robotic arms is illustrated by the recording in Figure 8, which was made using the field-sensing reticle mentioned previously [15].

The evidence from Figure 8 is that the ESD countermeasures such as equipotential bonding that have been introduced into semiconductor manufacturing facilities are not necessarily effective for damage prevention. If the static charge that grounding is intended to remove is located on an insulating part of the object being handled, which it most probably would be, grounding cannot remove it. As shown in this recording, the use of a grounded handling tool creates a risk from field perturbation that otherwise would not be experienced by the reticle. It also demonstrates that unless ionizers are correctly installed and maintained they can actually create an electrostatic risk – one that is accentuated by the use of equipotential bonding.

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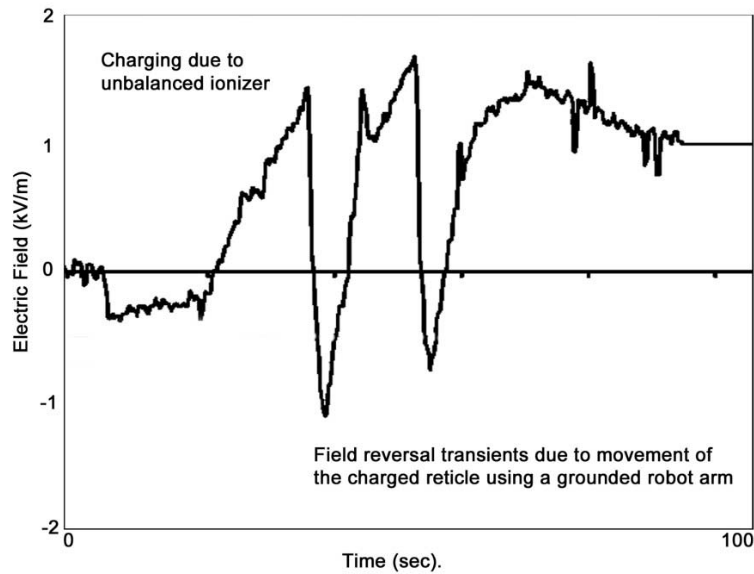

Figure 8: Electric field recorded by a sensor reticle introduced to a piece of reticle handling equipment fitted with an unbalanced ionizer and a grounded robot arm with static dissipative reticle contacts. The electric field generated by the charge on the reticle is strongly perturbed each time the robot arm approaches to move the reticle. Note that grounding the reticle through static dissipative contacts does not remove the charge.

This point is further illustrated by Figure 9, which shows the electric field recorded by the sensor reticle as it was being loaded into another piece of reticle handling equipment that had been fitted with an ionizer to neutralize incoming reticles at the loading station. The ionizer had been installed much too close to the reticle's handling path, so pulsed electric field from the ionizer tips was reaching the reticles as they passed underneath it. Every pulse of electric field from this ionizer was capable of causing field-induced damage in the reticle pattern, and after passing the ionizer the reticle had been put into a charged state, just as in Figure 8.

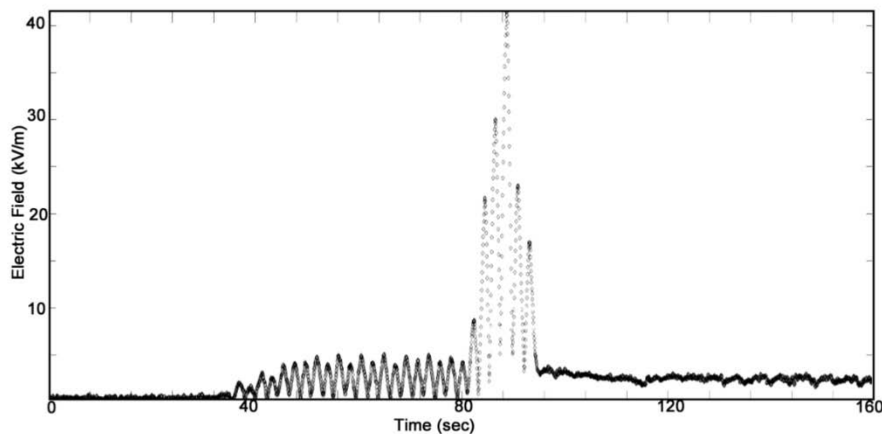

Figure 9: Electric field measured by a field-recording test reticle as it was loaded into equipment that had been fitted with an ionizer bar over the loading station. The ionizer was too close to the reticle path and it exposed every reticle loaded into the equipment to dangerous levels of electric field. The offset in the readings after passing the ionizer also shows that the reticle had been charged.

The studies into reticle electrostatic damage illustrated here have revealed shortcomings in the electrostatic protection principles adopted by the semiconductor industry and have also revealed errors in the implementation of them, the most significant two being the use of equipotential bonding and of making reticle pods and boxes from static-dissipative plastic. While equipotential bonding does indeed result in the elimination of conductive ESD events when material is being transferred from one manufacturing station to another, it does not protect field-sensitive items from the damaging effects of exposure to electric fields – it actually makes the damage worse. Static dissipative plastic reticle pods have been shown to allow hazardous

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levels of electric field to reach the reticle stored inside them, and such pods actually generate transient electric fields during normal use.

The conclusion reached here is that for absolute security no amount of exposure to electric field should be considered safe for any transmission reticle. The wisdom of making reticle pods from static dissipative or even "conductive" plastic is called into question, and because equipotential bonding increases the impact of any field exposure that might take place during reticle handling or use, it should not be used when handling reticles.

IV. Implications for the Safe Handling of Electrostatic Sensitive Devices

When material handling 'best practice' was being defined for the semiconductor industry decades ago the problem was addressed in a logical but somewhat over-simplistic way. It was apparent that semiconductor devices were being damaged by conductive ESD during handling and the deduction was that if the ESD could be prevented, so would the damage. Indeed, the control of ESD during semiconductor manufacturing has been accompanied by a corresponding yield improvement. However, it was not correct to believe that eliminating ESD meant that reticles would be safe, so it is probably not correct to think the same about the electrostatic safety of sensitive electronic devices.

The semiconductor industry almost exclusively characterizes device electrostatic sensitivity by means of discharge testing, for example as described by Diaz [18]. Diaz observes that there are two different forms of damage that can be caused to devices; thermal effects due to a current surge from an ESD event or from EOS, and field effects such as dielectric breakdown and latent hot-carrier damage. "Hot-carrier" damage refers to a reduction of the electrical resistance of dielectrics as a result of being exposed to an excessive electric field. Points of weakness in the dielectric caused by excessive electric field can subsequently break down completely during device operation, producing thermal damage that appears similar to EOS or ESD.

There is, unfortunately, a "grey area" wherein some of such electrostatic damage is classified as EOS and some as ESD, with no clear indication of the origin of it. Distinguishing between the two mechanisms after the damage has occurred is very difficult indeed, and it is almost impossible to determine the precursor state after breakdown has happened.

Identifying the root cause of the failure requires a detailed understanding of the physical mechanisms involved and very careful analysis of the damaged area. It was possible to do this quite easily in reticles, because the damaged features were easily accessible for AFM imaging, which meant that the subtle differences between ESD damage and that caused by EFM could be identified. They could then be characterized and quantified through controlled experimentation, as shown in Figure 4. Real-life damage signatures in semiconductor devices are far more difficult to deconvolve, because the damage is usually extensive and can completely destroy the damage site. It can also be necessary to expose the damage site deep within the device by carefully deconstructing it in order to analyze the damage, which is a laborious and difficult task that is not routinely undertaken. For this reason, a great deal of device electrostatic damage is probably being incorrectly classified, which also means that the root cause is not being correctly understood. Failing to correctly identify the root cause of electrostatic damage can result in inappropriate guidance being given to try and prevent it (as happened when equipotential bonding was recommended to prevent reticle electrostatic damage).

It is believed by many people that the spark between a charged device and ground results in the device literally becoming "discharged", meaning neutralized. For example, Diaz states in his article [18] "*Electrostatic discharge occurs whenever a charged object is grounded, resulting in the release and equalization of the static charge*." The impression that neutralization has occurred is reinforced when a device that has experienced such an ESD event is measured using a Faraday cup and is found to carry little or no net static charge. However, this impression is wrong in most cases.

The static charge on a charged device will most likely be present on an external insulating surface as a result of tribocharging during handling. The spark that jumps between ground and the charged device generally strikes one of the connector pins, which is why it injects a current pulse that damages the internal circuitry. So, what actually happens during such a CDM static discharge event is that an opposite charge to that present on the encapsulation enters the device circuitry from ground, attracted by the electric field from the static charge on the encapsulation. The opposite charges cannot physically recombine and neutralize one another as they are separated by insulating material. Hence, such balancing of the charge on the device as a consequence of grounding it results in the device being in an energized state, just like a charged capacitor. It contains electrostatic potential energy, just as a charged capacitor does, stored within the internal electric field. The same final energized state would be achieved whether the balancing charge flowed into the device rapidly through a spark or slowly as a reduced current through a resistive contact in an equipotential bonding scheme.

If the flow of balancing charge into the device is gradual, as in an equipotential bonding scheme where static dissipative contact materials are used, there is no

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initial current surge that can cause the thermal damage effects described by Diaz. Hence it would be correct to say that ESD damage had been prevented by the equipotential bonding scheme slowing down the transfer of charge – but field- induced damage effects that can result in latent dielectric damage could still occur if the internal electric field generated by the balancing charge exceeded the capacity of the dielectric layers in the device to withstand it.

ESD protection circuitry is generally designed to shunt an incoming current surge in order to protect the device's operational circuitry, but it will not change the final location reached by a balancing charge, as this will be determined by the physical layout of the device and the location of the static charge on the encapsulation. The balancing charge will move as close as possible to the static charge on the encapsulation, driven there by the internal electric field. Therefore, even if the ESD protection circuits do prevent an immediate thermal damage event by diverting the route taken by the charge as it enters the device, they may be ineffective at preventing any field-induced damage that occurs as a result of the injection of a balancing charge.

A similar risk from the generation of internal electric fields could also be created in a partly-processed silicon wafer should it become charged during processing, which is a common occurrence. If the partly completed devices on the wafer contain conductive layers separated by dielectric barrier layers, an electric field can be generated between the isolated layers. If a balancing charge were introduced to the substrate from ground during handling, attracted by static charge on an outer insulated layer of the partially-completed wafer, the balancing charge would distribute itself within the wafer until it approached as close as possible to the static charge, after which any further charge movement (and ultimately, static charge neutralization) would be prevented by the interposed insulating layer(s). Like the device in the previous scenario, the wafer would appear to be electrically neutral but it would be in an energized state, just like a charged capacitor.

An excessively strong electric field can damage the structure of dielectric material, resulting in the rearrangement of the atomic bonds, which degrades its insulating strength. The mechanism by which dielectric degradation happens is described by Azizi and Yiannacouras [19]. It has been shown by Pey and Tung [20] that this mechanism and the degradation it produces are independent of the dielectric composition. Hsu et al report that the dielectrics being used in latest-generation devices exhibit degradation that is dependent on the field strength within the dielectric [21]. Another field- induced damage process in semiconductor devices involves the diffusion of dopants and contaminants [22]. This can alter the electronic properties of devices that rely on a particular dopant profile within their active features, or create conduction barriers at interfaces.

So, it is conceivable that enhanced electric fields produced within a device while it is being manufactured, as would be likely to occur as a result of using equipotential bonding, could potentially cause any of the above described damage effects.

Some devices may continue to operate as they were designed to, but the robustness of a damaged dielectric to EOS or TDDB (which is a life-limiting aspect of many semiconductor devices) will be reduced. Any material degradation that has the capability to cause premature failure is classified as a "latent defect", and it is evident that the practice of equipotential bonding has the capability to introduce such defects into devices and wafers that have become charged during handling or processing.

Clearly, any procedure that can generate an uncontrolled internal electric field within a device containing thin dielectric layers must be considered potentially hazardous – and that is exactly what equipotential bonding can do. The ultimate consequence of a device being stressed in this way would be dependent on the type of device and would also be affected by how it was subsequently handled and operated. When failure eventually happened, it would not be apparent that the use of equipotential bonding during the manufacture of the device could have contributed to its demise. It would be practically impossible to identify the root cause of such a delayed failure.

V. Discussion

At this point, it is perhaps worth reflecting on the fact that the potentially harmful outcomes described previously rely on a combination of two factors, one of which is avoidable:

a) Charging of the device (which is not always avoidable, but is not itself damaging) and
b) Grounding of the device.

It is not possible to directly observe the described effects in a semiconductor manufacturing environment, so there is currently no empirical evidence from semiconductor manufacturing sites to analyze. Such effects could only be observed and measured if carefully designed experimentation were carried out, in much the same way as reticle electrostatic damage was extensively studied at Sematech. Even then, it would be necessary to analyze the results very carefully to avoid the risk of reaching false conclusions, as initially happened with the analysis of the Sematech data. Re-evaluation of the Sematech reticle damage data ultimately led to the completely unexpected discovery of both EFM and identification of the detrimental effect of equipotential bonding. Similar studies could potentially reveal previously unidentified field-induced damage effects in semiconductor devices.

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There have been some heated discussions about the sensitivity of semiconductor devices to electric fields and the effectiveness of equipotential bonding for device protection in online discussion groups, following the research into reticle damage. The perspective of most electrostatics consultants working in the semiconductor industry seems to be that packaged devices are not field-sensitive. They also state that their experience gained over decades working in semiconductor manufacturing proves that equipotential bonding is protective, because damage rates are improved when using it. However, as mentioned previously, the avoidance of immediate thermal damage from an ESD event by using static dissipative contacts to ground a device does not mean that the grounding of the device is an inherently safe procedure. Grounding does not remove static charge from an insulating part of the device and it does not actually neutralize the device, but it does inject a balancing charge that creates an internal electric field. Since the purpose of grounding the device is actually the removal of static charge and the neutralization of the device, it does not seem to be a particularly valuable result to avoid an ESD event while failing to achieve either of these objectives. Not grounding the device would achieve the same outcome, but it would also avoid the generation of potentially hazardous internal electric fields through the injection of a balancing charge.

While the disagreement continued about whether or not devices are susceptible to damage from electric fields, Smallwood [23] conducted a simple experiment. He demonstrated that it is possible to damage ESDS semiconductor devices through field induction alone, without a conductive ESD event taking place. His simple experiment confirms that the principles presented in this paper are valid and that the concerns expressed here are justified.

One further unforeseen negative consequence of using equipotential bonding to try and remove static charge from devices during handling is that grounding a charged device virtually eliminates external electric field, by balancing the charges held on the device. Ionizers are the only practical way of neutralizing static charge on an insulator, and they are widely adopted in semiconductor manufacturing to help control static charge accumulation. Airborne ions of the appropriate polarity respond to the presence of static charge by being attracted by the electric field it creates, while ions of opposite polarity to those needed for neutralization are repelled. If the external electric field emanating from a tribocharged device is nullified by the injection of a balancing charge into the device from ground, it removes the mechanism through which charge neutralization by an air ionizer is achieved. Thus, grounding is not only incapable of safely neutralizing a charged device or wafer, it acts against the only feasible method of doing so.

The importance of understanding and controlling all forms of device degradation, going beyond those typically caused by ESD, has been emphasized by Sonnenfeld et al [24] who state:

"…it is not widely known how degradation mechanisms propagate as a function of environmental conditions and various stressors. The attainment of such knowledge is critical for advancements in the field of power electronics health management and prognostics. The ability to perform large scale experiments and characterize the degradation signatures of such semiconductor devices under various scenarios is of great interest…

The assumption of new functionality will also increase the number of electronics faults with perhaps unanticipated fault modes. In addition, the move toward lead-free electronics and microelectromechanical devices (MEMS) will further result in unknown behaviors."

The study of field induction in reticles and the computer simulations performed to help the understanding of field induction on a nanometer scale, which cannot be directly measured, have demonstrated that measurements of charge and voltage on a macroscopic scale during typical ESD audits in a factory environment tell only a partial – and often misleading – story. It is necessary to consider the physics that operate on the scale of the device structures themselves, or even at an atomic level, to fully appreciate the varied detrimental effects that may be caused by electrostatic imbalance. This requires shifting the focus of attention from the traditional approach of controlling voltage on a macroscopic scale to managing electric field on a microscopic scale.

One might wonder why focusing on electric field management might lead to a different treatment of electrostatic risk than other approaches, such as those like equipotential bonding that are designed to control electrical potential. After all, electric field is measured in volts per meter, so if voltage is controlled, electric field will be controlled too, no? Intuitively the two approaches might seem to be the same. However, the reason for the fundamental difference can be understood by looking at a graph of field induction between conductive structures on the scale of the features found in reticles and semiconductor devices.

Figure 10 is a graph of computer simulation results showing the electric field and voltage that would be present between two isolated conductors, when exposed to a constant electric field, as a function of their separation. It was produced to help explain the observed effects of field induction in reticles. The simulations show that as the separation of conductors is reduced (as reticle patterns and the structures in semiconductor devices become further miniaturized following Moore's Law) the voltage that is induced between adjacent features by an external electric field rapidly falls, while the electric field concentrated in the gap between them rapidly rises. The effect is highly nonlinear.

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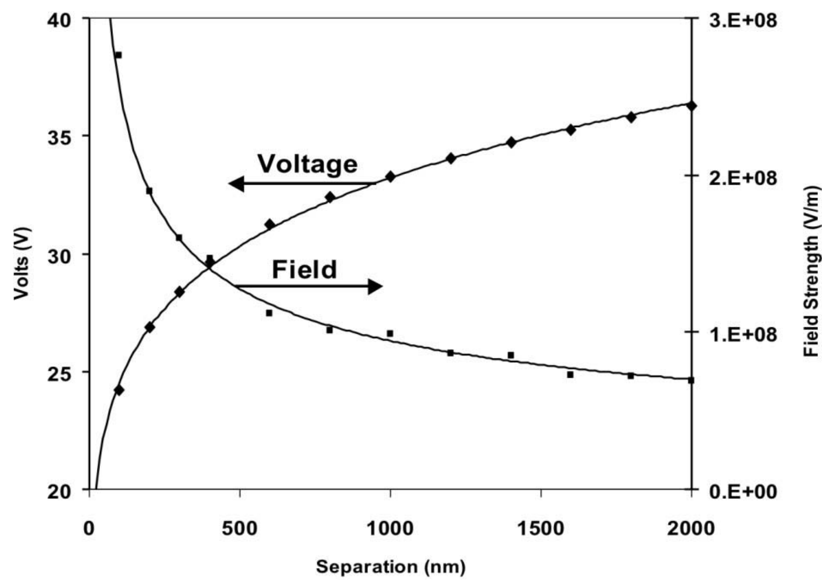

Figure 10: Two-dimensional finite element analysis simulation of the induced potential difference and field strength between two isolated conductive lines as a function of their separation in a constant external electric field.

By the time the separation of conductors reduces to the scale of the structures in semiconductor devices it becomes extremely difficult for an electric field to induce high voltages between them, which many people might believe automatically reduces any risk arising from field induction. However, a high induced voltage is not the stress factor that causes the damage. It can be seen from the graph that on this dimensional scale low induced voltages can be accompanied by very strong electric fields, and this fact is further illustrated by the simulation shown in Figure 11. This computer simulation was produced to show that the guidance published in the ITRS specifying the maximum electric field to which a reticle should be exposed to control ESD risk was actually unsafe when considering the risk of EFM. It shows that on this scale, with only a small fraction of a volt induced between the adjacent conductors, the local electric field strength can be dangerously high. The ITRS guidance was subsequently updated and the figure for the maximum electric field to which a reticle should be exposed was significantly reduced, in recognition of the newly identified risk of field-induced damage.

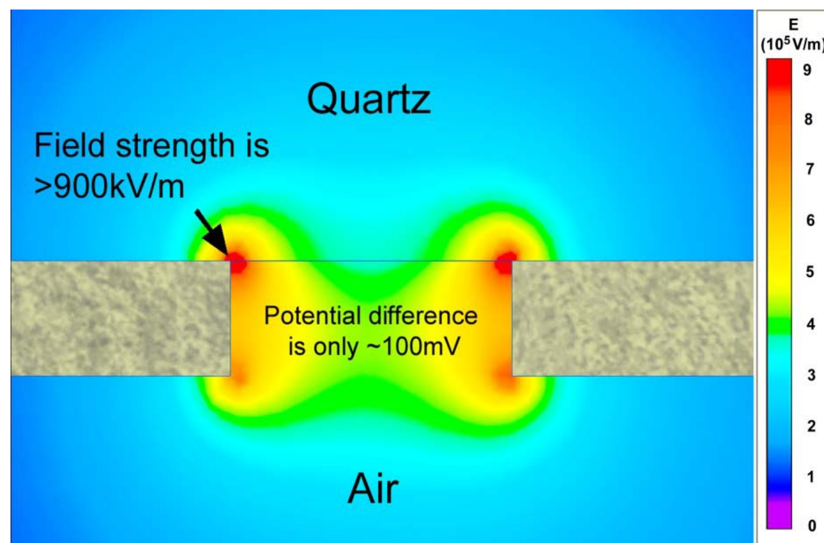

Figure 11: Computer simulation of field induction in a metal-on-glass reticle with a feature separation of 250nm. The concentration of the field at the edge of the line in contact with the quartz substrate produces field strength above 900kV.m^{-1} with a potential difference of only around 100mV induced between the features.

The pursuit of Moore's Law, with the consequent reduction of the separation between isolated conductive elements in a circuit, therefore acts to accentuate any risk from electric field. Having polarizable dielectrics

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present between the conductive features, as in semiconductor devices, would further increase the local electric field strength at any induced voltage by comparison with the situations modelled in Figure 10 and Figure 11. Such points of field amplification, as indicated in Figure 7, are the very locations that would be susceptible to damage by the generation of an excessive local electric field.

It is impossible to measure the potential differences and local electric fields that are induced between different internal parts of a semiconductor device, so one cannot measure this kind of risk directly. It is also practically impossible to simulate field induction effects in such complex three- dimensional structures, so the only way of estimating the risk is to base the risk assessment on what is already known from the study of field induction in reticles. One crucial aspect of this is that grounding through an equipotential bonding program that is principally designed to reduce ESD during material handling accentuates any risk to devices and wafers from electric field.

When considering all the matters that have been discussed, injecting a balancing charge into a semiconductor device or wafer through equipotential bonding, which cannot achieve the intended neutralization but will inevitably create a strong internal electric field, does not seem to be a very prudent thing to do.

VI. Conclusions

It was first shown theoretically and subsequently proven experimentally that using equipotential bonding to prevent ESD during the handling of reticles has negative consequences for the safety of the reticle. Even though equipotential bonding is intended to be protective, is a recommendation given by many electrostatics consultants, and even forms the core of several semiconductor industry patents, it is definitely not protective for reticles. Detailed investigations of damage effects in reticles have revealed that as well as increasing the risk of ESD within the reticle, rather than reducing it, equipotential bonding enhances other field-induced damage mechanisms that until recently were completely unknown. These cumulative damage processes take place under conditions of electric field exposure that are orders of magnitude weaker than those that cause ESD, but their cost implications to semiconductor production are more severe than ESD [16].

Extending this understanding to an assessment of the handling of semiconductor devices leads to the conclusion that equipotential bonding may also have negative consequences for their security. Experimentation to validate the concerns expressed herein has been performed only on a very limited and simplistic scale, but the result shows that concern about this is justified.

Consequently, it is recommended that the extensive experimental research described as being “of interest” by Sonnenfeld should urgently be undertaken, to investigate whether electrostatic damage processes are capable of being enhanced in devices by equipotential bonding - a practice that is universally applied in the semiconductor industry and is presumed to be protective. Even if current semiconductor devices are found to be sufficiently robust to withstand stresses of the kind that have been described in this paper, it does not mean that creating such stress is advisable; neither is it guaranteed that all future electronic, optoelectronic and micro-electromechanical devices would be able to withstand such treatment.

If it is confirmed that significant risk of device electrostatic damage is being created through the use of equipotential bonding, as has been proven to be the case for reticles, this does not create an insurmountable challenge for the semiconductor industry. A methodology for handling extremely electrostatic sensitive (EES) devices without exposing them to increased risk by grounding them through an equipotential bonding scheme has already been described in SEMI Standard E163 [25], and the technology that would be required to implement such a handling scheme is already available.

Further experimental research, and the willingness of the industry to change its way of working if it should be found to be beneficial, are urgently needed in order to assure the future electrostatic security of ESDS and EES devices that are yet to be developed.

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