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Numerical Simulation and Characteriation of Pentacene based Organic Thin Film Transistors with Top and Bottom Gate Configurations

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Abstract- In this paper, we model the characteristics of top and bottom gate configurations of organic thin film transistors (OTFTs) including top gate top contact (TGTC), top gate bottom contact (TGBC), bottom gate top contact (BGTC) , bottom gate bottom contact (BGBC). The path of charge carriers changes in different geometries which possess difference in the electrical behaviour of the devices. The performances of bottom and top gate pentacene based OTFT devices have been analyzed and their performance parameters like mobility, threshold voltage, sub threshold slope, trans conductance, on off ratio have been extracted and compared.

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NUMERICALSIMULATIONANDCHARACTERIATIONOFPENTACENEBASEDORGANICTHINFILMTRANSISTORSWITHTOPANDBOTTOMGATECONFIGURATIONS

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Numerical Simulation and Characteriation of Pentacene based Organic Thin Film Transistors with Top and Bottom Gate Configurations

A. D. D. Dwivedi [α] & Pooja Kumari [σ]

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I. Introduction

Organic electronics is the field which is fast developing in today's scenario. Organic semiconductors (OSC) have made the device low cost and made the field of organic electronics active. Organic transistors can be directly fabricated on flexible cheap substrates and it requires low temperature which makes the device cost efficient. Various researchers used the flexible substrates like glass [1] and plastic [2] which led the fabrication cost very low. Organic thin film transistors have been used in various applications like Organic light emitting diodes (OLEDs) [3], Organic displays [4], Organic radio frequency identification tags [5-23], organic sensors[6-23] and many more high end applications. Several improvements have been made by researchers in geometry, materials, insulators and fabrication to make the device more reliable in performance issues and still it is needed to be improving to implement in basic electronic circuitry.

Numerical simulation is very useful in understanding the sub threshold characteristics and electrical properties of a device which is also helpful in designing of a better model. 2D device simulator like ATLAS from Silvaco international would be suitable for the purpose. In this paper, numerical simulation of the device is done with top and bottom gate configurations to understand how the device behaves physically.

A number of devices with different geometry were implemented in the structure of device and their performance was noted down. Pentacene organic semiconductor was used as an active layer of transistor because of its high mobility. In this paper, we model the characteristics of top and bottom gate configurations including top gate top contact (TGTC), top gate bottom contact (TGBC), bottom gate top contact (BGTC), bottom gate bottom contact (BGBC). The path of charge carriers changes in different geometries which possess difference in the electrical behavior of the devices. The performances of bottom and top gate pentacene based devices are compared and their performance parameters like mobility, threshold voltage, sub threshold slope, trans conductance, on off ratio are summarizing in detail.

II. Experimental Setup

Top and bottom gate configurations of the Pentacene based Organic thin film transistor have been implemented and the schematic of the bottom gate configuration and top gate configuration are shown in Fig.(1) and Fig (2) respectively. For the fabrication of OTFT devices, Layer by Layer (LBL) technique is used in which the materials are evaporated in form of layers one by one.[7] Bottom and top contact structure are differentiated in terms of position of source and drain contacts with respect to active semiconductor layer and keeping gate at constant position. Fig.1. shows the top gate geometry with top contact fig.1 (a) and bottom contact fig.1 (b) used in the simulation.

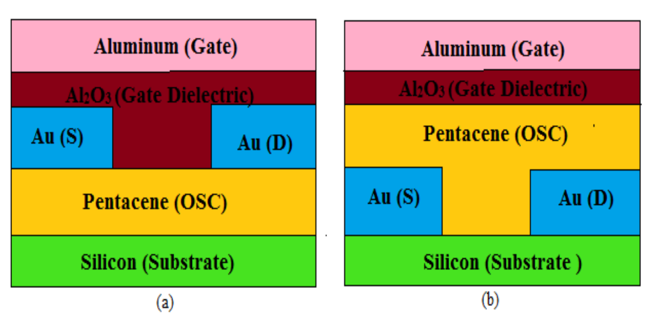

Fig. 1: Schematic of Top gate configuration (a) top gate top contact (TGTC) (b) top gate bottom contact (TGBC)

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Numerical simulation and electrical characterization of the bottom gate and top gate configuration is done in tend to compare the performance parameters with a channel length and width of 10 μm and 220 μm respectively. Organic semiconductor is used as pentacene with doping concentration of 3×10^{17} and with a thickness of 0.03 μm. Al_2O_3 which has permittivity of 8.5 is taken as gate dielectric with thickness of 0.0057 μm. Source and drain contacts and gate electrode are of aluminum(Al) and gold (Au) with thickness 0.03 μm and 0.02 μm respectively. Bottom gate configurations with top contact and bottom contact are shown in fig.2(a) and fig.2(b) respectively. The electrical characterization shows a difference in bottom and top gate geometries due to the unlike path travelled by charge carriers between source and drain electrodes.[8] the structural dimension used in the work for top and bottom gate configurations are summarized in Table I.

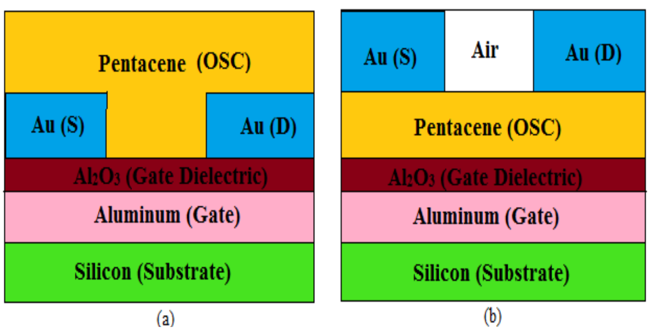

Fig. 2: Schematic of bottom gate configuration (a) Bottom gate bottom contact (BGBC) (b) Bottom gate top contact (BGTC)

Table 1: Structural dimensions used in top and bottom gate configuration

Device Parameter	Value (μm)
Channel Width (W)	220
Channel length	10
Gate thickness. T_G	0.02
Dielectric thickness, t_{ox}	5.7×10^{-3}
Organic semiconductor thickness, t_{osc}	0.03
S/D contact thickness, t_c	0.03

III. Modelling and Numerical Simulation

Numerical simulation of Electrical characteristics of the top and bottom gate configuration is measured using TCAD ATLAS by Silvaco International software. TCAD ATLAS by Silvaco International is physically based, numerical device simulator which predicts the electrical behavior of device and used to design a high performance device. This section describes the simulation procedure followed by ATLAS software. This software follows some fundamental equations that are linked with performance parameters. The equations used by the ATLAS to simulate the Device are Poisson's equation and Continuity equation which were used to measure the characterization of these two devices.[9-23]

a) Poisson's equation

Poisson's Equation relates variations in the electrostatic potential to local charge densities. It is mathematically described by the following relation [9-23],

$$\nabla.(\varepsilon \nabla \psi) = -\rho \tag{1}$$

$$\nabla.(\varepsilon \nabla \psi) = -q\left(p - n + N_d^+ - N_a^-\right) \tag{2}$$

Where ψ is the electrostatic potential, ρ is the local space charge density, ε is the local permittivity of the semiconductor (F/cm), p is the hole density (cm^{-3}), n is the electron density (cm^{-3}),N_d^+ is the ionized donor density (cm^{-3}) and N_a^+ is the ionized acceptor density (cm^{-3}). The reference potential is always taken as the intrinsic Fermi potential for simulations in ATLAS. The local space charge density is the sum of all contributions from all mobile and fixed charges, including electrons, holes and ionized impurities.

b) Continuity Equations

For electrons and holes, the continuity equations are defined as follows:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.J_n + G_n - R_n \tag{3}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla.J_p + G_p - R_p \tag{4}$$

where n and p are the electron and hole concentrations, J_n and J_p are the electron and hole current densities, G_n (R_n) and G_p(R_p) are the generation (recombination) rates for the electrons and holes, respectively and q is the fundamental electronic charge. ATLAS incorporates both eqns. In simulations, but, also gives the user an option to turn off one of the two equations and solve either the electron continuity equation.

c) Transport Equations

These equations are to specify the physical models for electrons and holes current densities and generation (recombination) rates. The Current density equations are obtained by using the "drift-diffusion" charge transport model. The reason for this choice lies in the inherent simplicity and the limitation of the number of independent variables to just three ,ψ , n and p. The accuracy of this model is excellent for all technologically feasible feature sizes. The drift-diffusion model is described as follow:

$$J_n = qn\mu_n E_n + qD_n \nabla n \tag{5}$$

$$J_p = qn\mu_p E_p - qD_p \nabla p \tag{6}$$

where μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the electron and hole diffusion constants, En and Ep are the local electric fields for electrons and holes, respectively, and Δ n and Δ p are the three dimensional spatial gradient of n and p. The local electric fields are defined as follows:

$$E_n = -\nabla(\psi + \frac{kT_L}{q}\ln n_{ie}) \quad (7)$$

$$E_p = -\nabla(\psi - \frac{kT_L}{q}\ln n_{ie}) \quad (8)$$

Where n_{ie} is the local effective intrinsic carrier concentration.

For numerical simulation of OTFT device with top and bottom gate configuration, the Poole–Frenkel mobility model has been employed for Pentacene active channel and defines the dependency of mobility capability due to electric field, this model is expressed as [20-23],

$$\mu(F(x),T) = \mu_{\circ}(T)\exp[\gamma(T)\sqrt{F(x)}] \quad (9)$$

Here, in equation (9), $\mu_{\circ}$ is zero field mobility, F is electric field, and γ is characteristic parameter for the field dependence.

IV. The Density of Defect States

The density of the defect states (DOS) g(E), which dominates the properties of amorphous or polycrystalline TFTs, is modeled as a combination of four components [3] an acceptor-like exponential band tail function $g_{TA}(E)$, a donor-like exponential band tail function $g_{TD}(E)$, an acceptor like Gaussian deep state function $g_{GA}(E)$ and a donor like Gaussian deep state function $g_{GD}(E)$, where E denotes the state energy. The equations describing these terms are given as follows [8]

$$g_{TA}(E) = N_{TA}\exp\left[\frac{E-E_C}{W_{TA}}\right] \quad (10)$$

$$g_{TD}(E) = N_{TD}\exp\left[\frac{E_V-E}{W_{TD}}\right] \quad (11)$$

$$g_{GA}(E) = N_{GA}\exp\left[-\left[\frac{E_{GA}-E}{W_{GA}}\right]^2\right] \quad (12)$$

$$g_{GD}(E) = N_{GD}\exp\left[-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right] \quad (13)$$

where E is the trap energy, E_C is conduction band energy, E_V is valence band energy, and the subscripts T, G ,A, D stand for tail, Gaussian (deep level), acceptor and donor states respectively. The exponential distribution of DOS is described by conduction and valence band intercept densities (N_{TA} and N_{TD}), and by its characteristic decay energy (W_{TA} and W_{TD}). For Gaussian distributions, the DOS is described by its total density of states (N_{GA} and N_{GD}), its characteristic decay energy (W_{GA} and W_{GD}), and its peak energy/peak distribution (E_{GA} and E_{GD}).

Input parameters used in the simulation of the OTFT devices with different geometries are summarized in Table II.

Table 2: Parametrs used during the simulation of top and bottom gate organic tft Devices

Parameters	Values
Effective density of state in conduction band(N_c)	1.0×10^{21} cm^{-3}
Effective density of state in valence band	1.0×10^{21} cm^{-3}
Dielectric constant for Al_2O_3	8.5
Electron gap at 300K	2.8
N_{TD}	1.0×10^{18}cm^3/eV
N_{TA}	2.5×10^{18}cm^3/eV
W_{TD}	0.5eV
W_{TA}	0.129eV
W_{GA}	0.15eV

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W_{GD}	0.15eV
E_{GD}	0.78
E_{GA}	0.62
Doping concentration	$3\times10^{17}cm^{-3}$
Permittivity for Pentacene	4.0
Activation energy for Zero electric field for holes (deltaep.pfmob)	1.792×10^{-2}eV
Hole poole frenkel Factor (betap.pfmob)	7.758×10^{-5} $eV(cm/v)^{1/2}$
Workfunction for Au (S/D)	5.1
Workfunction for Al (gate)	4.28

V. Results and Discussions

All Organic thin film transistor devices were built up with technique of top gate and bottom gate configuration with top and bottom contacts. Electrical characterization and numerical simulation of the devices are measured using TCAD ATLAS by Silvaco International software and with the help of characterization of devices, electrical performance parameters such as Mobility, Trans conductance, threshold voltage, Sub threshold sweep and on/off ratio were calculated.

Mobility is the rate of flow of charge carriers in the electric field. It is the parameter which deals with processing speed of device. This mobility (μ) has been calculated using the following equations,

$$\mu = (L \times g_m) / (W \times C_{ox} \times V_{ds}) \qquad (10)$$

$$g_m = dI_{ds} / dV_{gs} \qquad (11)$$

$$C_{ox} = \varepsilon_{ox} / d_{ox} \qquad (12)$$

Here, g_m is the trans conductance which is calculated by transfer characteristics curve (I_{ds} /V_{ds}) and calculation is done by equation (11). L and W are length and width of device respectively. C_{ox} is the capacitance of oxide with is the ratio of permittivity of oxide and thickness of oxide, given by equation (12).V_{ds} is drain voltage which is taken as 1V for all the devices.

Minimum voltage required for the device to be in ON state or the accumulation of charge carriers at gate dielectric-semiconductor interface is said as Threshold Voltage or Cut-in Voltage. Sub threshold sweep is ratio of change in gate biasing to change in logarithm scale of drain current. It can be expressed as,

$$SS = \partial V_{gs}/\partial \log_{10} (I_{ds}) \qquad (13)$$

a) Top gate configuration

Fig. 2 (a) and (b) shows the output and transfer characteristics of top gate top contact configuration top gate bottom contact configuration. At high operating gate voltage, linear and saturation region are expect in the thin film transistor and the same is observed in the output graph for Top gate configuration at top contact and bottom contact. Similar characteristics behavior is also observed in am bipolar organic TFT reported in [10]. Figure 2(a) is the comparison of top gate top contact and top gate bottom configuration which tend to gain better characteristics in top gate top contact than top gate bottom contact.

Transfer characteristics shows a good electrical performance with good electrical parameters with higher on-off ratio greater than 10^5 and sub threshold sweep of 0.11 in top gate bottom contact and 0.02 in top gate top contact shown in fig. 2(b).

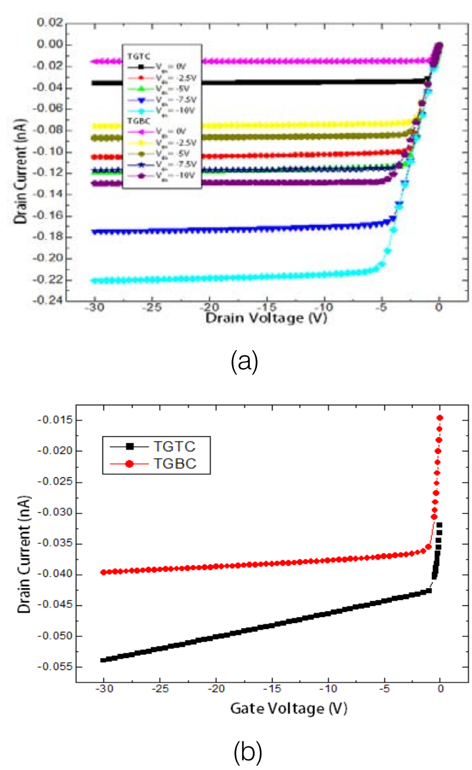
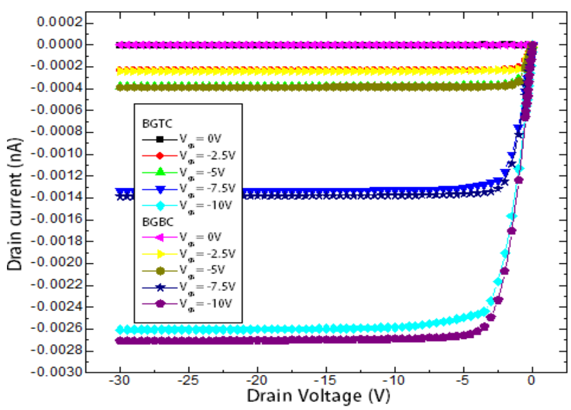


Fig. 2: (a) Output (b) Transfer characteristic curve (V_{ds} = -1V) of OTFT in TGTC and TGBC configurations

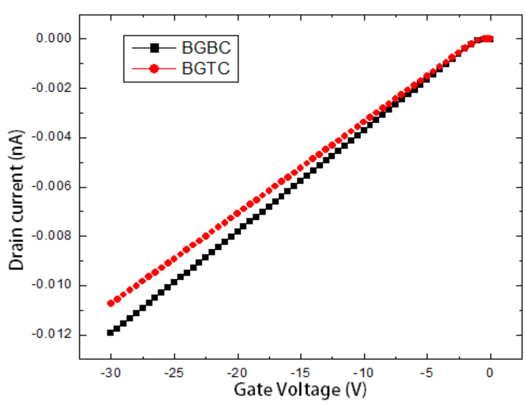
b) Bottom gate configuration

Fig. 3(a) and (b) inset shows the output and transfer charactistics of bottom gate configuration with bottom contact and top contact respectively. It is observed that both the BGBC and BGTC configurations have same output characteristics at low gate voltage ($V_{gs} \leq 5V$) but if the gate voltage is high ($V_{gs} > 5V$) it shows a drastic increment in the output characteristics which is grater in Bottom gate bottom contact than bottom gate top contact configuration.

Transfer characteristics shows good performance characteristic with linear increment at drain voltage of -1V with higher on off ratio greater than 10^3 and sub threshold slope of 0.26 in BGBC and 0.32 in BGTC configurations. All the extracted values of electrical parameters are tabulated in table III.



(a)



(b)

Figure 3(a): Output (b) transfer charactristics curve (at V_{ds} = -1V) of OTFT in BGTC and BGBC configuration

Table 3: Extracted Values of parameters ot top and Bottom gate configuration in organic thin film transistor

Parameters	Structures			
	BGBC	BGTC	TGBC	TGTC
V_t (V)	1.1	1.2	0	0
On off ratio	1.9×10^4	9.5×10^3	1.9×10^8	7.9×10^8
Sub threshold slope(V/dec)	0.26	0.32	0.11	0.02
Transconductance (μS)	4.13×10^{-6}	3.759×10^{-6}	6.62×10^{-7}	3.73×10^{-6}
Mobility(cm^2/vs)	0.14	0.129	0.022	0.128

From above calculation, it was observed that bottom gate configuration perform better than top gate configuration in terms of mobility, sub threshold slope and with good on off ratio but top gate configuration have higher on off ratio as compared to bottom gate configuration which is in magnitude of 10^8.

VI. Conclusion

This paper presented the numerical simulation and characterization of bottom and top gate pentacene based OTFTs. The performances of these devices have been analyzed and their performance parameters like mobility, threshold voltage, sub threshold slope, trans conductance, on off ratio have been extracted and compared. It was observed that bottom gate configuration perform better than top gate configuration in terms of mobility, sub threshold slope and with good on off ratio but top gate configuration have higher on off ratio as compared to bottom gate configuration which is in magnitude of 10^8.

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