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Thermal Stress Analysis of BGA Packaging Structure

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THERMALSTRESSANALYSISOFBGAPACKAGINGSTRUCTURE

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Thermal Stress Analysis of BGA Packaging Structure

Tasneem Khan Shifa[α] & Dr. Md. Faruque Hossain[σ]

Abstract- In this paper the performance of the ball grid array (BGA) electronic packaging is investigated. The fields of temperature and stress are analyzed for the overall model & for solder balls by finite element method (FEM) using COMSOL Multiphysics 5.2a soft ware to analyze different aspects to improve the reliability & efficiency of integrated chip. The simulation result shows that the maximum value of temperature and thermal stress are 41 degree Celsius &199MParespectively.The maximum temperature is obtained on the chip surface and the maximum stress happens on the outside corner of the ball joints. The range analysis shows that the maximum stress increases with the increase of chip thickness, substrate width, ball pitch, CTE but the value of maximum stress decrease with the increase of ball diameter and Poisson's ratio.

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I. Introduction

In recent years, the volume of a new developed electronic device has reduced by more than three orders of magnitude compared with several years ago. Thus, it is very important to research an efficient electronic packaging form to improve the efficiency and reduce the cost [1]. The electronic packaging technologies have developed to control a large amount of heat that is generated through the integrated circuit (IC) and match the coefficient of thermal expansion (CTE) between different parts of packaging materials. Among various advanced forms of packaging, ball grid array (BGA) becomes one of the most promising packaging technologies due to its higher efficiency, smaller geometry size, lower cost [2]. However, among all the factors leading to the failure of the electronic device, such as vibration, humidity, loading& temperature affects mostly.

Furthermore, because electronic packaging consists of different CTE materials, the thermal stress emerges during the working cycle due to the expansion between adjacent materials which fails the products. Therefore, it is necessary to find appropriate materials combination to lower the thermal stress. To guarantee the stability of integrated chip, the packaging material should have characteristics like strength and stiffness to prevent stress deformation and other features such as high gas tightness, low density, radiation protection and low Cost [3].

A significant number of literatures are published about the BGA packaging. Luo [4] developed an analytical thermal resistance network model to calculate mean die temperature of a typical BOA packaging which is demonstrated to be accurate in predicting the temperature distribution. Z. Sauli, V. Retnasamy, R. Vairavan, K. Anwar, and N. Abdullah [5] analyzed the stress response of BGA solder with the different material during maximum vertical loading using the simulation method. The results showed that the Normal BGA demonstrated a higher stress response. Q.Gao, K.K. Wang [6] studied the thermal field and stress field distribution when chip worked on a given power. The results showed that the influence on the temperature and stress decreased with the increasing heat convection coefficient. K.K. Wang, L. Wang, L. Wang, Y.Z. Wang [7] studied the influence of different materials and boundary conditions on the temperature distribution. The results showed that the packaging temperature rose up faster at the beginning of the simulation than that at the end and high convection significantly reduced the maximum temperature. Also, adhesive thickness had an impediment on heat transfer due to the package temperature slightly rose as the thickness of adhesive increases. S.F. Popular [8] studied the reliability of flip chip BGA package based on the finite element method (FEM) parametric analysis. L.L. Mercado, V. Sarihan, Y.F. Guo, and Mawer [9] applied FEM parametric analysis to study the reliability of flip chip BGA, and the design parameters including solder bump layout, solder bump center to die edge, solder material/geometry, die size as well as substrate size/material. W. Chen [10] investigated the test methodology for assessing reliability performance of both single chip BGA& multiple chips flip-chip BGA on board assemblies. B. Rosner, J. Liu, and Z. Lai [11] developed a thermal cycle testing experiment for the flip chip BGA packaging &a daisy chained test IC was designed for the packaging reliability testing.

The fields of temperature and stress are analyzed for the overall model & for solder balls by finite element method (FEM) by COMSOL Multiphysics 5.2a software.

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II. Background

a) Pin Grid Array

Pin grid array (PGA) is a package with one face covered with pins is in a grid pattern. It is placed in a printed circuit board (PCB) and carry out electrical signal between integrated circuit & printed circuit board (PCB).PGAs are often mounted on printed circuit boards using the through hole method or inserted into a socket [12].

b) Ball Grid Array (BGA)

A ball grid array (BGA) came from the Pin grid array (PGA) in which there are pads instead of pins on the bottom of the package and a tiny solder balls stuck to each of the pads. The device is placed on a PCB with copper pads in a pattern that matches the solder balls. The assembly is then heated which melts the balls & the melted solders hold the package with the circuit board. Then the solder cools down and solidifies& forms soldered connections between the device and the PCB [13].

III. Experimental Procedure

a) Finite Element Method (FEM)

The finite element method (FEM) is the dominant discretization technique in structural mechanics. To deal with a large problem, it subdivides a large problem into smaller, simpler parts that are called finite elements. The simple equations are used to model these finite elements and they are then assembled into a larger system of equations that models the entire problem.

b) Geometry Model

A typical 3-D model BGA structure with 16 solder joints with the diameter 0.3 mm are placed on the substrate and connect the electronic chip & one-quarter model is imported into simulation software COMSOL Multiphysics 5.2a to reduce the calculating time. Figure 1 shows the model,

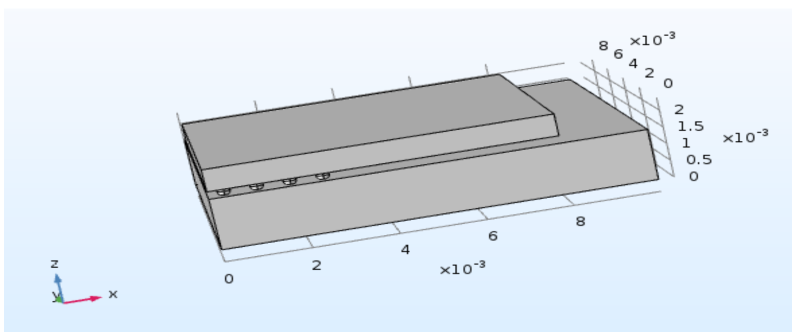

Figure 1: Simplified quarter BGA model

Table 1 shows a comprehensive geometry size of BGA,

Table 1: BGA Dimension

Component	Size (mm)
Chip	8×8×0.65
Ball Grid	0.3
Substrate	10×10×1.5

c) Meshing

The BGA model meshed with 7318 number of domain elements shown below,

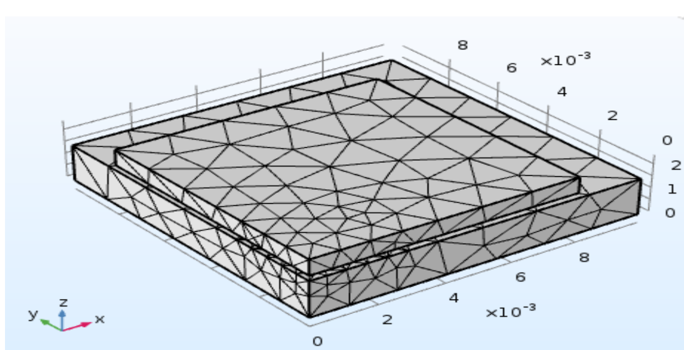

Figure 2: The mesh result of the BGA model

d) Chosen Material & Parameters

Materials used in the BGA mode were homogeneous and isotropic, they were adhesive to Each other & pre-stress between them was ignored. The following table 2 shows the material parameters.

Table 2: Material Parameters

Component	Chip	Ball grid	Substrate
Material	Si	Sn-Pb	Epoxy
Thermal Conductivity (W/m.K)	120	30	0.2
CTE	2.6	24.5	18
Poisson's ratio	0.28	0.35	0.38

The environment temperature is 25 °Cand the power of the chip is 0.2 Watt. The convective heat coefficient between the chip and substrate is 10W/(m^2.k) [14]. The thermal stress analysis is conducted on the base of the thermal results obtained above.

IV. Simulation & Result Analysis

a) Temperature Field

Figure 3 shows the temperature distribution of BGA model. It indicates that the maximum temperature is on the surface of the chip and the minimum temperature is on the substrate. The heat generated by the chip transfers to the substrate via the solder joints. Also, the heat also dissipates to the surrounding environment. Finally, a steady state is found.

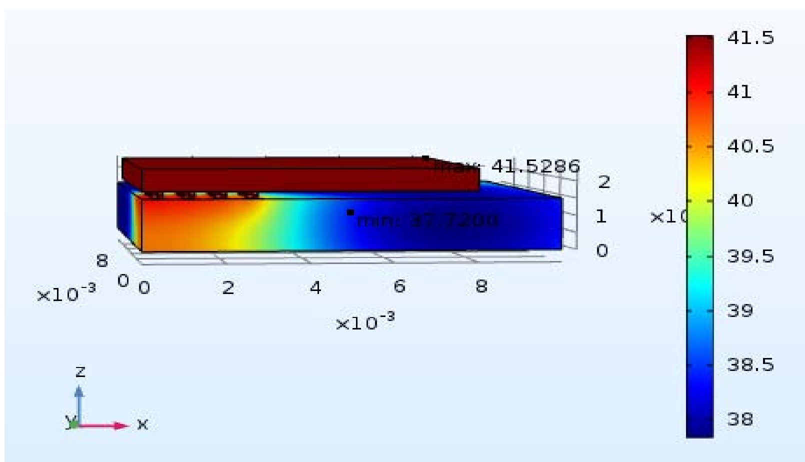

Figure 3: Temperature distribution in BGA

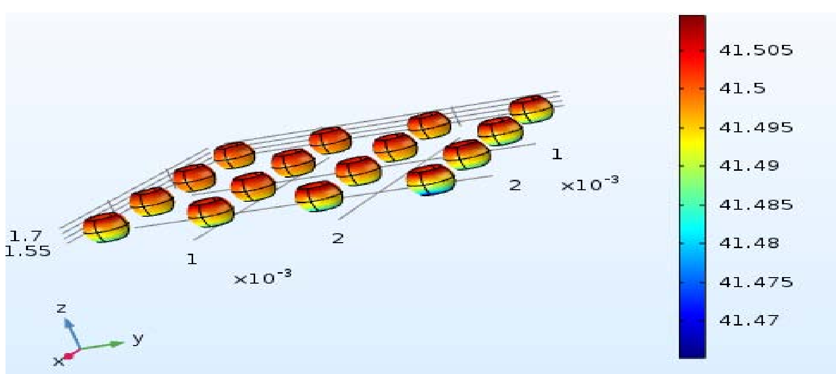

Figure 4: Temperature distribution of solder joints

In figure 4, it is seen that among all the sixteen ball grids, the ball grid farthest away from the center has the maximum temperature at the top surface and the minimum one at the bottom surface. So, this temperature difference makes it easier to produce defects like fatigue and cracks.

Figure 5 shows the temperature distribution of the substrate,

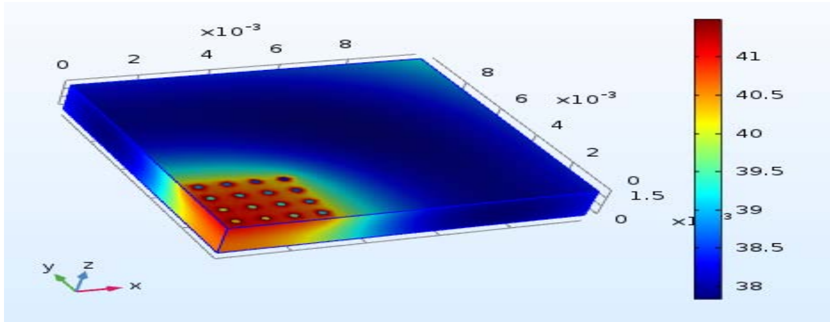

Figure 5: Temperature distribution of the substrate

From figure 4&5, it is seen that the maximum temperature of both ball grid array, chip & substrate reaches the maximum value at the corner far away from the center area because of the more heat dissipation via the solder joints, making the lower temperature at the center.

b) Thermal Stress Field

Figure 6 &7 shows the overall von misses stress distribution of BGA,

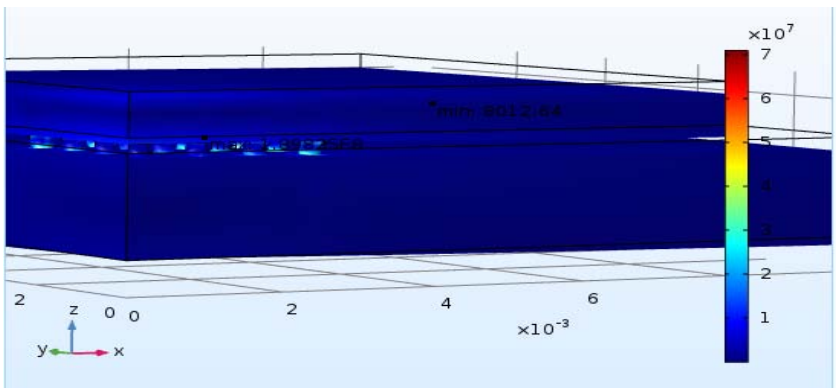

Figure 6: Von Mises stress field in BGA

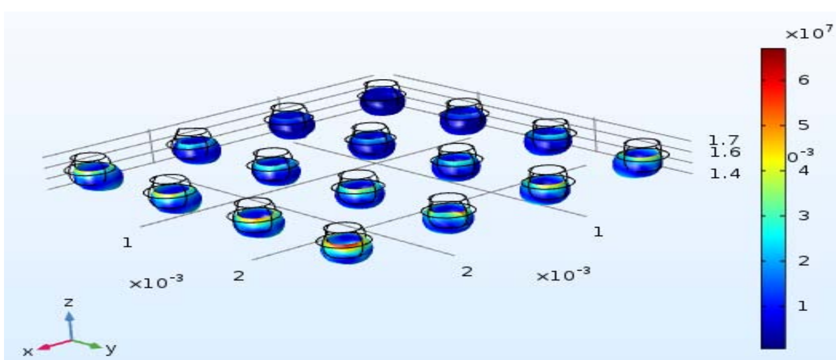

Figure 7: Von Mises field of solder balls

From figure 6, the maximum stress happens on the outside corner of the ball joints because of heat dissipation. From Figure 7, the solder joints have the highest stress value due to the higher thermal expansion coefficient than the substrate & the chip and the maximum & highest displacement of the solder joints happens in the same place with the maximum stress [14].

The maximum value of temperature and thermal stress are 41 degree Celsius & 199MPa respectively.

V. Factors Influencing Thermal Stress

Maximum stress plays a significant role in affecting the reliability and efficiency of BGA packaging. Various factors were considered for optimization.

a) Influence of Ball Pitch

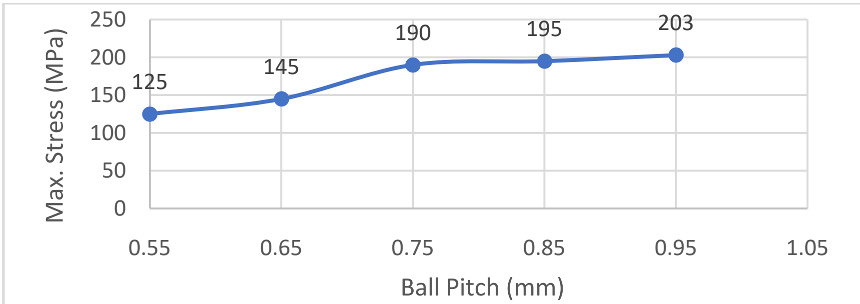

Figure 8: Influence of max. stress as a function of ball pitch

b) Influence of Chip Thickness

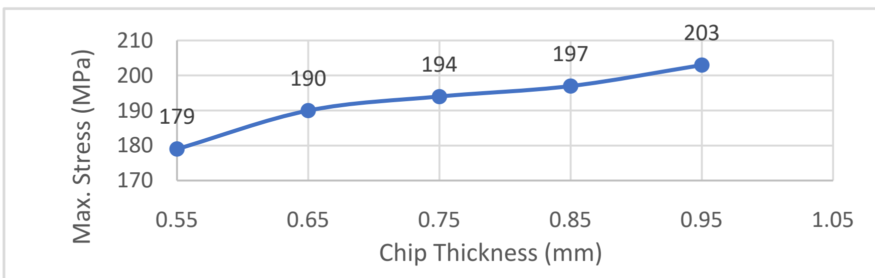

Figure 9: Influence of max. stress as a function of chip thickness

c) Influence of Substrate Width

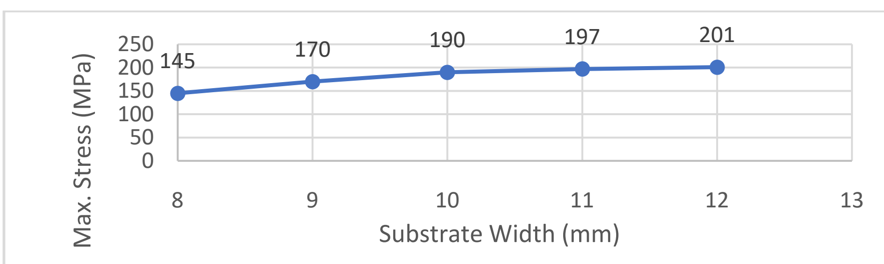

Figure 10: Influence of max. stress as a function of substrate width

In figure 8, 9 & 10, it is observed that with the increasing values of ball pitch, chip thickness& substrate width maximum stress increases because as value increases more heat is dissipated& heat transfers from chip to substrate via solder balls. Thus, temperature difference gets higher.

d) Influence of Ball Diameter

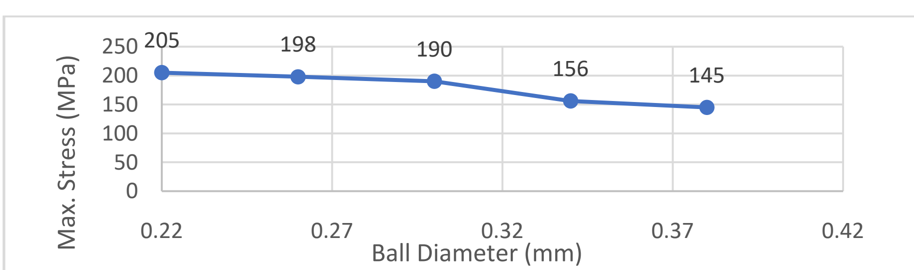

Figure 11: Influence of max. stress as a function of the ball diameter

Figure 11 shows that for higher values there is a notable decrease in maximum stress. With the ball diameter of solder balls getting larger, more heat is generated at chip & more heat is dissipated from chip to substrate through solder balls.

e) Influence of Poisson's Ratio

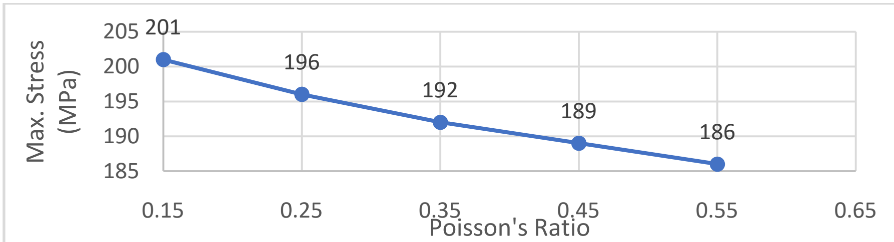

Figure 12: Influence of max. stress as a function of Poisson's ratio

Figure 12 shows that as the value of Poisson's ratio of solder balls increases, maximum stress decreases. Because for any given temperature distribution the thermal stresses are directly related to the Poisson's ratio.

f) Influence of Coefficient of Thermal Expansion

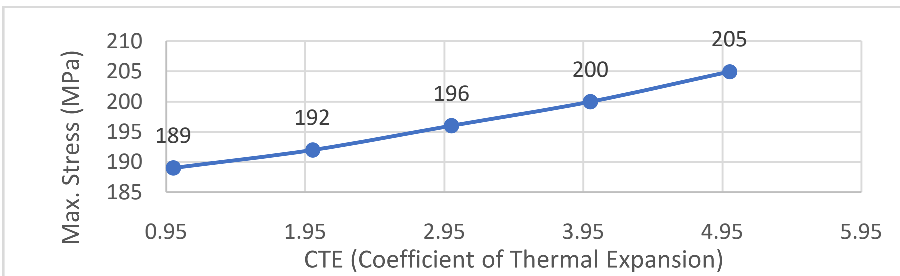

Figure 13: Influence of max. stress as a function of a coefficient of thermal expansion

From figure 13, it is observed that with the values of CTE increases, more heat is dissipated & maximum stress gets higher because heat dissipation increases exponentially with coefficient of thermal expansion.

The decreasing of the stress and temperature has a positive effect on the reliability & efficiency of BGA packaging. So, based on these values minimum stress can be obtained with a new series of parameters.

Several conclusions can be summarized as follows in the table:

Table 3: Results of factors range analysis

Ball pitch (mm)	0.55	0.65	0.75	0.85	0.95
Max. stress (MPa)	125	145	190	195	203
Ball diameter (mm)	0.22	0.26	0.3	0.34	0.38
Max. stress (MPa)	205	198	190	156	145
Chip thickness (mm)	0.55	0.65	0.75	0.85	0.95
Max. stress (MPa)	179	190	194	197	203
Substrate width (mm)	8	9	10	11	12
Max. stress (MPa)	145	170	190	197	201
Poisson's ratio	0.15	0.25	0.35	0.45	0.55
Max. stress (MPa)	201	196	192	189	186
CTE	0.96	1.96	2.96	3.96	4.96
Max. stress (MPa)	189	192	196	200	205

VI. Conclusion

In this paper, the typical BGA packaging is modeled and simulated using COMSOL 5.2a Multiphysics. Several conclusions are summarized as follows:

a) The maximum temperature is found on the chip surface. The maximum stress happens on the outside corner of the ball joints. The maximum value of temperature and thermal stress are 41 degree Celsius & 199MPa respectively.

b) The maximum stress increases with the increase of chip thickness, substrate width, ball pitch, CTE but the values of maximum stress decrease with the increase of ball diameter and Poisson's ratio.
c) Considering different values for different factors of BGA geometry structure, it is observed that the geometry size of the substrate & chip and different material parameters of solder balls plays a significant role in influencing the temperature and thermal stress.

In future work, by using these different factors, a standard BGA model can be designed where maximum stress can be lowered and also can be more reliable and efficient.

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