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Robustness Evaluation Study of Power RF LDMOS Devices after Thermal Life Tests

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I. Introduction

Lateral diffused metal-oxide-semiconductor (LDMOS) have been widely used in many smart power applications. Also on base stations, TV broadcast or in radar applications with high capabilities particularly in terms of RF, output power and Power Added Efficiency (PAE). These applications can cause damage and limiting factors to device reliability, especially to the gate oxide of MOS devices [1,2,3]. Quite often accelerated life tests of MOS capacitors are performed by applying a high constant voltage at the gate contact (constant voltage stress: CVS) or by injecting a constant current across the oxide (constant current stress: CCS) over a period of time. They produce electrical instabilities which have been the subject of numerous experimental studies in MOS devices [4,5]. Current is a more effective parameter than voltage for defect detection in MOSFET devices and CMOS ICs, although both are necessary for complete testing.

Problems related to oxide degradation are of increasing concern for the development of MOS technology. The leakage current represents one of the most important issues of oxide reliability, especially for MOS applications [6]. The leakage current with temperature can contribute to the thermal runaway of device [7]. Many papers have been devoted to the study of leakage current and its relation with device lifetime [6,8]. Leakage current in a MOSFET can be a significant contributor to power dissipation [9]. A small amount of leakage current is always present, even in healthy devices. The maximum allowable leakage current in a MOSFET is the manufacturer specified zero-gate-voltage drain current (I_{DSS}) and gate body leakage current (I_{GSS}). I_{DSS} is the current flowing between the drain and the source when the gate and source are at the same potential. I_{GSS} is the current flowing between the gate and the source when the source and drain are at the same potential.

An electrical stress can produce an increase of the low field leakage current across thin gate oxides, further reducing the lifetime of devices [8]. Failures that are precipitated by excessive leakage currents include junction and dielectric failures [9]. Which consist of leakage through the oxide layer leading to destruction of the dielectric film. Therefore, the leakage current can reach the semiconductor surface and may lead to degradation of the electrical properties of the transistor [9]. It is required to study the hot electron induced performance degradation of MOS transistors. In order to qualify new power RF LDMOS reliability for radar applications, a 3000 h pulsed RF life test has been conducted on a dedicated RF S-band test bench in operating modes [11].

This work presents a degradation study to the properties and various mechanisms of thin gate oxides, based on the electric characterization of leakage current increase on power MOSFET transistor behaviour after new experimental accelerated ageing tests under various conditions. The content of this paper is presented as follows: the section 2 describes the life test bench and the general power RF LDMOS transistor performances. The discussion of simulation and experimental results are shown in Section 3. The conclusion and prospects are given in Section 4.

II. Experimental Setup Of Ageing Test Bench And Simulation Process

Recently, the characterization, optimization, and reliability of power RF LDMOS devices have drawn much attention [12,13]. For this purpose, we designed

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and implemented an innovative reliability bench able to keep track of all RF powers, voltages and device base-plate temperatures whose values correspond to stress operating conditions [14].

This bench is able to keep track many parameters like voltages, currents, base-plate temperature, and peak power. Eight devices is the bench capacity to be tested simultaneously in order to keep it easy to manage. The Fig. 1 and Fig.2 represent the component under test placed on its test fixture, supplied by DC power and connected to RF connector (type N). The conditions of pulsed RF life test are much closed of radars applications with operating 24h/24h.

The bench consists of three interdependent subsets:

* a microwave part,
* a control/command part piloted by PC,
* thermal module for each devices.

The microwave part essentially allows the power injection and measurement in every branch for each device. Each branch contains a tuner to set precise output VSWR stress on any of the devices. The command/control system ensures the achievement of the following functions:

* biasing voltage supply and current measurement tracking,
* separate control and measurement of each device temperature,
* power switching between the eight devices branches,
* safe data record.
* The measured data on each branch are the following:
* input, output and reflected power,
* output power variation in RF pulse ,
* device biasing current,
* temperature.

All data necessary to keep track of each device degradation evolution in real time are secured thanks to the rack. Life-tests are run in the working conditions (pulsed RF) using various device base plate temperatures (10°C, and 150°C) and a high drain–source voltage (44 V) in order to get more power from the device for radar applications.

The RF transistors (8 samples) have been submitted during 3000 hours to ageing test on the reliability bench. This bench operates in radiofrequency pulse mode. During the life test, the goal is to study the component performances in actual working situation to ensure that it will maintain a good performance level. The device under test is placed on a thermal module in order to maintain a constant flange temperature. The command unit manages DC supply voltage, temperature regulation and RF signal monitoring.

The picture of 50Ω-matched test fixture on thermal support using the Peltier effect for power LDMOS amplifier in S-band radar application.

The component is in centre of support of test specifically designed for operation at full power in pulsed mode (2.9 GHz and 44 V). These values (frequency and tension) are particularly high compared to nominal values given by the manufacturer (2.2 GHz under 26 V). The power RF-LDMOS device under test is a commercial telecom dedicated transistor (encapsulated in a 2-lead flange package with a ceramic cap) S-band operating in class B at saturation and 65 V DC biasing. Indeed, these performances are given in conditions of width pulse 500 μs with a duty cycle of 50%. The gate length is equal to 0.8μm.

The Power density is equal to 1.89 W/mm. More than 61% of drain efficiency, and a gain More than of 11 dB can be obtained around the S band frequency at 2200 MHz in a common source test circuit. The junction temperature does not exceed 150° C for a flange temperature equal to 65° C. The thermal resistance is 0.2 C/W.

A modified structure of RF power N channel LDMOS, previously developed by Raman et al [15], was implemented and simulated using the physical simulator Atlas of Silvaco [16]. Fig. 3 shows the device's structure with approximate doping wells. The main geometrical and technological parameters are given in Table 1. The implemented structure is typically similar to our tested device. Consequently the qualitative understanding of physical phenomenon will be studied. The suggested structure has a Gaussian doping profile along LDD and channel surface. The doping profile was optimized using a technological process simulation carried out by SSUPREM3 [16], see Fig. 3.

III. Results And Discussion

The bench allows to record temperature, currents and voltages (gate and drain), the input power, reflective and output powers. After RF life-tests, the degraded device under test was characterized at ambient temperature, and then a parameter set is extracted.

The current I_{ds} measured is average and in order to have the correct peak current, the duty cycle is needed on the expression of DE. During all the life tests, threshold voltage V_{th}, drain-source current I_{ds} and feedback capacitance C_{rss} are shifted. We can partially conclude that these three DC critical parameters are affected by the RF life test. The increase of the V_{th} was detected and it presented a good correlation with the I_{ds} slump (decrease of the I_{ds} corresponded to increase of the $R_{ds\text{-}on}$). The shift after and before life tests of device threshold voltage V_{th} is presented in fig.4. An interpretation is proposed to explain the discernable change observed on the feedback capacitance, once again more noticeable at 10°C. The C_{rss} at zero drain-source bias is reduced from 2.6pF to 1.8pF at 10 °C, indicating a shift of 30%. Even at 26V bias, the C_{rss} is reduced from 0.43pF to 0.34pF (shift 21%), see fig.5.

Fig. 6 displays changes of S-parameter (S_{21}) before and after RF life-tests at 10°C and 150°C. The gate–source voltage for S-parameters measurement was 4.7 V, and the drain–source voltage was 28 V. The devices are operated in the saturation region. Ideally the I_{GSS} value would be zero for voltage levels that are less than the voltage required to reach the dielectric strength of the gate oxide. In the data sheet the value is less than 40 nA (Table 2). Fig.7-a shows the gate leakage current (I_{GSS}) measured of three samples power RF LDMOS before ageing test.

Overstressing the gate either periodically with RF or statically with DC can also cause an increase of I_{GSS} and thus degrades device performance with respect to RF power gain. Fig.7-b shows the increase Gate leakage current (I_{GSS}) measured of three samples power RF LDMOS after ageing test but still far from the total limit of device failure. I_{GSS} due to many factors that are related to the integrity of gate oxide and surrounding regions. I_{GSS} can be used to evaluate reliability of this integral component of the MOSFET. Increase of this parameter with a particular device stress can be used to extrapolate the mean time failure (MTTF) of the gate oxide [12]. Other considerations for the gate oxide include careful electrostatic-discharge (ESD) precautions since the gate oxide is easily damaged [12].

A higher junction temperature will increase the leakage current [9,10] which may lead to thermal runaway phenomenon [13]. The electrical parameters are shown in Table 2, in which the measured and the manufacturer's data sheet values of the power MOSFET are compared.

The breakdown voltage as per the manufacturer's data sheet (Vgs=0; I_{ds}=0.2mA) is higher than 75 V. The value of this voltage $V_{(BR)DSS}$ was found 86 V in the case virgin and 81 V after ageing. I_{DSS} include minority carrier injection from the source due to carriers overcoming the energy barrier resulting from surface band bending and also from sub-critical avalanching caused by high electric fields due to a non-ideal body as well as the Laterally-Diffused-Drain (LDD) doping profile [12].

After accelerated RF pulsed life test, the degradation of leakage current can be explained by the increase of V_{th} and C_{rss}. These parameters are degraded due to the interface state generation after stress, device performances should be degraded due to the same degradation mechanism. This indicates that the performance degradation is mainly due to the hot carrier induced interface state generation [17,18]. The Miller capacitance C_{rss} is composed of two parts, the oxide capacitance (C_{OX}) and the drift region capacitance (C_{SI}) [19].

The electric parameters of MOS transistor are more and more sensitive to defects bound to the presence of charges in the gate oxide and at the Si/SiO_2 interface [10].

The origin of the observed shift could be related to the presence of very high electric field, which increases carrier injection into the grown silicon dioxide layer (SiO_2) and into interface state Si/SiO_2 [10,19]. The detail of the lateral electric field distribution of the active silicon layer in channel and drift regions is shown in Fig. 8.

The hot carriers produce an additional interface trap density and trapped electron charge which results in a build up of negative charge at Si/SiO_2 interface [20]. This negative charge attracts holes depleting the negative charge in the power LDMOS N-drift region and by consequent increasing the $R_{ds\text{-}on}$ device resistance. Hence, $R_{ds\text{-}on}$, C_{rss} and I_{dsat} variations are more remarkable at 10°C, due to the fact that the maximum impact ionization rate is located near the gate edge, see Fig. 9.

The aggressive gate leakage current due to the carrier direct tunneling has become as ultimate limit for gate oxide down scaling [6]. The RF performances are not stable during all 3000 h the life test; we see a variation of I_{ds}. This variation affects the RF performances. According to the literature [19,20], the most probable cause of degradation for power RF LDMOS technology is attributed to hot electron-induced interface state generation and/or impact ionization. May be state interface Si/SiO_2 between drain and gate are responsible of this phenomenon. In order to explain this behaviour, the characterisation of these defects should be investigated. Particularly, the distribution of the data in the figures shows that the aging of the transistor is relatively dependent of the temperature.

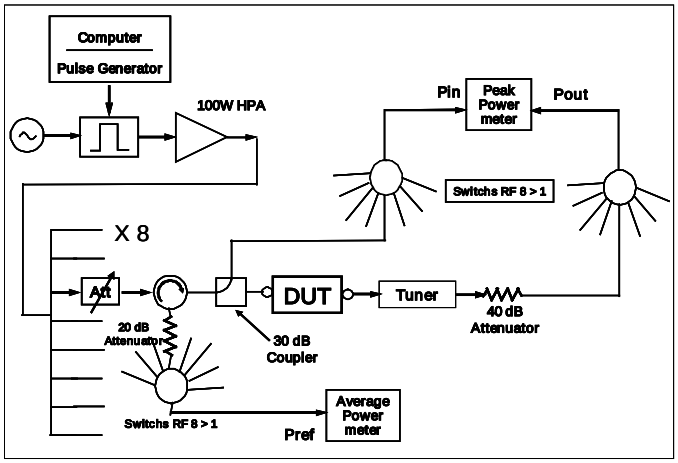

Fig. 1: Synoptic of a RF pulsed life test bench

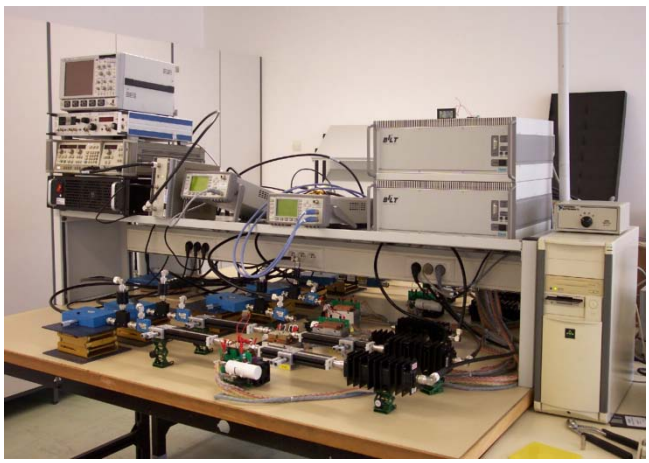

Fig. 2: Photography of the RF pulsed life test bench

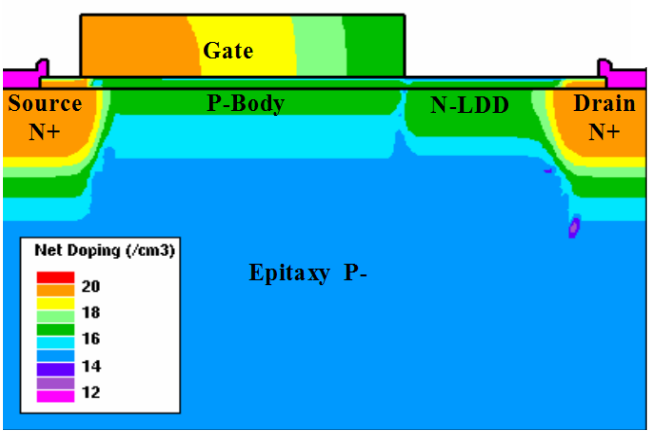

Fig. 3: Cross-section view of power RF N-LDMOS device with Net doping profile along silicon surface implemented in Silvaco-Atlas

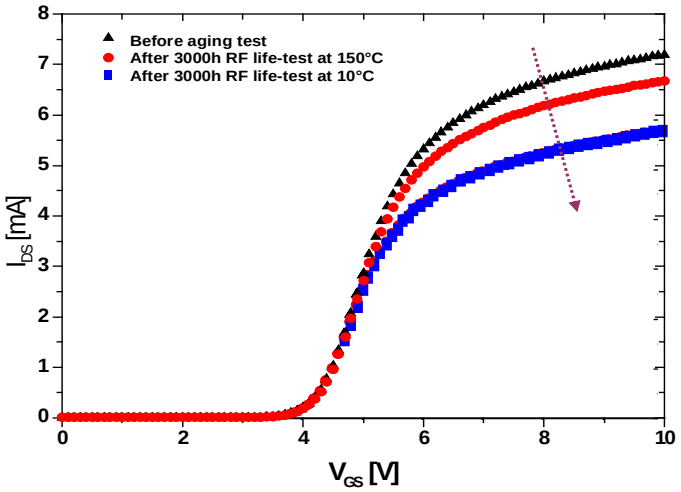

Fig .4: V_{th} evolution before and after ageing RF Life tests with V_{DS}=10mV

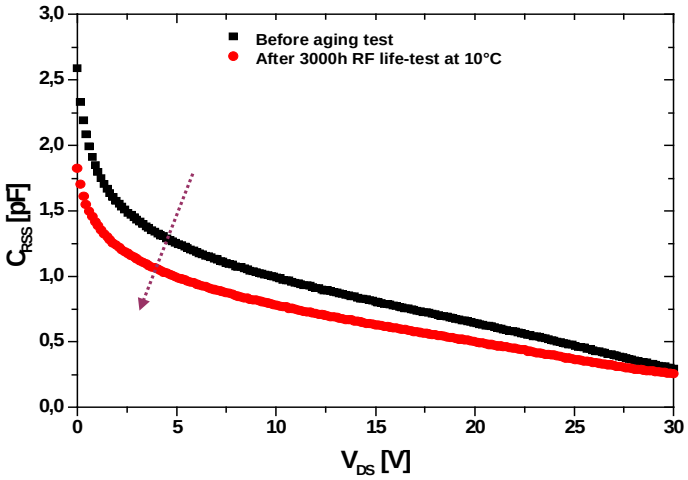

Fig. 5: C_{RSS} profile before and after 3000h RF Life test (10°C) with Freq=1MHz

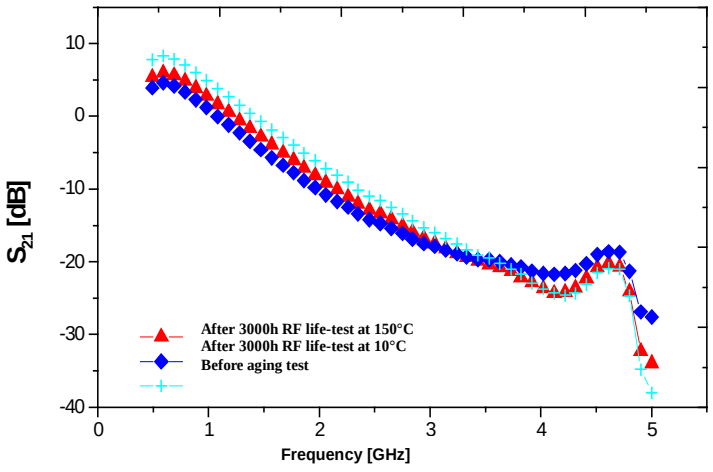

Fig. 6: S-parameter (S_{21}) degradations of the power RF LDMOS before and after RF Life-test, with V_{ds}= 28V, V_{gs}=4.7V and Freq=[0.5GHz, 5GHz]

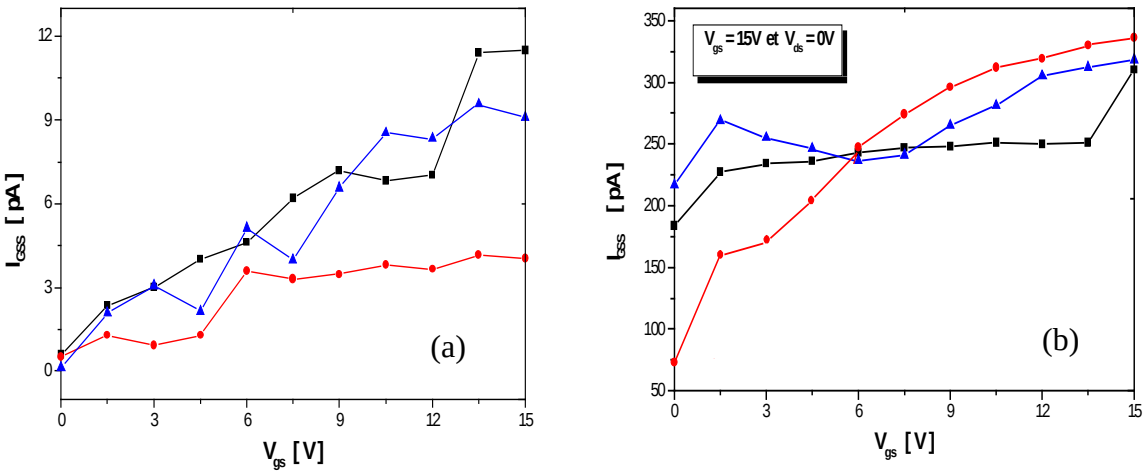

Fig. 7: Variations of Gate leakage current (I_{GSS}) measured of three samples power RF LDMOS before and after ageing test

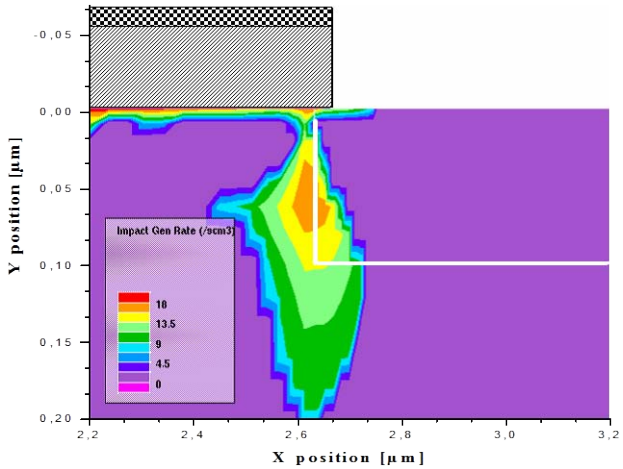

Fig. 8: Simulated impact ionization rate distribution, at bias conditions (Vds = 44 V and Vgs = 3.8 V)

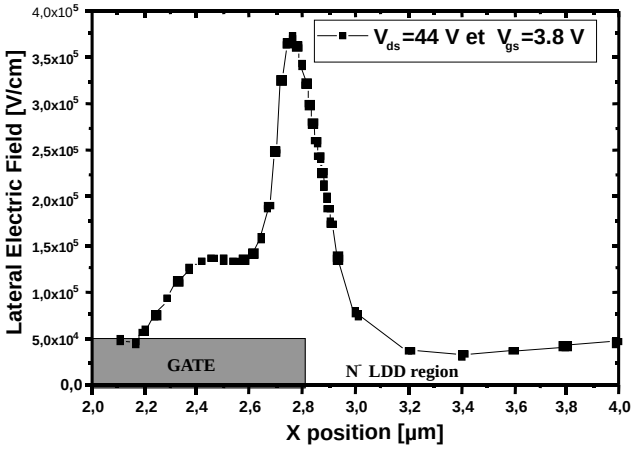

Fig. 9: Lateral electric field distribution in power N-LDMOS structure, with Vds=44V and Vgs=3.8V bias

Table 1: Device dimensions

Parameter	Value (μm)
Source length	1.1
Source-gate spacing	1
Gate length	0.8
Gate-drain spacing	3
Drain length	1.1
Gate oxide thickness	0.065

Table 2: Measured and data sheet values of the electrical parameters

Parameter measured	Measured value			Data sheet value
	Virgin	Degraded shift%		
I_{GSS}	12 pA	340 pA >100		‹ 40 nA
I_{DSS}	2 nA	90 nA >100		‹ 1.5 μA
V_{th}	4.1 V	4.83 V	17	4v ≤ ; ≥ 5v
$V_{(BR)DSS}$	86 V	81 V	6	75V ≤
Crss	0.43pF	0.34 pF 21		typ. 0.5 pF
S_{21}	-7.3 dB	-10 dB 36		‹ 11 dB

IV. Conclusions and Prospects

This objective constitutes an investigation to clarify the problems related of Hot Carrier Injection effects for reliability exerted on power RF LDMOS under operating conditions of radar application (stress: electrical, thermal and RF). The reliability is shown by monitoring I_{ds}, V_{th}, C_{rss}, S_{21}, T°C and I_{GSS} parameters in order to put in evidence the device performances. The simulation approach helps to assess the device robustness under critical conditions by means of the temperature evaluation, RF and current distributions in LDMOS structures operating. The results obtained highlighted a degradation caused primarily by the mechanism of hot carrier injected in oxide layer and in channel interface states (i.e. hot-electron-induced interface state generation and/or impact ionization), and in turn its effect on critical parameter drifts (I-V, C-V and RF). These are sensitive parameters to the electrons injected in gate/SiO_2 interface traps.

This paper represents the starting point for the development of an accurate and more complex FEM based simulation concept which would correctly include electro-thermal effects. Further failure mechanisms, e.g. the possible activation of the CEM will be integrated within the simulation condition. Moreover, it would be interesting to make the connection with the normal life of a component, through an aging model or MTTF (Mean Time To Failure). The comparison of this study with other technologies such as IGBT and VDMOS is underway.

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