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An Extansive Review of Emerging Technology Networks-on-Chip Proposals

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An Extansive Review of Emerging Technology Networks-on-Chip Proposals

Ahmed Ben Achballah [α], Slim Ben Othman [σ] & Slim Ben Saoud [ρ]

Abstract- Many synthesis works discussed emerging technology networks−on−chip (NoC) from different aspects. These works were and still are a solid foundation of the state of the art for emerging technology NoC research and practices. However, with respect to their quality and conciseness, the available literature is outdated or don't give an extensivere view of the available contributions in this area. In this paper, we iterate and discuss our findings in terms of research and practices for emerging technology NoC for the last ten years. The analyzed proposals are exposed chronologically. This will help to answer to the questions of when and how the concept was introduced, what is its present state and what the future directions are.

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I. Introduction

NEtworks-on-chip are a widely used technology within recent systems-on-chip (SoC) and chip-multi-processors (CMP)[1]. However, several emerging technology NoC are proposed as a potential replacement for classical NoC [2, 3]. To this aim, several research works have focused on the design of emerging technology NoC. The research in this particular field is further developed because the fabrication processes of integrated circuits are also evolving. Unfortunately, the literature for emerging technology NoC is scattered and is not extensively reported[4, 5].

In this paper, the lack of a global review of the emerging technology NoC research is addressed. An extensive review of the available literature regarding emerging technology NoC is executed, resulting on the analysis of more than 200 papers. Additionally, the available surveys and textbooks in the NoC domain are reported. The analyzed research papers are exposed chronologically. This will help to answer to the questions of when and how the concept was introduced, what is its present state and what the future directions are. To organize the survey, we categorize the available research and contributions for emerging technology NoC as it is shown in Figure 1. Our approach is a technology−based approach.

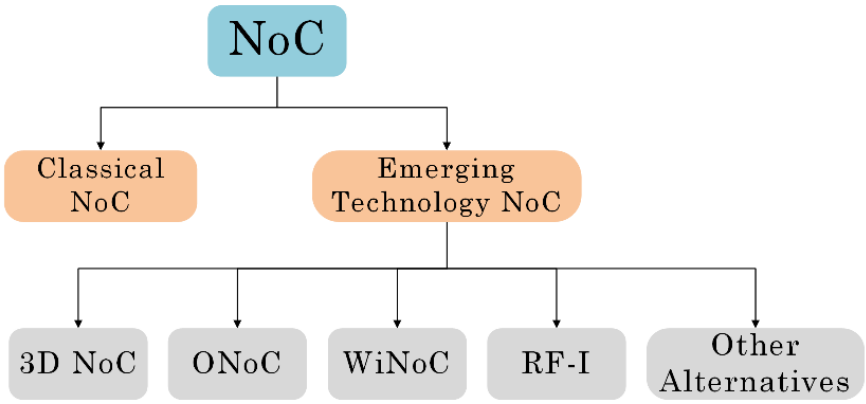

Figure 1: Technology−based classification of NoC

Before we move forward in this review, we briefly introduce in the following the two NoC's alternatives that are classical or emerging technology NoC.

- *Classical NoC* constitute an established baseline technology in the field and the unique commercialized technology. Most of the available efforts in the literature were built around such technology. The research community has explored this lead very well. However, the most significant result, is in the industrialization of the NoC concept, for both sides, providers of NoC solutions [6-8] and SoCs/CMPs vendors[9-12].
- *Emerging technology NoC* are a direct result from exploiting any valuable advances from silicon industry. Usually, the research efforts regarding emerging technology NoC are divided in four major categories, which are 3D NoC, Optical NoC (ONoC

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also reported PNoC for Photonic NoC), Wireless NoC (WiNoC also reported WNoC), and finally Radio-Frequency Interconnect (RF-I also reported RFNoC). However, there are other original attempts. They targeted some of the advanced and under development technologies such as graphene substrate.

The remaining of the manuscript is organized as the following: we briefly recall and classify the available surveys and textbook in the second paragraph. In the third paragraph, we review the emerging technology NoC literature subdivided in terms of principal research axis while in the fourth paragraph we conclude the manuscript.

II. Related Surveys And Textbooks

For the last fifteen years, many surveying works had enriched the NoC literature. Such synthesis papers constitute a solid backbone for present and future research as well as for this work. Through this paragraph, we tried to collect and expose these works as the literature lacks such collection. This is also an interesting aid for new NoC researchers as it could shorten their state-of-the-art investigation exercise. Table I lists the available surveying works that we found in the literature. In addition, we give a list of the published textbooks in the same area.

Table I: NoC–Related State of the Art

NoC– related surveys and synthesis efforts		NoC– related textbooks	
Authors [Date]	Reference	Authors [Date]	Reference
Seitz [1990]	[13]	Dally and Towles [2003]	[14]
Dally and Towles [2001]	[15]	Duato et al. [2003]	[16]
Benini and De Micheli [2002]	[17]	Jantsch and Tenhunen [2003]	[18]
Ogras et al. [2005]	[19]	Ogras and Marculescu [2006] from Chen (Editor) [2006]	[20]–[21]
Pande et al. [2005]	[22]	De Micheli and Benini [2006]	[23]
Bjerregaard and Mahadevan [2006]	[24]	Kogel et al. [2006]	[25]
Owens et al. [2007]	[26]	Yoo, Lee and Kim [2008]	[27]
Salminen et al. [2007] – [2008]	[28]–[29]	Pasricha and dutt [2008]	[30]
Atienza et al. [2008]	[31]	Jerger and Peh [2009]	[32]
Dafali et al. [2008]	[33]	Chrysostomos et al. [2009]	[34]
Zydek et al. [2008]	[35]	Gebali et al. [2009]	[36]
Feero and Pande [2009]	[37]	Murali [2010]	[38]
Marculescu et al. [2009]	[39]–[40]	Flich and Bertozzi [2011]	[41]
De Micheli et al. [2010]	[42]	Silvano et al. [2011]	[43]
Deb et al. [2010]	[44]–[45]	Cong-Vinh [2012]	[46]
Rahmani et al. [2010]	[47]	Cota et al. [2012]	[48]
Chen et al. [2011]	[49]	Fu and Ampadu [2012]	[50]

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Gu [2011]	[51]	Ogras and Marculescu [2013]	[52]
Fernandez–Alonso et al. [2012]	[53]	Palesi and Daneshtalab [2013]	[54]
Kim et al. [2012]	[55]	Bergman et al. [2014]	[56]
Postman and Chiang [2012]	[57]	Tatas et al. [2014]	[58]
Ben Achballah and Ben Saoud [2012]	[59]		
Buckler et al. [2012]	[60]		
Choudhary and Samota [2012]	[61]		
Radetzki et al. [2013]	[62]		
Abbas et al. [2014]	[63]		
Bertozzi et al. [2014]	[1]		
Wang and Jin [2014]	[5]		

III. Emerging Technology NoC Proposals

a) 3D NoC

A natural evolution in the NoC paradigm is the transition from 2D to 3D NoC. As the integration technology is evolving, many 3D techniques are developed allowing the stacking of multiple dies with numerous processing elements and memories. The connection between these dies is physically assured by interconnect techniques such as wire-bounding, micro-bumps, TSVs and lately wireless capacitive- and inductive-coupling [64]. These interconnects fabrics are shifting from simple point to point connections to more developed networks that link at the same time between the die elements and the dies from different layers, called 3D NoC. Several comparative studies between 2D and 3D NoC are available [58, 64-66]. The research in this area is very mature compared to the other emerging technology NoC. In fact, we can find in the literature many established works where the efforts have evolved from simple architectural dimensioning to high-level abstraction, routing algorithms, fault tolerance and resolving physical related problems like the TSVs failures or the thermal overheads. In the following, a distillation of the recent works is provided.

i. *Fault tolerant and reliable 3D NoC*

3D NoC offer a better area-performance ratio compared to 2D NoC thanks to the third dimension. However, this has triggered additional issues. Among them, we can find the containing of the TSVs number and the design of more low-power architectures. Hence, the reliability of 3D NoC is more challenging and by consequence is heavily investigated in academia. Recently, Jiang and Xu surveyed the works as regards fault–tolerant 3D NoC architectures[4]. The authors provided an extensive classification of defects and fault models. A listing of the existing fault-aware routing algorithms as well as a comparative study are also provided. In this section, some of the studied proposal in [4]are considered. In addition, the more recent proposals that are not studied by Jiang and Xuare also discussed.

Researchers targeted the deadlock freedom of 3D NoC. For example, Ben Ahmed and Ben Abdallah proposed an efficient fault–tolerant and deadlock free algorithm for 3D NoC called Hybrid-Look-Ahead-Fault-Tolerant (HLAFT)[67]. The presented algorithm showed better results than XYZ algorithm and its predecessor called LAFT [68].

Dubois et al. [69]and Somas undaram et al. [70] respectively developed two other similar works. The first one is an algorithm called Elevator-First. It is a distributed algorithm with deadlock-and live lock-freedom capabilities. It is also applicable to both 2D and 3D partially connected architectures. The second one is a deadlock-free algorithm and when combined to a 3D NoC topology developed by the same team, outperforms the proposition of the first work [69].

Lee et al. in their turn [71], attempted to enhance the Elevator-First approach from [69]. The authors maintained the performances of the Elevator-First algorithm with the elimination of virtual channels, which is a very area-saving maneuver. More recently and also based on the Elevator-First algorithm, Lee et al. developed a new energy-efficient and deadlock-free algorithm for 3D NoC called Redelf [72]. The evaluation results showed that the proposed algorithm acted better than the basic Elevator-first in terms of energy consumption and latency.

Ebrahimi et al. established a similar approach[73]. The authors developed a fault-tolerant routing algorithm for 2D and 3D NoC using the advantages of the Hamiltonian path. NaghibiJouybari and Mohammadi, in their turn, developed another fault tolerant algorithm for 3D mesh NoC[74]. The authors proposed FT-DyXYZ, a fault tolerant adaptive routing algorithm that was able to avoid permanent faulty links. The same team proposed a newer fault-tolerant and

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energy-efficient algorithm for TSV-based 3D NoC called FT-Z-OE[75]. Finally yet importantly, some of the other efforts focused on developing innovative 3D NoC architectures. As an example, Ben Ahmed et al. presented in [67]a 3D NoC router architecture called 3D-Fault-Tolerant-OASIS while Marcon et al. developed a lightweight and fault−tolerant 3D NoC architecture called Tiny NoC[76].

ii. *Novel 3D NoC architectures*

To bypass the limitations caused by TSVs, other research efforts explored wireless capacitive-and inductive-coupling between the stacked dies [77]. The difference between the two technologies is that for capacitive-coupling only two dies or chips can be connected in a face-to-face fashion. However, with inductive-coupling, many dies can be stacked together. Take et al. [78]and Miura et al. [79]respectively proposed two 3D NoC architectures called Cube-0 and Cube-1. The communication between the different layered chips was assured by inductive-coupling links that are organized in a ring topology. These architectures are also reported as 3D wireless NoC (3D WiNoC) in the literature [77].

Later, several extended studies related to 3D NoC architectures with wireless vertical links were conducted. Matsutani et al. executed in [80]a routing and topology design space exploration. The authors used spanning tree optimizations to reduce the hop count of the network. Zhang et al. developed in [81]an optimized power management scheme. The authors managed to dynamically activate and deactivate the supply power for a portion of the vertical links. The two studies demonstrated that a good balance between the proposed power management technique and the spanning tree optimizations achieved good performances at a reasonable power cost.

Recently, Matsutani et al. investigated the use of an extra NoC layer with a random or mesh topology to enhance the performances of 3D ICs[82]. Two approaches were developed. The first one targeted NoC-less 3D ICs while the second one targeted NoC-based 3D ICs. The authors experimented several configurations scenarios. Several combinations between four vertically-layered ICs with all-mesh, all-random or mixed topologies NoC were benchmarked. The simulation results showed that such configurations could reduce the latency of the transferred packets especially when random topologies were considered. It was also demonstrated that one or two NoC layers with a random topology are sufficient to reduce the packets latency [82].

The latter works have shown a very interesting economic potential with the 3D wireless NoC architectures. Rather than integrating components in a single chip like for SoCs, the required IPs can be vertically stacked on multiple chips equipped with inductive coupled links in a System-in-Package (SiP). As a direct consequence, many chip combinations can be established with legacy designs at moderate design costs.

Finally, other esoteric studies were also developed. For example, Elmiligi et al. used a genetic algorithm to build 3D mesh NoC with reduced power consumption from a given application[83]. The algorithm was tested and validated in an architecture of 32 microprocessors. Daneshtalab et al. presented a novel methodology to reorder request packets without the need of the two conventional solutions: the dimension−order routing by limiting the packet to use the same path that is performance degrading, or the packets reordering inside the network interfaces that is area expensive[84].

iii. *Design space exploration for 3D NoC*

To tackle the several challenges of 3D NoC, a design space exploration of the 3D NoC-based designs is important. This goes through the developing of analytical models for 3D NoC components as well as for common defects and faults. Khayambashi et al. studied the impact of the TSVs' failures on the reliability of 3D NoC[85]. This allows a more accurate estimation of the area overheads versus the performance gains from the use of TSVs in the design. Jiang et al. proposed the resolution of the latter compromise at higher levels of abstractions[86]. The authors developed an adaptive algorithm that can provide low latency and low power without increasing the TSVs number. This solution maintained a reduced TSVs number for larger 3D NoC-based designs. Ying et al. [87], in their turn, developed a task allocation method for 3D NoC with limited number of TSVs. The proposed method was contrasted with prior methods such as the genetic algorithm and the simulated annealing.

Ebrahimi et al. explored several partitioning methods of multicast communications in 3D mesh NoC in addition of developing analytical models for each method[88]. They came with a conclusion that among the applied methods, the recursive method was the productive one. A similar approach was proposed by Meena et al. called 3D-RPM for 3D recursive partitioning multicast routing algorithm[89].

Lastly, Dahir et al. discussed the reduction of the 3D NoC temperature[90]. The authors alleviated this challenge from the application layer. The authors used a runtime thermal management technique called DPN to moderate the traffic flow in the network, hence assuring a moderate silicon temperature.

b) Optical-Photonic NoC

Optical-photonic NoC are a very serious candidate to succeed to classical NoC. In fact, Optics were and still are a viable and widespread solution used in macroscopic networks from the simple single−server installation to the complicated data centers. The reason is such technology offered a very interesting

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performance by power consumption ratio among other important benefits. Optical interconnects have been imagined for ICs in very earlier studies such as in these works [91, 92]. At the same time, many efforts showed that in the transistor scale, the integration of basic optical components in CMOS technology, such as laser sources [93, 94], modulators [95], on−chip waveguides [96], and finally detectors [97], was feasible. Moreover, basic functionalities such as buffers [98]and optical-based logic functions [99]were experimented. These discoveries have not only triggered the research and the exploration of optical interconnects, but also proved their positive potential for an eventual commercialization [100].

Earlier established studies by Haurylauet al. in [101], Chen et al. in [102], and Petracca et al. in [103], discussed the performances that might emanate from CMOS compatible optical components. Depending on the available or the projected technology, the authors also contrasted the optical interconnect performances with their electrical counterparts to demonstrate the electrical interconnect limitations in the future.

i. *All-optical NoC*

To the best of our knowledge, Kirman et al. presented the first attempt to develop an on-chip optical network[104]. The authors designed a ring-based topology optical NoC where the network consisted of an optical ring or loop on which four switches are connected. Each switch managed a set of IPs such as memory controllers or L2 caches. The results showed performance enhancements in terms of latency for the proposed architecture, a four-node opto-electrical buses, compared to its pure electrical counterparts especially when two or more distinct wavelengths were used.

ATAC was also another alternative to build optically interconnected many-core processors chips [105]. The proposed architecture utilized an on-chip optical network to connect 64 clusters for 1024 cores. Compared to a similar electrically-interconnected 1024 cores architecture, ATAC succeeded on 39 % of speed-up [106, 107].

Shacham and Bergman executed another attempt in the field[108]. The authors presented an optical interconnect called SPINet. The experimental architecture of SPINet is a 2x2 switching node that exploited wavelength division multiplexing (WDM) for a total bandwidth up to 160 Gb/s (16 wavelengths x 10 Gb/s link). As an experimental setup, the authors tested a four nodes architecture to demonstrate the SPINet capabilities. Later, a second demonstration with six SPINet nodes was described [109].

Vantrease et al. proposed a 3D optical network called Corona[110]. The optical interconnect was used to link up to 64 clusters composed essentially by four cores with a shared L2 cache and where on top of them were placed optically connected memories (OCMs). The optical interconnect was a global broadcast optical bus where all the clusters were connected. Corona showed high performances of 10 Tb/s for OCMs and 20 Tb/s for the clusters' cores. However, the separation between the optical interconnect, the clusters and the OCMs omitted the scalability problems. This is one of the most important challenges for ONoC. Vantrease et al. developed a related work to Corona consisting of an optical arbitration mechanism to maximize the channels utilization of optical interconnects[111].Moreover, Hendry et al. tackled in [112]the posed problems by a circuit−switching ONoC such as in [108]. The authors started from the results of an earlier established analysis[113]. After, they proposed a TDM arbitration scheme to replace the electrical parts, which were responsible of the network resources allocation.

Similarly, Biberman et al. developed an electro-optical switch architecture with up to 40 Gb/s data transfer rate[114]. Furthermore, a multi layered version, based on the previous switch architecture, was presented by the same team [115]. In addition of the CMOS compatibility and the high scalability of the architecture, the authors demonstrated the usefulness of such switch fabric in the case of data-centers. The switch architecture consisted of 256x256 non-blocking ports for a 51.2 Tb/s bisection bandwidth capable of linking up to 2560 server racks.

As conventional processors were scaling to many-core systems with higher bandwidth networked memories (usually DRAMs) [116], many solutions have emerged not only to alleviate such demands but also with energy efficiency considerations. In [117] and [118], and later extended in[119], the authors presented a monolithic processor-memory network architecture based on photonic technology. The architecture used dense wavelength-division multiplexing (DWDM) in local meshes to global switches (LMGS) ring matrix topology. Up to 256 cores could be connected to 16 DRAM modules for an improved throughput of 8 to 10 times compared to an aggressive purely electrical network.

Joshi et al. developed another related LMGS architecture that was organized on an U-like shape[120]. This architecture showed a less power consumption for thermal tuning circuits but suffered from higher power losses in the waveguides and the end-to-end through.

Beamer et al. [121]proposed a novel photonically interconnected DRAM (PIDRAM) architecture based on a previous design that has been described earlier in [117]. Major enhancements were high per−pin bandwidth with on-and off-chip energy savings, compared to equivalent, even future, pure electrical counterparts. More details for the design of on-chip core-to-core and core-to-memory photonic networks are provided in[122]and in [123].

Joshi et al. also presented a similar architecture based on Clos networks[124]. Simulation results

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demonstrated that Clos networks had a smaller power and area impacts compared to a baseline NoC or to a photonic NoC with global crossbars (centralized and distributed). In addition, the Clos photonic network maintained a uniform latency and throughput thanks to its extensive path diversity. The Clos network was also used to design a buffer less photonic Clos-based NoC called BLOCON [125]. A contention-free algorithm called Sustained and Informed Dual Round-Robin Matching (SIDRRM) along with a path allocation scheme named Distributed and Informed Path Allocation (DIPA) were used as routing mechanisms for the proposed architecture. Similarly, Koohi and Hessabi developed a contention-free all−optical routing method called CoNoC[126]. An extended version of the developed efforts with CoNoC is available here [127].

The research on the field of pure photonic point−to−point interconnects for on-chip communications had continually evolved. The proposals that we have already discussed like the Cornell ring architecture [104], the MIT ATAC [105], the Columbia SPINet [108] and Corona [110] constitute a foundation to the following works.

Pan et al. proposed a nanophotonic architecture called Firefly[128]. The authors combined electrically connected nodes (organized by clusters of four nodes) with a global photonic wave-guide for intra-clusters communications. For a more energy efficiency, a reservation-assisted single-write-multi-read (SWMR) design was implemented. Initially, all the network receivers are disabled. To send a packet, the router broadcasts a packet with the destination and the control information. Hence, only the receiving router is activated. Overall, the Firefly architecture resulted on performances better than the state-of-the-art all-optical or all-electrical architectures.

Later, the same authors tackled a very common challenge in optical NoC that is the reduction of the static power consumption[129]. They presented Flexi Share: a crossbar architecture with minimum but globally shared channels for all the nodes. Although such architecture seemed to add more energy constraints due to the design complexity, the energy gain was perceptible due to the reduction of the channels' number with their static power overhead.

Morris and Kodi investigated on their turn the feasibility of a 64 cores ONoC called PROPEL and its extended version E-PROPEL for up to 256 cores architecture[130]. The two versions were confronted to Batten et al. [117] and Vantrease et al. [110]proposals, at an equal number of wavelengths. The comparison was discussed in terms of hardware complexity with metrics such as the number of waveguides, microring resonators and photodetectors. The power loss and the optical/electrical areas were also considered. The comparative study also compared the proposed ONoC architecture with a conventional mesh NoC in terms of the obtained throughput and power consumption.

Xue et al.[131]studied another optimistic approach. The authors presented a 3D optical interconnect using free-space optics. This type of propagation medium offered a speed of light propagation with a small energy loss. However, this technique relied on the technological advancements of optical components like micro-lenses and micro-mirrors. In addition, to demonstrate the feasibility of their design, the authors conducted a study related to newly-developed or emerging devices, circuits, and optical dedicated technologies. A prototype in relation with this study was also fabricated[132].

In the last 3 years, many ONoC architectures have emerged. Among them, we can find the Olympic ONoC[133]. A full-optical ring topology NoC where local and global rings were used to mitigate the low latency versus the high-energy consumption problem.

Luminoc was another all-optical mesh topology NoC that took advantages from MWSR (multiple write single read) arbitration method and from point-to-point connection for data transmission[134]. Simulation results showed that Luminoc acted better than electrical mesh NoC and the Clos architecture from[124]. However, such topology still depends on technology integration of dense optical channels on a silicon chip. Recently, Kakoulli et al. considered the integration of optical components in silica to develop a comparable approach to Luminoc in terms of performances[135]. Unlike Luminoc, the P-sync proposal was a shared-bus based architecture that used Photonic Synchronous Coalesced Access Network (PSCAN) [136]. The full architecture targeted long range interconnect applications that require non-local data accesses such as the distributed Fast-Fourier Transform (FFT).

Zulfiqar et al. studied in [137]the impact of the point-to-point and shared channels for optical interconnects for a fixed laser power budget. The authors pointed the static power consumption of ONoC in particular the laser sources that were the major consumers. As a solution, they estimated an ideal sharing degree in function of the optimal sharing gain and proposed wavelength stealing. The proposed solution used the same topology as for point-to-point networks with N2 channels. Each channel had at least two nodes, the owner and one or more stealers. Evaluation results demonstrated that such architecture provided between 20 and 23 % energy-delay product (EDP) improvement compared to point-to-point topology.

Similarly, PROBE was another alternative to diminish the static power consumption of ONoC [138]. The authors proposed the use of tunable splitters instead of the passive power-inefficient ones. The authors used the tunable splitters to scale the available bandwidth dynamically. For an accurate scaling of the bandwidth, a prediction evaluation was computed from the link and the buffer utilizations of every output port.

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At a higher level of abstraction, Chao et al. tried to alleviate the challenges of the laser power consumption[139]. Their proposition was to split the energy budget among the network buses based on a weighted time−division−multiplexing scheme. The TDM mechanism was based on the instantaneous bandwidth requirements of the running applications. Later by 2014, the same authors proposed a methodology for the placement and the sharing of on-chip laser sources for an optimal and high energy-efficient use [140]. Additionally, the last study included a relevant state-of-the-art synthesis for ONoC research axis. In the same way, Heck and Bowers conducted a study to demonstrate that on-chip laser sources can increase the source efficiency and the energy consumption compared to off-chip laser sources due to the modularity they offer and because of the absence of coupling losses.[141]. Pintus et al. unveiled in [142]a novel all-optical and ring−based ONoC architecture. Recently, Gambini et al. detailed the prototyping of the same ONoC in silicon[143]. The ONoC was centralized on a principal ring coupled to multiple local micro-rings. The authors provided simulation scenarios for both performances and fabrication tolerances with a silicon-on-isolator (SOI) technology platform.

Network interfaces (NIs) were at the heart of the study presented by Ortín-Obón et al. [144]. The authors discussed the lack of the research in the NI level in ONoC in spite of its important participation for the data transfer of an optical on-chip network. The authors proposed the design of a complete NI architecture for wavelength routed ONoC. They also demonstrated that to maintain an acceptable bandwidth with realistic power budget, 3- to 4-bits parallelism should be applied. Less than 3-bits parallelism results on a very low bandwidth while more than 4-bits parallelism results on poor power behavior in particular with the static power consumption.

Two other all-optical wavelength-routed NoC proposals were developed by Koohi and Hessabi in [145] and [146], respectively. The first one, called 2D-HERT used a novel topology based on a passive routing with wavelength-routed optical switches (WaROS). The obtained results showed a reduced energy consumption and a lower data-transmission average delay compared to a baseline ONoC as well as to a classical NoC with torus topology. The second all-optical architecture was called Power-efficient Scalable Wavelength-routed Network-On-Chip (PeSWaN). The proposed ONoC had the ability of a controlled scaling. In fact, the implemented control mechanism of PeSWaN used N/4 control units for a total number of N nodes along with contention-free switching data circulation.

Hamedani et al. developed a similar architecture[147], namely QuT. The QuT proposal was based on a ring topology constructed with microring resonators in addition of strategically placed shortcuts. Compared to a baseline ONoC such as Corona[110], QuT had smaller insertion losses but more microring resonators. Compared to CoNoC[127], QuT had a smaller number of microring resonators but more insertion losses. Overall, QuT offered a balanced power and energy consumption for a better scalability than Corona and CoNoC.

Similar to QuT, Werner et al. proposed an ONoC based on a mesh-like topology called Amon[148]. The proposed architecture outperforms QuT and several other ONoC. With a limited overhead in the waveguides area, Amon offered a better power consumption as well as a lower area consumption for the microrings area while maintaining similar performances.

Wu et al. [2014] presented SUOR[149]. The authors designed a cluster organized ONoC for up to 256 cores. Dedicated clusters called cluster agent (CA) assured the flow control and the data channels set−up. Simulation results showed a more reduced EDP compared to Corona [110] and Flexi Share [129].

Last but not least, Xiaolu proposed a ring−based packet-switched ONoC called RPNoC[150]. The proposed architecture showed a better energy/bit consumption compared to an optical NoC with a mesh topology, and an electrical NoC with mesh or ring topologies. RPNoC also had a higher packet throughput and a lower latency compared to the aforementioned NoC.

ii. *Hybrid-optical NoC*

A common practice for hybrid emerging technology NoC was the combination of a local electric baseline NoC or some of its components with a global optical one. The Phastlane architecture was an example of such heterogeneity [151]. The authors tackled the contention that might occur in optical NoC with electrical buffers in a manner that the received packets could be electrically-buffered or dropped then retransmitted.

Ye et al. proposed a hybrid electric-optical router to build a torus topology based ONoC[152]. The proposition called THOE was composed of clusters (4 cores per cluster with electrical interconnections) connected with an optical network with, full-optical, circuit-switching capabilities. THOE showed not only better power consumption compared with a classical NoC with the same topology but also better resource usage compared to baseline ONoC such as the torus network [153] and Corona [110].

Meteor was another hybrid optical-electrical NoC [154]. The architecture coupled an optical ring-shaped waveguide with 2D mesh electrical NoC. This architecture offered a more simplified optical network with its power efficiency and reduced latency combined to a full-distributed 2D electrical mesh. METEOR offered an interesting modularity with its Photonic Region of Influence (PRI) in a way that the optical waveguide could

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connect a set of cores' islands from 2 to up 36 cores. When compared to the state-of-the-art ONoC such as Corona [110]., Firefly[128], the optical mesh from [153]and a 2D mesh equivalent NoC, METEOR had a reduced power consumption and EDP with a simpler photonic architecture.

Close to the Meteor proposal, Grani and Bartolini established another effort[155]. An optical ring NoC in combination or not with a conventional NoC was studied in terms of power consumption and latency. Many simulation scenarios were provided including diverse arbitration strategies along with the possibility of the variation of the optical ring numbers.

Fu et al. developed a similar electrical-optical NoC architecture, namely, HEON[156]. The authors tackled long electrical wires with a global optical one in a serpentine shape to link the distant cores. They also used a dynamic power strategy capable of dynamically managing the network components. Simulation results showed that HEON had more than 43 % EDP gain compared to a baseline NoC and ONoC, respectively.

In [157], Tan et al. described a hybrid locally-electrical and globally-optical connected architecture (HONoC). The architecture was organized in a BFT-based topology. HONoC relayed on hybrid routers to link between locally-electrical cores and globally-optical connected clusters. The latter were in their turn connected via a generic wavelength-routed optical router (GWOR) developed earlier by Xianfang et al. [158].Moreover, Büter et al. developed a controller called DCM for distributed channel management that was capable of switching between two different parallel NoC such as an ONoC and an electrical one[159]. The DCM was also able to reconfigure the same electrical NoC if reconfigurability was implemented. For a hybrid configuration, the authors used the two baseline ONoC architectures from [153] and [130] to validate their approach.

Finally yet importantly in the optical-electrical hybrid NoC direction, Balboni et al. [160] studied the internal interconnect fabric of general-purpose processor accelerators (GPPA). The authors addressed the global electrical NoC that serve to link processing elements on-and off-the chip with an optical one. The proposed hybrid network architecture was simulated for 1- to 4- bits parallelism. After that, it was compared to its pure electrical counterparts. Results showed an important overhead on static power, however in the dynamic energy domain the proposed hybrid ONoC was more efficient.

As another direction for hybrid emerging technology NoC, 3D optical NoC were developed. Ye et al. utilized two superposed layers, an optical layer and an electrical one[161]. The optical upper layer was used to transfer data packets while the bottom electrical layer handled the control packets as well as controlling signals to the optical switches. The communication between the two layers was assured with vertical TSVs. Similarly, Le Beux et al. proposed the exploitation of the low power and latency advantages of an additional optical ring NoC (ORNoC) layer to connect multiple conventional NoC-based layers in a 3D fashion[162]. The proposition also provided guidelines for an optimal placement of the NoC layers and the TSVs as the distance separating the upper ORNoC layer from the lowest NoC ones could be considerable. Moreover, Qing et[163] presented a comparative study between 3D ONoC and 2D ONoC. After developing the 3D ONoC router model, they demonstrated that 3D ONoC alleviated 2D ONoC related problems such as long interconnects. They also provided better results in terms of the delay and the packets losses.

iii. *Design space exploration for Optical-Photonic NoC*

No efforts related to ONoC we cited above would be achievable if the research community did not execute a rigorous design space exploration [1]. In the following we cite our findings in terms of design space exploration, analysis and tools related to optical interconnects.

Hendry et al. initiated the analysis of photonic networks through a developed model for omnet++ tool[113]. Many simulation scenarios with diverse loads and topologies were executed. Later, Chan et al. [164] investigated several tools and design methodologies. The authors developed an extensive study as regards ONoC [165]using a dedicated ONoC tool called Phoenix Sim [166]. The same team explored the physical layer of ONoC. A variety of the basic components for ONoC was modeled [167]. More recently, Abadal et al. studied ONoC in terms of area and energy scalability[2].

The industry was also involved on the design space exploration of optical NoC[168] while Koka et al. presented an earlier proposition[169]. The authors conducted an extensive comparative study between many baseline ONoC architectures. The studied architectures were token ring, point-to-point, limited point-to-point, circuit switched and two-phase with two ramifications. The simulation results of the considered 8x8 microchip developed by Krishnamoorthy et al. demonstrated that the point-to-point optical network showed an interesting EDP[170].

From a topology perspective, Faralli et al. investigated the performances of bus- and ring- based ONoC[171]. The authors contrasted the performances of the ring-based ONoC developed in [143]with a bus-based one. The comparative study was proceeded at the physical layer with real prototypes. The obtained results showed that the performances of ring- and bus-based ONoC are comparable in worst-case scenarios. However, if interferences could be avoided, the ring-based ONoC outperforms the bus-based one.

As optical component are thermally sensitive and by consequence can degrade the system performances, thermal management of ONoC is a research direction of a huge interest. To remedy to the

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deviation of on-chip optical components, Zhang et al. proposed to localize the hotspots on the targeted platform with an accurate simulation[172]. Based on the latter results, a new task allocation scheme was deployed to contain the temperature of the network modulators and filters while maintaining the bandwidth full-availability.

Since PhoenixSim, many other DSE tools have emerged such as VANDAL [173], DSENT [174] and PROTON [175]. More recently, other tools were developed such as CLAP [176], OTemp [177], PROTON+ [178] and the ONoC dedicated reliability-aware design flow in [179]. Additional information for ONoC dedicated tools are also available in this textbook [56] (Refer to the fourth chapter).

Even with the recent advancements on the technology integration of on-chip optical components [180], some recent studies putted the accent on the exploration of the physical layer. Mainly because the physical layer is a major bottleneck for an ONoC-based design. In this way, Ramini et al. studied the power behavior of wavelength routed ONoC (WRONoC) with multiple topology configurations[181]. The authors also demonstrated how a design could diverge from its high-level initial expectations due to the place & route constraints. In addition, they pointed the lack of CAD dedicated tools for ONoC at the physical layer. A potential solution to this challenge were presented by Boos et al.[175], Ramini et al.[182] and recently[178]. Moreover, Ramini et al. questioned with respect, the viability of ONoC solutions and demonstrated how an aggressive conventional NoC outperformed its optical counterpart[183]. A key assumption on the last attempt was the consideration of an accurate modeling framework (AMF) instead of the common one (CMF). This led to a meticulous consideration of every design power parameter.

iv. *Final remarks*

To conclude this paragraph, we cite some recent and very promising results obtained at the physical layer for optical on-chip components and networks. Qian et al. succeeded on integrating a quantum-dot light emitting diodes on a multilayer structures[180]. Qiang et al. designed and profiled a compact silicon optical switch based on the thermo-optic effect instead of the usage of traditional microring resonators or Mach-Zehnder interferometers[184]. Lately, Wang et al. presented a complete ONoC integrated in Si-CMOS platform[185]. Similarly, Yang et al. presented a reconfigurable and non-blocking four port optical router[186]. The fabrication process as well as the measured performances results were reported.

The Hubeo+ project is also another promising work that was presented by Thonnart and Zid in [187]. In fact, a demonstrator of an optical networks-on-chip is planned for 2016 for up to 36 cores with a bandwidth up to 2 THz and a 20 W power consumption. The authors also claimed that by 2020 the expected performances will reach 4 THz for more than 72 cores with the same power consumption of 20 W. The targeted cores of the demonstrator were supposed to be microprocessors and memories. Finally, readers can find an updated and extensive listing of the available literature for inter- and intra-chip optical-networks in this online bibliography[188].

c) Wireless NoC

Wireless NoC can circumvent many of the persistent issues related to classical NoC. For example, WiNoC can tackle the correlated increase of the power consumption and the computation capacity or the on−chip long-range wires vulnerability[189]. As the integration technology matures, the research for WiNoC is evolving. In addition of the various feasibility studies that are elaborated by Ding et al. [190], Karim et al. [191]and Xinmin et al. [192], there are now various hardware prototypes which are developed[193, 194]. According to many simulation scenarios[195], WiNoC have the best bandwidth by packet energy ratio among other emerging technology NoC. Moreover, WiNoC showed a very interesting scalability for 512 cores system size and more. This important scalability is offered with a limited area overhead due to the absence of wires [44]. Only RF-Interconnect or Optical NoC can compete with such capabilities, in some aspects. Ganguly et al. investigated the design methodologies, the technology specifications and the performance evaluation for WiNoC architectures[196] but recently Abadal et al. established a new design space exploration related to WiNoC[3].

The wireless NoC architectures can be classified in two major categories. The first one is composed of many wired NoC clusters that connect a set of cores. Usually, they are organized in a mesh topology fashion. Each one of the sets communicates with the other ones through wireless shortcuts. The second one, called small-world wireless NoC, aims on developing a NoC with a balance between short local links and long range wireless links[45]. Hence, this approach alleviates the topology-inflexibility problems of the mesh-based WiNoC. The idea was inspired from natural networks such as the brain neurons networks or from macroscopic networks like the Internet and some social networks.

i. *Mesh-topology based wireless NoC*

The first attempts have targeted the first type of WiNoC architectures. The proposed work by Zhao and Wang figured among these efforts[197]. The authors developed a WiNoC architecture based on CMOS ultra wide band (UWB) technology. Later, the same authors relied on the flexibility of the wireless nodes to rebuild as needed the network topology to meet the application constraints[198]. An unfeasible operation with wired nodes without considerable area overheads. Moreover, a limited set of wired links are used to control the

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wireless nodes and so leaving 100 % of the wireless link bandwidth to data transportation. When the topology is fixed, a location-based routing (LBR) is used to circulate the data among the nodes.

An additional impact of topology rebuilding was the possibility of multi-channeling in a way that a node can broadcast the same data to many other nodes, hence increasing the network throughput. Moreover, deadlock avoidance capability was implemented to maximize the determinism and the reliability of the proposed architecture. The enhanced WiNoC architecture was called multi-channel wireless NoC (McWiNoC).

Zhao and Ruizhe[199]presented an overlaid mesh topology where "big" wireless nodes with long-range multi-channel links were placed among "small" nodes with simple short-range links to the bigger ones. They also developed a network capacity model that was used to search the optimal topology configuration for the network. The followed methodology relied on a zone-aided routing algorithm to assure deadlock freedom for the data transfer without sacrificing the network efficiency[200]. The multi-channeling and arbitration methodology we cited above was later enhanced with DuSCA that stood for dual selection channel arbitration scheme. DuSCA was developed to arbitrate receiving and sending conflicts at the receiver and the transmitter sides with a static channel assignment scheme [201].Lately, Ruizhe and Zhao proposed a more developed arbitration scheme[202]. The authors targeted conflicts that might occur from static channel assignments when many senders solicited the same receiver simultaneously. The authors presented a load adaptive multi-channel arbitration mechanism to alleviate DuSCA limitations and eliminated the contention problems.

Lee et al. in their turn, proposed a centralized single transmitting antenna to multiple receiving antennas WiNoC architecture, namely WCube[203]. The architecture can achieve 20% to 40% latency gain with less or comparable 2D mesh network for 1024 cores. Hanhua et al. developed in this work [204]an algorithm called APW that resolved some limitations of the WCube architecture [203]. The addressed limitations were the poor scalability of WCube and its dependency to its recursive topology that is necessary to avoid deadlock issues. The proposed APW algorithm and its ramification DAPW were deadlock−free and guaranteed the reachability of partial network structures. The scalability problem was resolved by an incremental interconnection structure called IWCube that allowed the construction of the network without maintaining the complete topology of WCube.

Chifeng et al. developed a similar architecture called WNoC[205]. The network was based on a 2D mesh wired NoC called Network-based Processor Array (NePA) divided on equal islands. Each one of the island had a wireless router to assure wireless communication with the rest of the islands.

DiTomaso et al. developed an architecture called iWise[206]. The network was organized under 16 clusters to where four cores are attached. Clusters can communicate using high bandwidth wireless link for a one-hop 64 cores' system and expandable to 256 cores for a total of three-hop count. The same team presented later another WiNoC architecture called A-WiNoC that can increase the bandwidth in hotspots, locally and globally, using local and global controllers[207].

Recently, Dai et al. proposed a hybrid WiNoC architecture[208]. The considered 8x8 mesh-topology is composed of several subnets of four IPs with a star topology. Each one of the subnets had its proper wireless router and all the wireless routers are fully-connected. The authors adopted a multicast scheme for the data transmission. However, an energy-efficient technique was proposed. The authors used the power gating technique to deactivate the wireless routers that are not involved on the multicast transmission. Although this architecture introduced several new techniques, the considered topology is inflexible and is not suitable for recent dense and heterogeneous designs.

More recently, Zhao et al. proposed an irregular and reconfigurable WiNoC architecture to alleviate the density and the heterogeneity problems of the recent designs[209]. The authors proposed an application-aware placement of the wireless routers. Hence, an application-specific topology will be obtained. For a more efficient exploitation of this custom topology, the authors developed a new routing scheme called region-aided routing (RAR). The combination of the latter features led to better performances when compared to regular topologies WiNoC with table-driven or location-based routing algorithms.

ii. *Small-world wireless NoC*

Small-world wireless NoC, which are the second type of WiNoC architectures, were explored and studied by Chang et al. [210] and Deb et al. [211], respectively. They proposed a WiNoC design called mm-wave small−world wireless NoC (mSWNoC). The mSWNoC outperforms largely its classical NoC counterparts. Recently, Pande and Heo[194] extended and presented the former studies from[210] and [211]. The mSWNoC transmitting circuit fabrication results that consisted of an on−off Keying (OOK) modulator chip were explained [212]. Lately, Xinmin et al. have also unveiled the details of the receiving part that consisted of an OOK demodulator[213].

Extra studies in relation with mSWNoC were also conducted. In one hand, Wettin et al. investigated the performances and the thermal profile of mSWNoC[214]. In the other hand, Murray et al. conducted a study regarding dynamic voltage and frequency scaling (DVFS) using MROOTS and ALASH

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routing algorithms[215]. In relation with the DVFS, Wonje et al. proposed to prune as possible the underutilized voltages thus reducing the design of the mSWNoC[216].

To obtain the desired performances from WiNoC, flow control algorithms and fault resilient techniques have to be investigated. Ganguly et al. exploited the fault tolerance behavior of natural networks such as microbes' colonies and the internet to develop a fault tolerant architecture of a small-world WiNoC[217]. The authors demonstrated that even at high fault rates, the developed architecture showed an interesting resilience compared to wired mesh NoC [196]and WiNoC. Moreover, the authors presented an error control coding mechanism that can maintain the network reliability thus achieving similar high performances of its wired NoC counterparts[218].

iii. *Design space exploration for wireless NoC*

Design space exploration studies are necessary to build power-efficient and reliable WiNoC. To this aim, Mineo et al. [219]studied an adaptive technique to control the transmitting power at runtime for WiNoC. The authors integrated a specific block called VGA (voltage gain amplifier) which is responsible of controlling the transmitting power via the power amplifier. This technique was integrated into two WiNoC architectures that are iWISE [206] and McWiNoC[198]. The evaluation of the iWISE and the McWiNoC architectures was carried within Noxim simulator [220]. The authors provided results that showed a significant gain in power consumption compared to a baseline power-management scheme. Lately, a more detailed study of this technique was developed[221]. The authors applied their technique to an additional WiNOC architecture namely HmWNoC[211].

Similarly, Laha et al. conducted an extensive study followed by a general exploration of the design landscape for WiNoC transceivers at the physical layer[222]. In their work, the authors discussed several alternatives for the design of transceivers in term of the fabrication technology, not only for on-chip wireless interconnect but also for off-chip wireless networking.

In the same way, Abadal et al. explored the enhancement of broadcast-enabled multicore designs with WiNoC[223]. The authors proposed to use a hybrid NoC architecture that was composed of a WiNoC and a classical one. The WiNoC will be used as a global shared medium for data broadcasting while the classical one assured the remaining of the data flow. Additionally, an insightful discussion of the WiNoC state-of-the-art and related challenges was developed.

The design of fault tolerant and reliable WiNoC is more and more explored. Hence, congestion-aware and conflicts-free techniques for WiNoC are necessary. For example, Murray et al. investigated the impact of a congestion-aware routing in the network thermal performances[215]. Additionally, the authors combined this routing scheme with dynamic voltage and frequency scaling to build power-efficient WiNoC.

It is also important to develop design methodologies that are capable to consider QoS factors for WiNoC. Recently, Mansoor et al. [224] presented a design methodology to build fault-resilient WiNoC. The authors considered in their study transient and permanent faults. The proposed methodology combined an optimization of the network topology, a medium access mechanism and an error correction code to build a robust WiNoC. Dehghani and Jamshidi studied a similar approach[225]. First, the authors developed a strategy for an optimal placement of the WiNoC router. Second, they used several fault−tolerant communication protocols to test the efficiency of their WiNoC architecture.

d) RF-Interconnect

Another known direction to explore for emerging technology NoC is RF-Interconnects (also reported RF NoC). The established works by Socher and Chang [226] and later by Tam et al. [227] could be a good starting point to this section. The authors answered very carefully to the question on how RF-Interconnect can enhance future chips. In fact, the benefits are diverse and can be summarized in the following:

- In the first place, RF-Interconnect are completely scalable and compatible with current and future CMOS fabrication processes.
- Secondly, they are totally immunized against noise thanks to their higher modulation frequency starting from 10 GHz.
- Thirdly, they are a valuable solution to chips with multiple clocked IPs since frequency-division multiple-access algorithms (FDMA) can be used to assure a multi-carrier link. This is useful to modulate heterogeneous clock domains data and transmit them simultaneously but spectrally separated.
- Finally yet importantly, multicast simultaneous communication can be implemented on a single physical waveguide for many receivers.

In addition of the explanations exposed above, the authors provided realistic implementation results of some prototypes to facilitate the design exploration of RF-Interconnect based architectures.

Conceptually, this technique is similar to the macroscopic RF networks. It is based on transceivers and waveguides as propagation medium but rely essentially on integration technology when applied to on−chip or to chip-to-chip networks. Chang et al. [228] discussed this potential solution since 2001. Havemann and Hutch by, in their turn, discussed the other potential emerging solutions[229]. However, first proposals emanated later for off-chip connections from the works of Shin et al. [230, 231] and Chang et al. [232, 233]. Furthermore, there are other works that discussed on-chip interconnects such as in [234] and [227].

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i. *RF-Interconnect proposals*

Chang et al. conducted to the best of our knowledge, the first design exploration for RF NoC[234]. The study compared a baseline NoC of 10x10-mesh topology with the same sized architecture but enhanced with a Z-like shaped global waveguide. Shortcuts to the global transmission line were strategically placed to minimize the hop count among the distant routers. The proposal, called MORFIC, showed that for an extra area of 0.13 %, the latency was reduced by 22%, compared to the cited baseline NoC above. Moreover, Tam et al. developed a tri−band RF NoC fabric for a simultaneous, up to 10 Gb/s transmission rate[235].

Liping and Hanson studied the addition of an extra layer on the top or at the bottom of the silicon substrate called guiding layer[236]. Although the study focused on the physical characterization of the guiding layer, it demonstrated, first the feasibility and second the potential of such propagation medium for on-chip interconnects.

Last but not least, we can cite some recent efforts involving the use of Orthogonal Frequency Division Multiple Access (OFDMA) modulation to build an RF NoC. Such approaches were described successively in[237], [238]and[239]. In the first effort[237], a feasibility study of an architecture composed of 32 clusters that were connected with OFDMA RF-based NoC, was developed. Each of the clusters had 16 tiles with 4−cores each one, for a total of 2048 cores CMP. In addition, the authors developed an arbitration scheme that reduced the average latency by 3.5x. Drillet et al. exploited the OFDM RF NoC fabric to build a 4096 cores CMP sharing up to 20 GHz of bandwidth [238]. Hamieh et al. in their turn[239], conducted a design space analysis at the physical layer of the same OFDM RF NoC transmission line. A power study was established for an efficient communication with two different shapes for the transmission line (U- and X-like shapes). Recently, Brière et al. presented a similar architecture[240]. The OFDMA technique was used to maximize the use of the available bandwidth. Hence, lower network resources will be needed.

ii. *Design space exploration for RF−Interconnect*

As it was the case for the other emerging technology NoC, many design space exploration exercises for RF-Interconnects were also proceeded. Among the first studies, we can cite the established proposal for intra-chip RF-Interconnect that we had already explained earlier in [234], and also for inter-chip communication like in[241]. Despite the fact that the study in[241]was intended for chip-to-chip communications, the components which were modeled and analyzed in the study, such as waveguides and UWB transceivers, could be used similarly for intra-chip communication purposes. Schinkel et al. proposed a more representative example of the design space exploration at the physical layer[242]. The authors designed a transceiver that can be exploited on a RF NoC capable of up to 5 Gb/s data rate where differential twisted links were used. RF on-chip components that could be utilized for on-or off-chip communications such as transceivers were also studied in [243]and [244], respectively.

Recently, Pourshirazi and Jahanian presented a more developed study[245]. The authors proposed an algorithm for an optimal placement of RF resources in addition of a maximum utilization of the available RF bands. The results showed that routing congestion and critical delay were significantly reduced at power and area costs of 2.33 % and 11.89 %, respectively. Later, ValadBeigi et al. presented another NoC architecture based on a novel framework to reduce the delay and the power consumption[246]. The proposed architecture was a hybrid architecture composed of a conventional NoC along with supplementary RF nodes that might use dedicated shortcut paths for a fast data traversal between distant nodes. The mechanism was assured by a router architecture that had the five classic input/output ports (East, West, North, South and local) in addition of the RF Tx/Rx ports for radio-frequency based communication. Xiao et al. presented a similar exercise[247]. The author discussed key problems related to the design of hybrid RF NoC combined with 2D mesh NoC.

Finally, a very promising attempt was developed by Yu et al. in [248]. The authors proposed the expansion of RF-interconnect capabilities to vertical layers through partially hollow TSVs (air-gap-based coaxial TSVs). Compared to its dielectric counterpart, the modeled air-gap TSV had a smaller power and area consumptions thanks to its reduced hardware footprint.

e) Other alternatives for the NoC design

In this section, we review some of the original proposals or outstanding still in-progress works. Most of these works are based on substrate materials such as graphene or carbon nano-tubes (CNTs)

Previously in Table IV, we mentioned that WiNoC bandwidth might be increased to THz domain with CNTs. CNTs were investigated for on-chip interconnect for many years [249]. Recently, Kaushik and Majumder reviewed the evolution of interconnects from a technological perspective[250]. In addition, the authors provided an extensive study on the performances of CNT-based interconnect.

Brun et al. developed a study in relation with CNT-based antennas[251]. The authors verified their study with a practical methodology of a CNT growth process[252]. Thus, they proposed CNTs as an RF-interconnect propagation medium. In addition, CMOS compatibility experiences of the proposed CNTs were described to demonstrate that they could be adopted on conventional CMOS processes.

The organic substrate feasibility and further its productivity were also widely investigated. In this

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direction, grapheme-based electronics was not only stated for grapheme-based transistors[253], but also in the particular cases of THz enabled nano-antennas [254, 255] and for wireless NoC[256]. In the last work, the authors studied the feasibility of grapheme-based WiNoC. Moreover, a design space exploration was initiated to study a grapheme-based WiNoC and ONoC hybrid architecture [257] and by consequence these advancements have attracted the industry [258]. More details of this attempt are provided in [259].

As it was the case in Anthony's work[100], the industry contributed on enriching the intra-chip connection paradigm, as well as the inter-chip one. In this context, Mitchell et al. proposed a proximity communication (PxC) scheme[260]. The concept was based on capacitive coupled channels of up to 4 Gb/s for each one, with less than 2.5 mW/Gb/s (the same concept was also used in a 3D NoC proposal [78] (refer to Section 3.2). The authors claimed that such inter-chip interconnect fabrics could be a viable solution to stack heterogeneous chips such as DRAMs and processors chips. However, they concluded on the fact that augmenting the number of connected chips degrades the overall system latency due to the on-chip metal wiring and they proposed optical interconnects as a potential solution.

f) Summary

In this section, we have reviewed the available literature for emerging technology NoC. We have covered the principal directions in this area namely 3D, Optical-Photonic, Wireless, and Radio-Frequency NoC, in addition of some original alternatives. For a more convenient reading, Table II provides a classification of the studied works in the previous paragraphs.

Table II: Summary of Emerging Technologynoc Proposals

		Relatedworks	Design space exploration efforts
3D NoC		[4][67][68][69][70][69][71][72][73][74][75][76][77][78][79][80][81][82, 83][84]	[85][86][87][88][89][90]
Optical	All-Optical	[104][105][106, 107][108][109][110][111][112][113][114][115][116][117][118][119][120][121][122][123][124][125][126][127][128][129, 130][131][133, 134][135][136, 137][138, 139][140][141][142][143][145][146][147][148][149][150]	[1][113][164][165][166][167][2][168][169][170][171][143][172][173][174][175][176][177][178][179][180][181][175][182][178][183][180][184][185][186][187]
	Hybrid	[151][152][153][154][153][155][156][157][158][159][153][160][161][162][163]	
Wireless NoC		[189][190][191][192-194] [195][44][196][3][45][197][198][199][200][201][202][203][204][203][205][206][207][208][209][210][211][194][210][211][212][213][214][215][216][217][218]	[219][206][198][220][221][211][222][223] [215][224][225]
RF –I		[234][235][237][238][239][238][239][240]	[241][242][243][244][245][246][247, 248]
Other Alternatives		[249][250][251][252][253][254-256][258][259][100][260][78]	

IV. Conclusion

In this work, we reviewed emerging technology NoC proposals for the last ten years. This includes 3D NoC, Optical NoC and Wireless NoC. We also discussed several other alternatives for the NoC design such as graphene based NoC.

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