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Reduced Size Single Switch Power Factor Correction Circuit

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Abstract

This article presents a new design of active power factor correction (APFC) circuit that can be used in single phase rectifiers. The proposed circuit provides almost a unity input power factor (PF) which contributes significantly in reduction of the total current harmonic distortion (THDI) as it eliminates the third harmonic component effectively from the input current.The most important attribute of this circuit is the small size and numbers of components (one switch, small size (L C) and a diode), which have been designed to get a unity PF at the AC source side. Therefore, the new circuit is cheaper, smaller size and lighter than other conventional PFC circuits.In addition, the new proposed circuit is a snubber-less and uses reasonably low switching frequency which reduces switching losses and increases efficiency. The circuit has been designed and simulated using Lt-spice simulink program.

Index terms— active power factor correction (APFC), AC - DC converter, total harmonic distortion (THD).

1 Introduction

ingle phase AC/DC rectifiers with a large electrolytic capacitor are commonly used for manufacturer and business issues. The main purpose to use diode rectifiers is to operate the switching power supply in data processing apparatus and to operate low power motor drive systems [1].

The large capacitor draws current in short pulses, which brings in a lot of problems including decreasing in the available power, increasing losses and reduction of the efficiency. In the conventional way of design, the capacitor voltage preserves the peak voltage of the input sine wave until the next peak comes along to recharge it [2].

The only way to recharge the capacitor is drawing the current from the input source at the peaks of the source waveform as a long pulse which includes an adequate amount of energy to nourish the load until the next peak. This is happens when the capacitor draws a large charge during short time, after the slowly discharge of the capacitor into the load. Therefore, the capacitor's current draws 5 to 10 times of the average current in 10% or 20% of the cycle period. Consequently, the source current has narrow and long pulses and the effective (r.m.s.) value increases [3], [4].

Customers with a large number of nonlinear loads also have large neutral current rich in third harmonics current. In order to increase the PF, decrease the losses and save the energy, then the input current harmonics (specially the third order harmonic) have to be eliminated. Several methods and techniques have been proposed to solve the problem of a poor power factor, which can be classified as active and passive methods [5].

Passive PFC circuits are generally simple, fewer components, smaller size and easy to design for small rating power (less than 200 watt). However, its bulky and not economical for large power ratings and the input power factor is (0.6 -0.7) and THD = 150% in best conditions without using big size elements [6].

Active PFC circuits, can considerably diminish losses and costs associated with the generation and distribution of the electric power and significantly improved power quality. Therefore, APFC circuits are receiving more and more attention these days because of the widespread use of electrical appliances that draw non sinusoidal current from the electric power systems. However, PFC circuits require additional, more expensive and complex components [7]. The author in [8], designed a novel PFC circuit that depends on the principle of limiting the work of the main capacitor in a manner which can eliminate the third order harmonic and improve the input

PF into 0.99. However, this design has been used two Mosfets and high switching frequency equal to 200 KHZ which may increase the switching losses and reduce the efficiency.

In this paper, a new design of PFC converter has been introduced and presented in figure (1). The new design is depending on the flexibility of the parameters' variation which produces low harmonics, high input PF and high efficiency.

The new proposed design, reduces the required number of components into one Mosfet switch with low switching frequency equal to 20 KHZ, and uses small value of inductor which is smaller more than 96% of the inductors used in conventional boost PFC circuits, because the new proposed design focuses on shifting the harmonics components to the high frequency region and consequently eliminating the third order harmonic current, therefore the cost, the weight and the size of the new circuit will be reduced hugely.

The description of the circuit, operation topology, control circuit and operation stages are all described in section (II). The details of system's parameters are described in section (III). The discussion of simulation results and assessment are presented in section (IV), followed by an overall conclusion in section (V). New proposed APFC circuit (V S) is the input DC source (represents AC single phase connected to full bridge rectifier), connected in parallel with LC resonant branch and MOSFET switch (SW) in parallel with the load. A control circuit has been designed in order to control the switching process.

2 b) Operation Topology

The new proposed circuit has the ability to control the working period of the capacitor. Consequently, the value of the input power factor, THD I of the source current waveform and the value of the output ripple voltage can be controlled as well through using one switching devices.

The principle of this design is depending on the distributing of the working time intervals of the capacitor into two regions, at the beginning (0 -t 1) and at the end (t 4 ???) via using control circuit. This smart switching pattern would eliminates the third order harmonic component and improves the input PF as the third order harmonic is the most significant component in single phase systems.

This design uses a minimum number of components and minimum values of (L) & (C) a s capacitor turned off on the middle of each cycle, which shift the harmonics components to higher frequencies. consequently, reduces the size and the cost of the new proposed circuit.

This circuit is snubber-less circuit, because the freewheeling diode (FWD) presents an alternative path for the discharge current of inductor (I L), so can the capacitor keep charged. Accordingly, (FWD) can avoids the negative part of I L and helps (C) to act as a snubber circuit in order to prevent the inductor's voltage (V L) to increase more than rated value of the source voltage, in this way (C) will protect the MOSFET switch from being burned in the effect of the high voltage spikes which may happened without the FWD.

3 c) Control circuit

A simple designed control circuit, as shown in figure (2) has been investigated in order to derive the MOSFET switch and control the switching frequency and duty cycle. because L, C and the load are series in this mode.

then the value of V L is approximately zero because the value of L 1 is very small (few micro henres). Year 2017 F Fig. **??**:I C = C dV C dt = I L = I Load = Vout R ? V Load = V out = V C + V L ? V L = L di L dt ? V out ? V C

The full time period of the input source current waveform (I S) is shown in figure (4) with the details of nine time modes.

2) Second mode: For the time period t 1 ? t < t 2 , when V S >V C1 , and SW is ON. At this mode, (L) discharges its current to (C) until being zero (at the t d moment), while the inductor voltage V L is equal to V C and remains charged. This topology dose not require a snubber circuit as V L has been prevented.

f r is the resonance frequency. At this mode, the load is fed by the source. Practically, a damper circuit (R=5 ? & C=1 nF) can be connected in parallel with the freewheeling diode in order to eliminate the resonance current (I0) totally, however, 0.1 % of power losses can be increased in the circuit as a circuit of 3 kw output power, has only 3 watt losses in the damper circuit which is negligible. The modes (2,3,4) are repeating every ON/OFF switching pulse of SW.F V S = V C + V L = V C + L. di L dt I S = I C + I Load = C. dV C dt + I Load ? V L = V C & I L = I C = C dV C dt ? X L = X C 2?f L = 1 2?f C ? f r = 1 2? ? LC = 1.59KHz V L = L di L dt = V C I S = I Load = Vout

The figure (6), shows the full picture of V C , V out , V L &V D waveforms. V C is in red color, V out is in brown color, V L is in green color, and V D is in blue color. V C still charged and slightly charging but approximately constant due to very small .

V C1 remains charged and considered as a constant value due to the value of I C1 is approximately zero, then the value of dVC1 would be very small.

The modes (6,7,8) repeat themselves every ON/OFF switching of the MOSFET. 9) Ninth mode: For the time period t 4 ? t < 10 ms., when V C >V S . SW-ON/OFF, the circuit is shown above in Fig. **??**3-a).

L & C are discharging while the R-load is fed by the main capacitor.

All the derived equations in the first mode are valid for this mode.

III.

4 System Parameters

The proposed circuit has been simulated in LTspice program and the parameters have been specified as the following table: Power factor has been calculated by using equation in [9], P.F =Table I: System Parameters IV.

5 Simulation Results and Assessment

? I L = Vout R V Load = V out = V C + V L Inductor (L) R Internal Ser. = 2.236 m ? R Internal Par. = 1413 ? Capacitor (C) ESR = 0.035 ? ESL = 0 ? MOSFET IPP070N8N3, N-channel V ds = 80 V, R ds = 7m ? Freewheeling diode Schottky, (UPSC600) V Breakdown = 600 V Parallel diode Schottky, (MBR745) V Breakdown = 45 V Load Resistive 20 ? 2)1 ? 1+(T HD I) 2

The total input power, has been calculated via below equation [10]:

The maximum efficiency is 98.68% when input power is 2.5 kw when R-load = 20 ? and (L) is 20 ?H.

6 Fig. 7: Different load values with PF and

It can be concluded, from table (I) and figure (7) that the values of ( ) and input PF, inversely proportion with the increasing of the load value.

7 3) Table (II) shows the relationship between different

inductor values comparing with with P in , P out , _and input PF, when R-load = 20 ? and f sw = 20 Khz. It can be concluded that, f sw can be kept around (10 -20) KHz in order to get approximately unity PF (0.98) at the input AC side when (L) is 20 ?H for 2.5 kw output power. As it is shown in figure (10), the third order harmonic is not exist at the input current waveform, and the only harmonic orders shown are the 5th and 7th order harmonics. This is because (C) was OFF at the middle of the waveform (t 2 ? t 3) and the load was fed by the source. 6) In the case of the absence of freewheeling diode in the time intervals t 1 ? t < t 2 and t 3 ? t < t 4 (which represent the 2nd and 6th modes), the equation of inductor's voltage is:

(D) is the duty cycle of (SW) and because of the switching frequency (f sw) is (20 KHz), therefore V L F I t = I 2 1 + I 2 h P in = V t .I t .P F ? ? L(uH) P in (W) Pout (W) ?(V L = L di L dt = L.di L .fsw D

would be a very large value at this moment. Consequently, V L may be a reason for huge spikes on MOSFET's terminals and may burn the switch. 7) Generally, in this situation a snubber circuit would be proposed as a solution to suppress the high frequency spikes and to protect the MOSFET switch. However in this circuit, the main capacitor (C) would be act as a snubber circuit because of the existence of the freewheeling diode (FWD), which makes V C charges on the negative value of V L and prevent high voltage on the terminals of the MOSFET when its in open the status. As shown in figure (11), the inductor voltage does not increases more than 140 V P-P in spite of that the source voltage is 311 V P-P , because of the small value of (L). The inductor's value used in the literature in [12] for a (3 kw) output power using interleaved boost converter was (270 ?H), while the value of inductor (L) in the new proposed circuit is (20 ?H) for the same power ratings. This reduction of the inductor's value will effectively contribute in reducing the size, weight and the cost of the converter. 9) One of the significant features of this design, is that the inductor's current is not related to the value of source voltage (except in the 2nd and 6th mode) as usually happens in PFC circuits. This advantage can be utilized in order to reduce the value of (L) into few micro henrys and avoid high V L values. Consequently, can reduce the size, weight and the cost effectively. 10) Practically, the internal capacitor of the used diodes in the circuit would combine with the stray inductors and compose a parasitic resonant frequency (f p). In order to get rid of the bad effects of (f p), the rising time (t r) or the falling time (t f) can be changed, or alternatively a damper circuit can be added to the circuit or using clamping diodes and that's require additional components and complex design [13]. 11) The inductor works like a proper choke or current limiter due to the high negative value of inductor voltage (V L) as its in counter direction of capacitor voltage (V C).

(L) charges in the time period t 1 ? t < t 2 because V S >V C On other hand, for the time period t ? t < t 3 , IL is zero because L and C are reverse biased. While, for the time period t 3 ? t < t 4 , (L) discharges as a positive current because V S >V C . However, for time period t 4 ? t < t 1 of the next period, L discharges as a negative current because V C >V S and the R-load would be fed by I L which is the same capacitor's current (I C = I L).

V.

8 Conclusion

According to the simulation's results, the new proposed PFC circuit was able to reduce the THD I to 17% with a unity power factor (0.986) at the input side and increases the efficiency to 98.68%.

The topology of reducing the conduction time of the main capacitor via dividing the waveform into three regions ONOFF-ON, can improve the efficiency, the input PF and reduce the THD I at the input side.

In addition, preventing the capacitor (C) from work in the middle of the time period for about half of the time will eliminate the third order harmonic and shift the 8) The required value of the inductance for the same voltage and power ratings in three level boost converter is (L), while the size would be doubled with the using of two inductors (2x2L) for the interleaved boost converter, on the other hand, the inductance would be doubled again (4L) for the conventional boost converter [11].

harmonics current to the high frequency region and that's will contribute in reducing the size of magnetics due to the small value of the inductor 20 ?H which produces a small amount of losses. Accordingly, the small inductor will effectively reduce the size and weight as used just one MOSFET, so the rectifier is not bulky any more, and thats reduces the cost of the converter. Another advantage of this circuit is that the snubber circuit is not compulsory because of the presence of freewheeling diode. In addition, the design is considered as a high efficient design due to minimum number and small values of components and simple circuit design due to uses single switch.

The performance of this circuit has a wide range of flexibility because, the output ripple voltage, the input PF and THD I can be improved via controlling the values of duty cycles of (SW), (L) and (C).

From graphical waveforms and tables of results analysis for different values of R-load, inductor (L), and switching frequency, can be concluded that the increasing of inductor value (L) and values required in order to get a constant unity power factor, small THD I and high efficiency.

VI. [1] [2] [3] [4] [5]

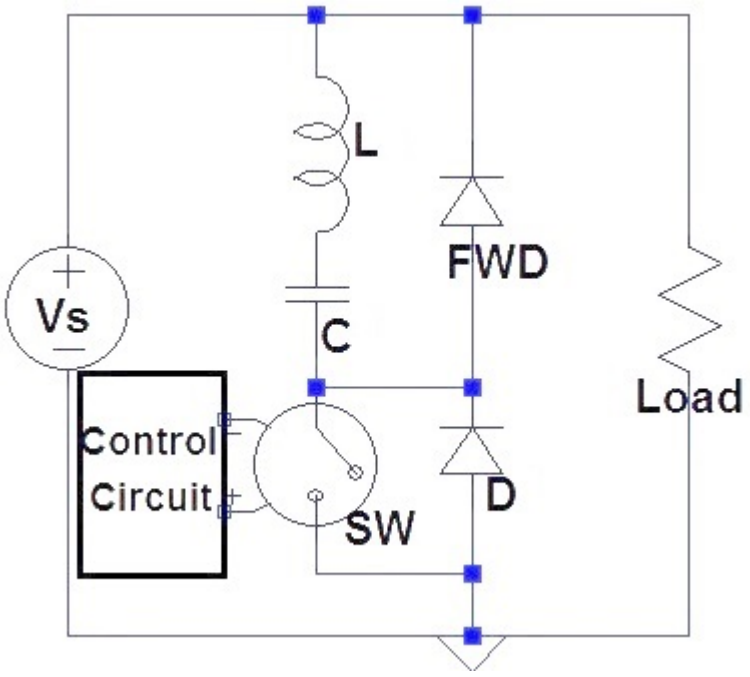

Figure 1:

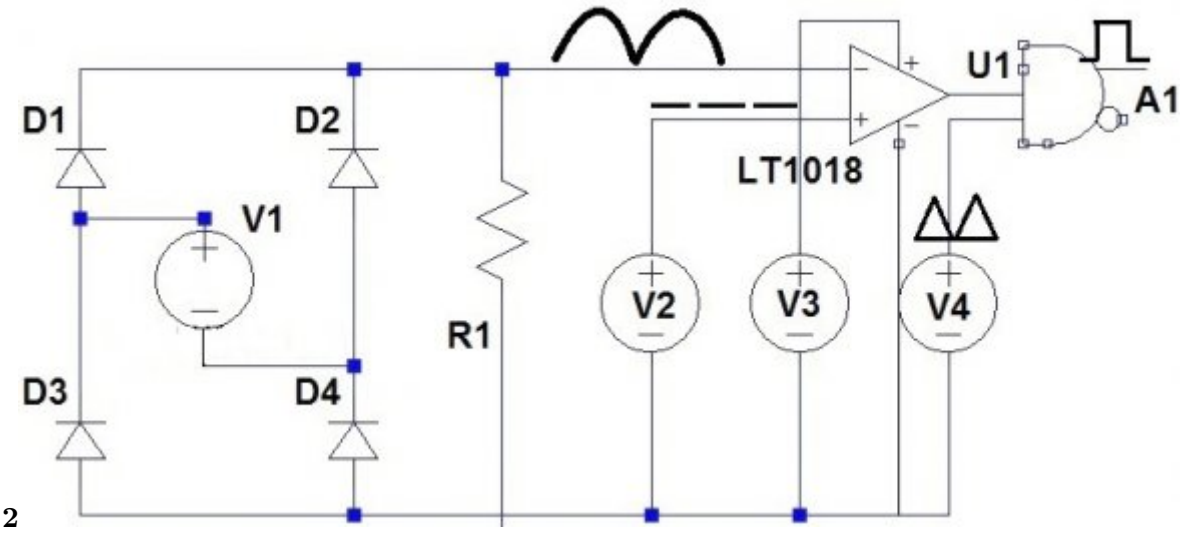

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Figure 2: Fig. 2 :

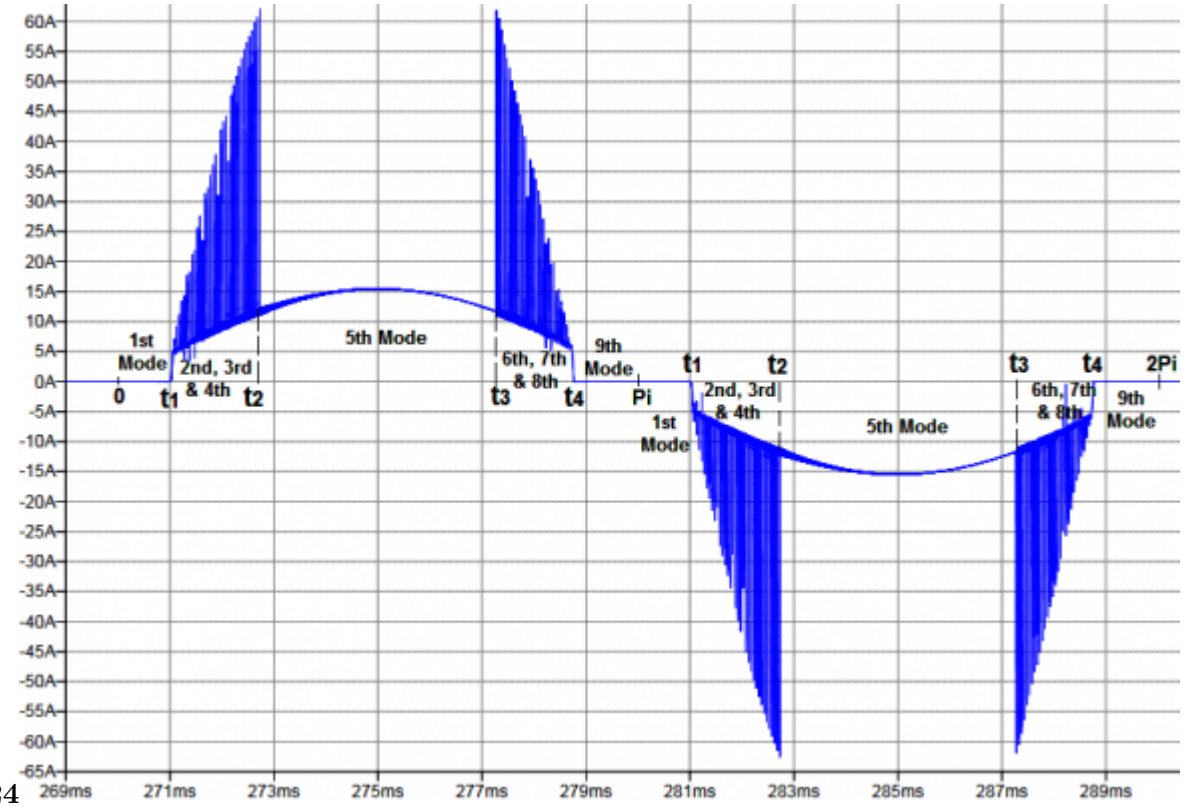

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Figure 3: t 2 ,Fig. 4 :

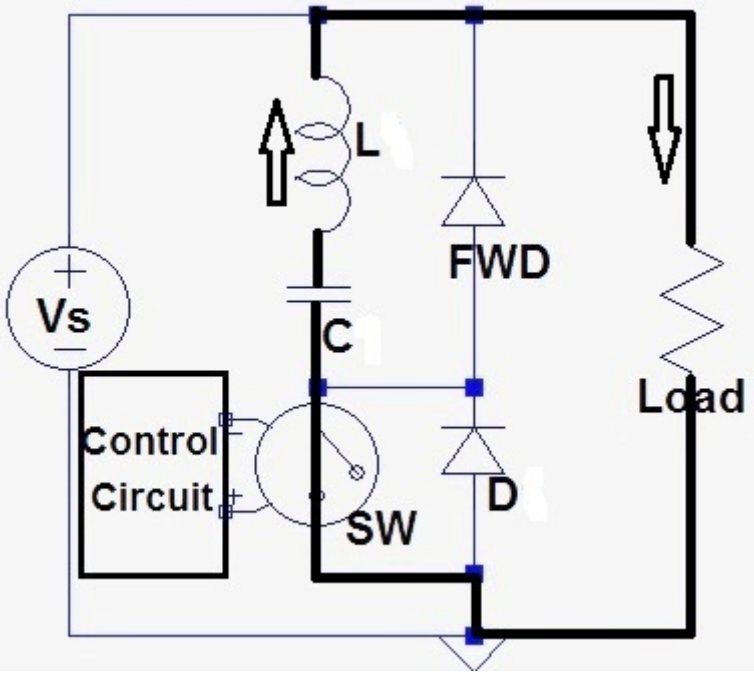

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Figure 4: 4)

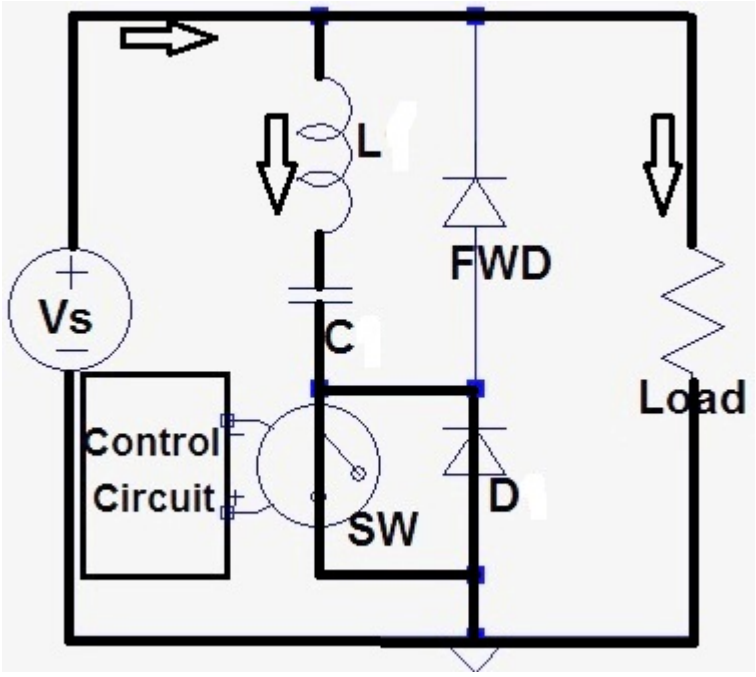

Figure 5: R

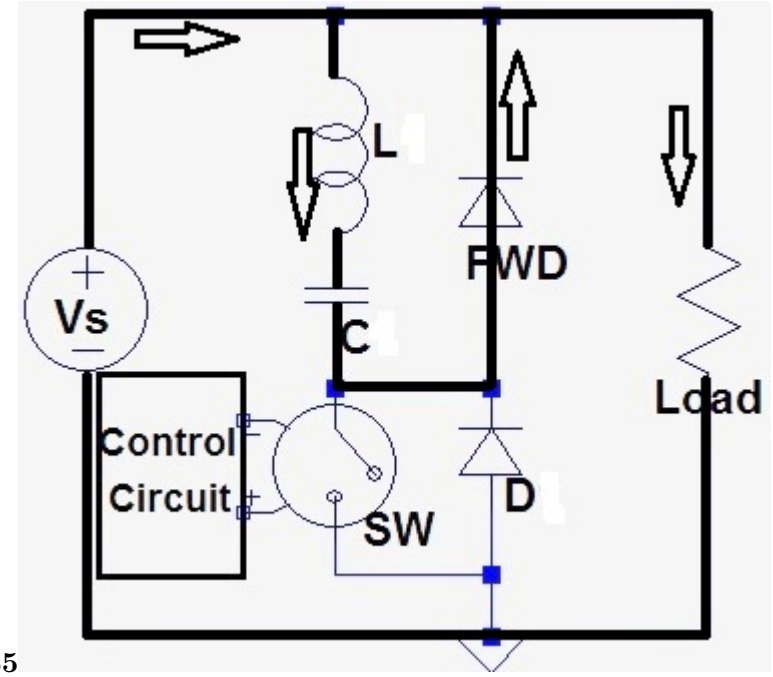

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Figure 6: Fig. 3 :Fig. 5 :

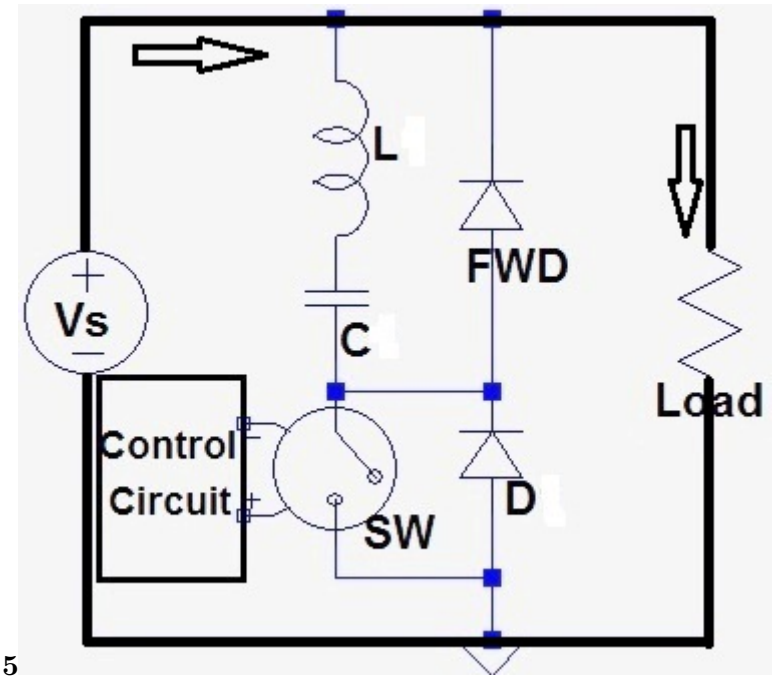

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Figure 7: 5)

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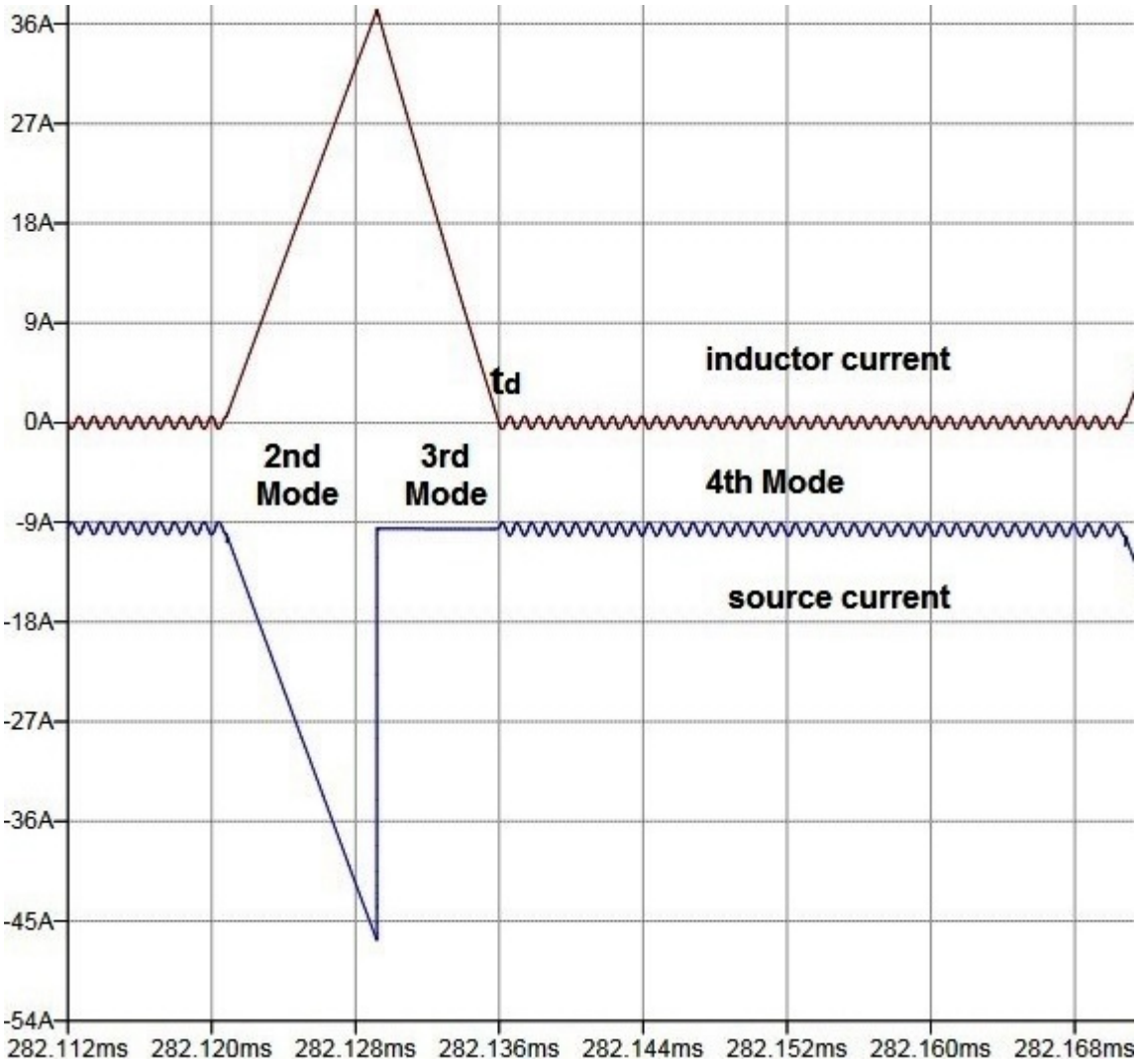
36A
27A
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9A
0A
-9A
-18A
-27A
-36A
-45A
-54A
282.112ms
282.120ms
282.128ms
282.136ms
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2nd Mode
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4th Mode
source current

Figure 8: I

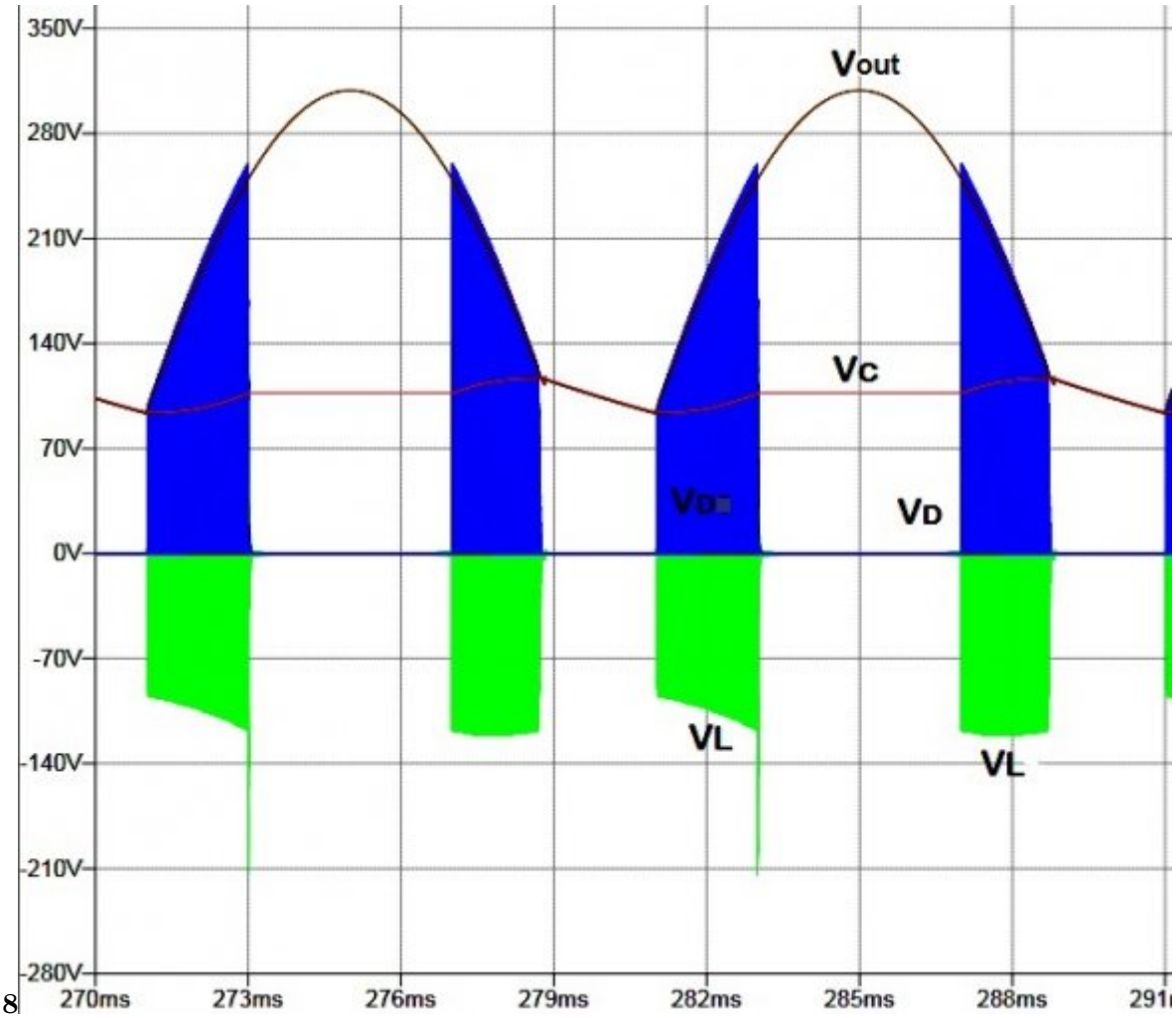

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Figure 9: Fig. 8 :

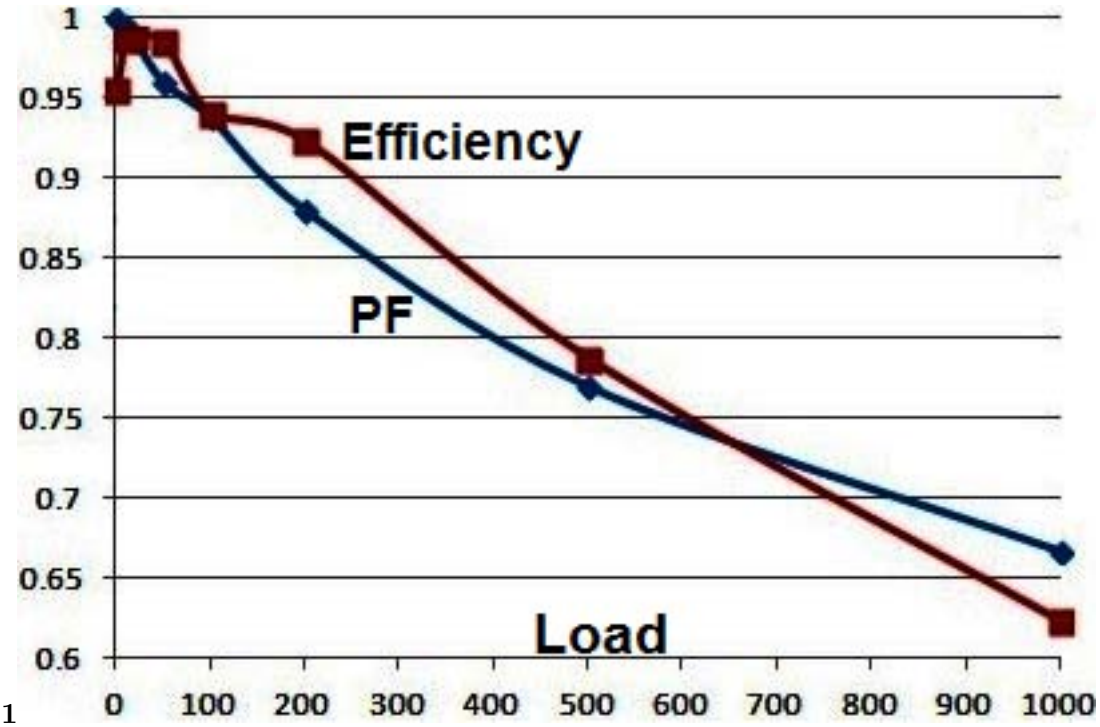

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Figure 10: ?Fig. 9 :Fig. 10 :Fig. 11 :

6

At this mode, (C) is charging while V L is equal to V C
until L fully discharges its current into zero ampere
at the time of (t d).
All the derived equations in the 3rd mode are valid
for this mode.
8) Eighth mode: For the time period t 3 ? t < t 4 , when V S
>V C1 , SW is OFF, for period (t d) until the next ON-
pulse for SW 2 . The circuit is shown in figure (3-d).

[Note: S >V C , SW is ON. t 4 is the moment when V C is greater than V S . The circuit is shown in figure(3-b). At this mode, C and L are charging and the load is fed by the source. All the derived equations in the 2nd mode are valid for this mode.7) Seventh mode: For the time period t 3 ? t < t 4 , when V S >V C . The circuit is shown in figure (3-c).]

Figure 11: 6)

II

R(?)	P in (W)	? Pout (W)	? (%)	THD(%)	? PF
1	46354.5	44260	95.48	5	0.999
10	4920.2	4851.5	98.6	11.6	0.994
20	2506	2473	98.68	17	0.986
50	1038	1021	98.36	28.4	0.96
100	543.48	525	96.6	37	0.938
200	292.68	269.6	92.1	52.4	0.886
500	141	110.75	78.55	83.2	0.77
1000	90.2	56.1	62.2	111.7	0.667

Figure 12: Table II :

III

It can be concluded, from table (II) and figure (8) below, that the value of and PF, directly proportion with the increasing of inductor value.
4) Table (III) shows the relationship between different switching frequencies of MOSFET comparing with P in , P out , and input PF when R-load = 20 ? and (L) is 20 ?H.
It can be concluded from table (III) and figure (9) that, the value of and PF directly proportion with the value of f sw .

Figure 13: Table III :

.1 Acknowledgment

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