Global Journals LaTeX JournalKaleidoscope™
Artificial Intelligence formulated this projection for compatibility purposes from the original article published at Global Journals. However, this technology is currently in beta. *Therefore, kindly ignore odd layouts, missed formulae, text, tables, or figures.*

Modelling and Simulation of Microcode based Built-In Self Test Technology for Multiported Memory

Miss. Musle Dipali B.[1] and Miss. Musle Dipali B.[2]

[1] Bharati vidyapeeths college of engg for women pune

Received: 10 December 2016 Accepted: 1 January 2017 Published: 15 January 2017

Abstract

Now a day?s embedded memory area and memory density is increasing. Due to this problem of fault is growing exponentionally.It is necessary to detect and repair those faults. There are different methods to detect the faults present in memory. Asynchronous P-MBIST method is used to detect the faults. Simulation result includes asynchronous P-MBIST which detect mismatch of data occurred and it is shown by high fault pulse. To correct the detected fault redundancy circuit is used. This system is implemented using FPGA platform.

Index terms— built-in-self test (MBIST), built-in-self repair (BISR), asynchronous P-MBIST, microcode MBIST multiported memory, redundancy logic array, field progr

1 I. Introduction

ccording to the ITRS 2015,Now a days the memory area is increasing than logic area in SOCs.Fig. **??** [1] shows that shrinking the technologies give rise to defect and new fault models.Thus, the new trends in Multiported memory testing will be driven by the following items. BIST: The new fault and new defects eliminate using BIST. The only solution that allows at-speed testing for embedded memories, it has generate fault detection and coverage, the higher repair efficiency only detecting the faults is no longer sufficient for SOCs so memory repair is also necessary for this purpose both diagnosis and repair algorithm are required. BISR: Combining BIST with efficient and low cost repair schemes in order to improve the yield and system reliability as well.

Fig. **??** : Embedded Memories in Future SOCs [1] Auhtor ? ?: Department of Electronics and telecommunication Bharati Vidyapeeth's College of Engineering for Women Pune, 43 Savitribai Phule Pune University. e-mails: srpatil44@gmail.com, dipali.musleb@gmail.com There are two methods which are efficiently used. These methods are as follow:

2 II. Related Work

Dr. R.K. Sharma et al. [2] introduced Redundancy Array Logic and BISR mechanism used to low cost repair the fault and to improve the system reliability.

Bo-Cheng Charles Lai et al. [4] introduced designs of multiported memories that leverage BRAMs have been proposed to attain better utilization of FPGA resources as well as system performance. BRAMs in an FPGA can support two access ports that can be used as either a read or a write port.

3 A

Global Journal of Researches in Engineering ( ) Volume XVII Issue II Version I Yash Jyothi et al. [1] introduced Asynchronous P-MBIST method for fault detection and repair of multiported memory. The main advantage is to get power efficient P-MBIST, it is being proposed to use handshaking signals instead of using clock and implemented on FPGA. Clocks are used to synchronize the test blocks on chip and handshaking signals are used to communicate between blocks of test controller.

4 III. built-in self test (bist)

Memory Built-In Self Test is test circuitry used to test on-chip memory devices. It contains finite state machine to generate test vectors to test vectors to test memory during test mode. Test coller includes Address, Data, read/write control. This address, data and read/write control signal is given as input to comparator and multiplexer. Multiplexer uses two modes of operations: Normal mode-In normal mode memory acts as a normal memory. Test Mode-During test mode test coller provides data and address to memory for testing purpose. In test mode while performing read operation data from test coller and output of memory are given to comparator for fault detection. Then, comparator compares test vectors with memory output. If, memory is working properly then, No Fault is detected and it is declared as memory is fault free but, if fault pulse becomes high it shows that memory under test is faulty.

5 Implementation of Asynchronous p-mbist

The block diagram shown in Fig. 3 **??**. [1] Table No.1: Microcode Instruction [1] V.

6 Flowchart of Asynchronous p-mbist

The flow of asynchronous P-MBIST is as shown in fig . **??**, fig. **??**

7 Asynchronous p-mbist Simulation

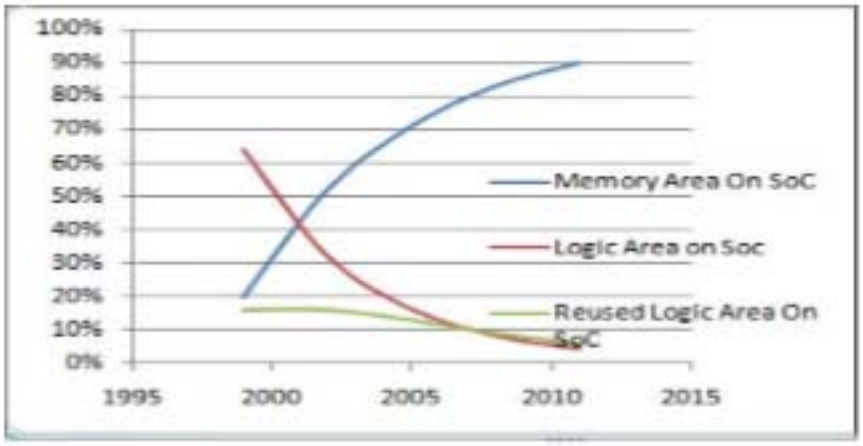
The simulation of asynchronous P-MBIST is depending upon request signal and mode. Output Response: Normal Mode: When mode=0, MUX selects normal mode, then test controller is off so as comparator is off. At this moment memory acts as normal memory without under test and generates external address and data if rw=0(i.e. reads address and corresponding data).During this mode as comparator is off, no fault pulse is generated. In this mode, memoutdata (memory output) data is data (External data) provided for normal memory operation. Test Mode: If mode=1, Memory is under test. If req=1, microcode instruction storage generates Read/Write control for test collar. Test collar writes data if tcrw=0 otherwise read to memory through MUX. The data from test collar and output of memory is compared in comparator. If mismatch happens at output of comparator, comparator generates fault pulse=1 otherwise fault pulse=0 [1]. During the normal mode each incoming address is compared with the address field of programmed redundant words. If there is a match, the data field of the redundant word is used along with the faulty memory location for reading and writing data. The output multiplexer of Redundant Array Logic then ensures that in case of a match, the redundant word data field is selected over the data read out (= 0) of the faulty location in case of a read signal. This can be easily understood by the redundancy word detail shown in Figure 7. VII. Results

8 VI.

9 Repair Module

10 Single port Memory

The single port memory support single read and write operation. 1 2 3 4



2

Figure 1: Fig. 2 :

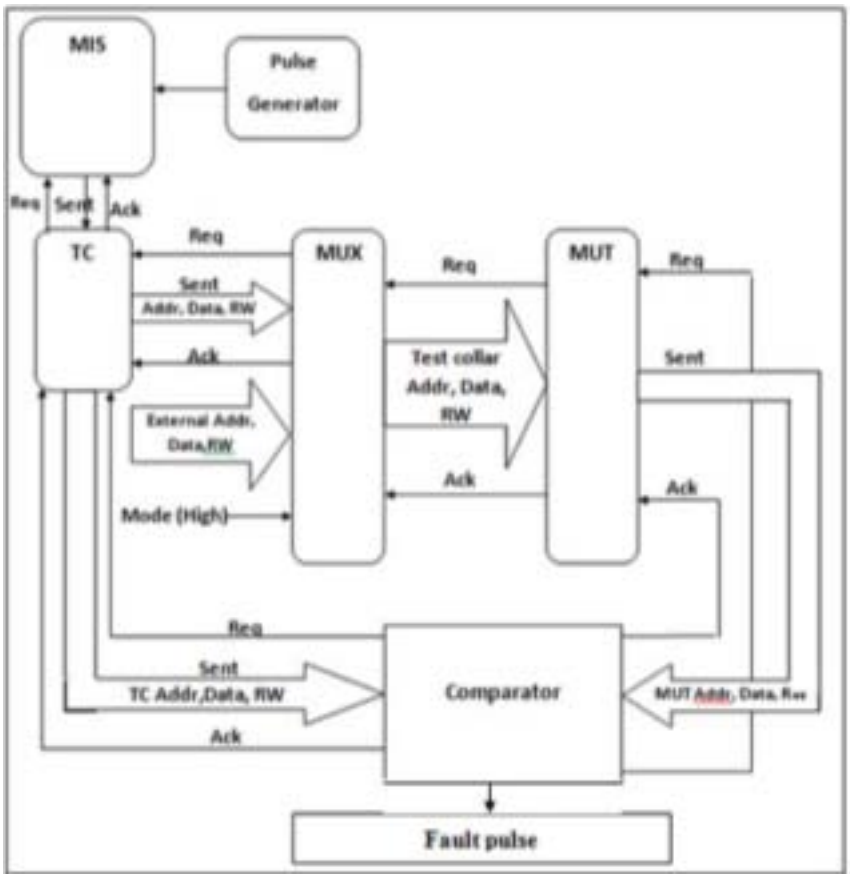


Figure 2:

3

Instruction	Description
R0	Read is low so no read operation occurs
R1	Read is high so read operation occurs
W0	Write is low so no write operation occurs
W1	Write is high so write operation occurs

Figure 3: Fig. 3 :

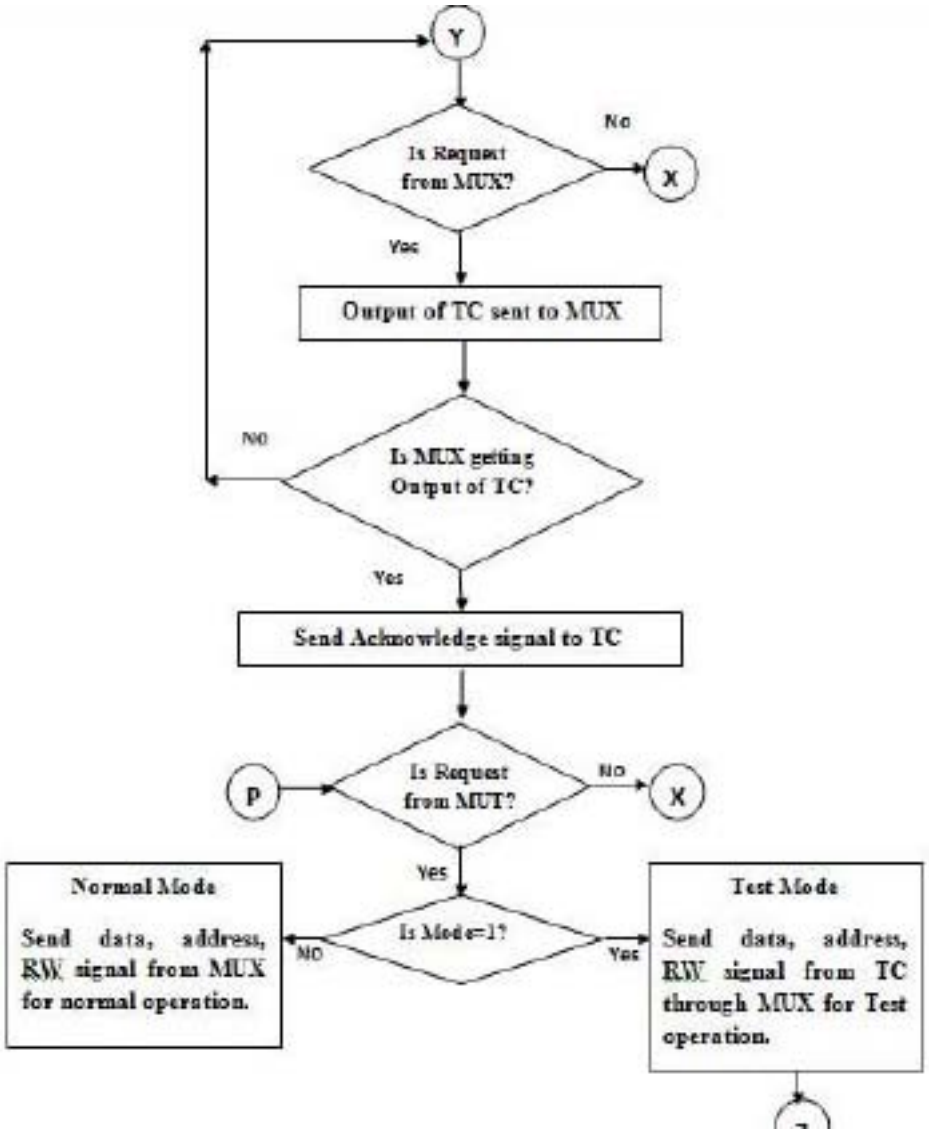
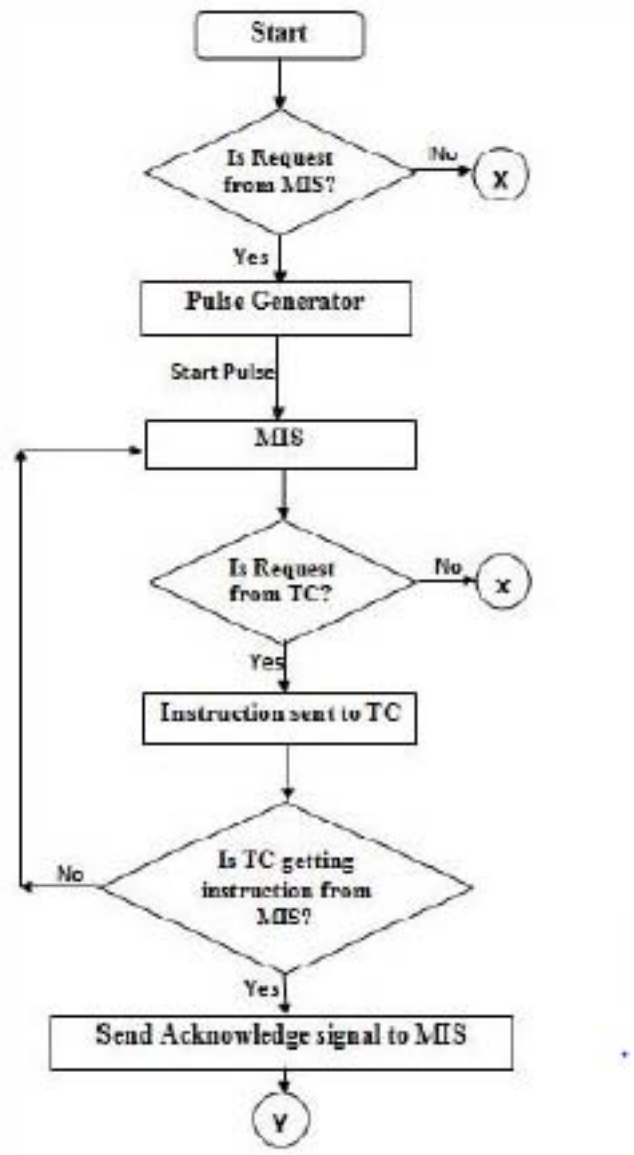
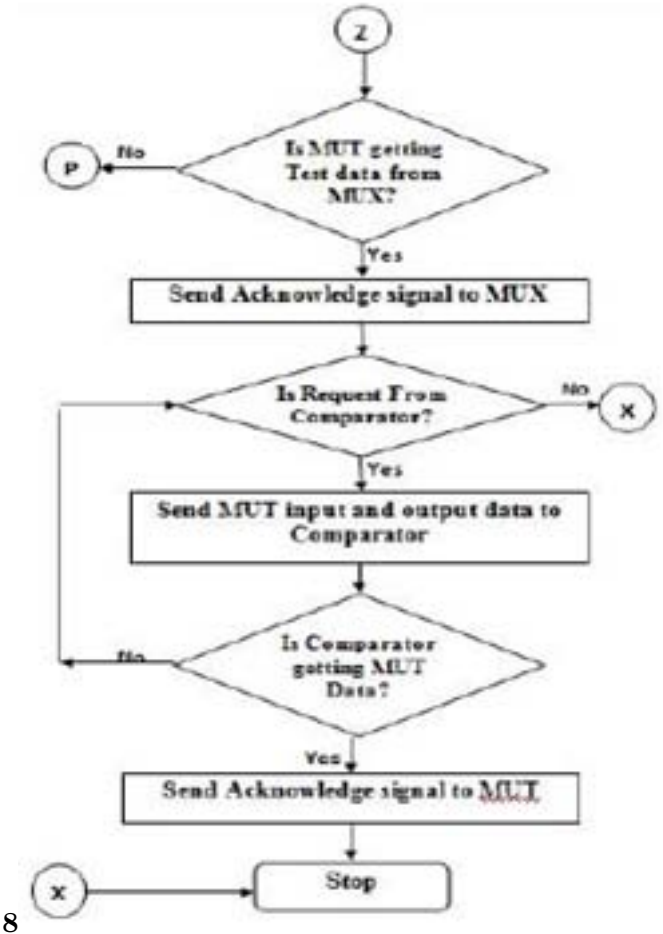


Figure 4: Address



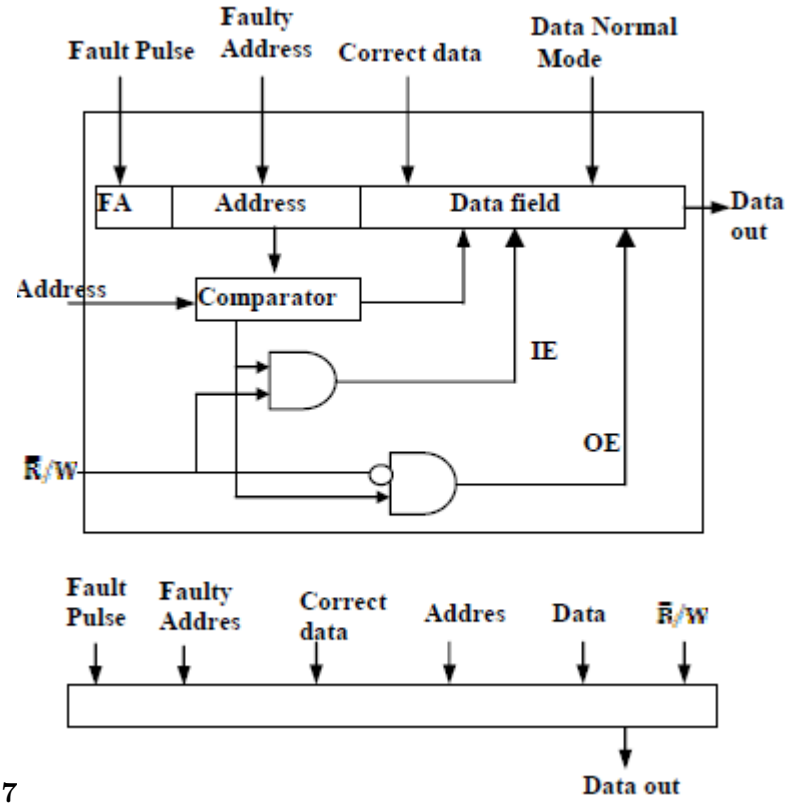
456

Figure 5: Fig. 4 :Fig. 5 :Fig. 6 :



8

Figure 6: Fig. 8 .



7

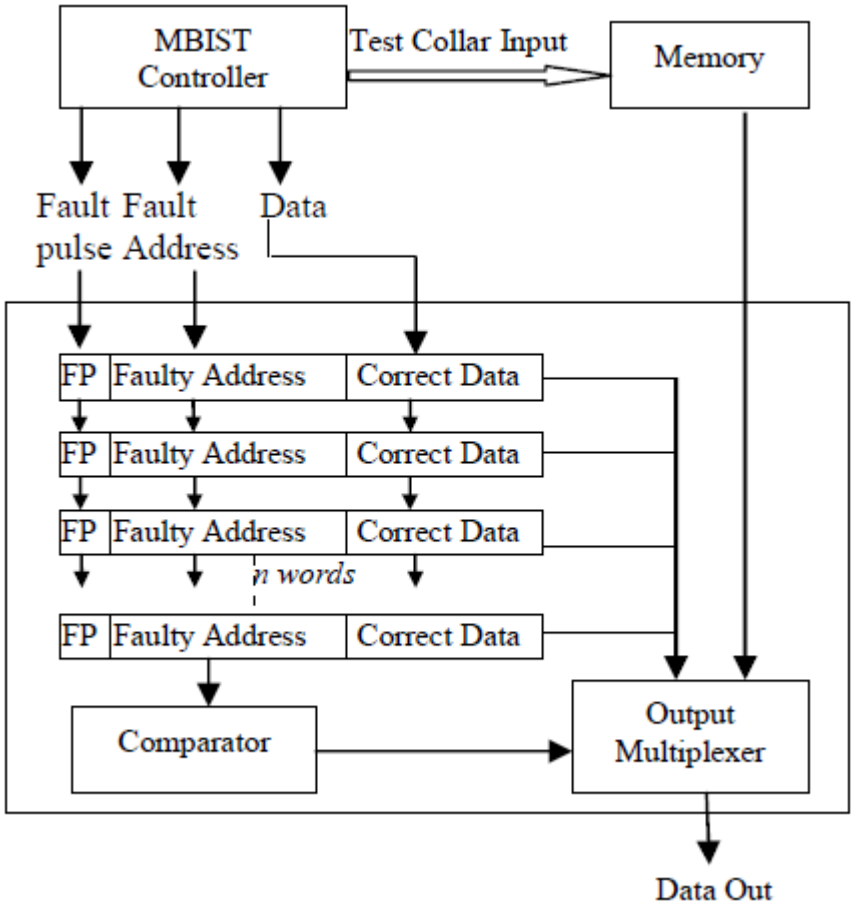
Figure 7: Fig. 7 :

[1]Year 2017 F © 2017 Global Journals Inc. (US)

[2]Modelling and Simulation of Microcode based Built-In Self Test Technology for Multiported Memory © 2017 Global Journals Inc. (US)

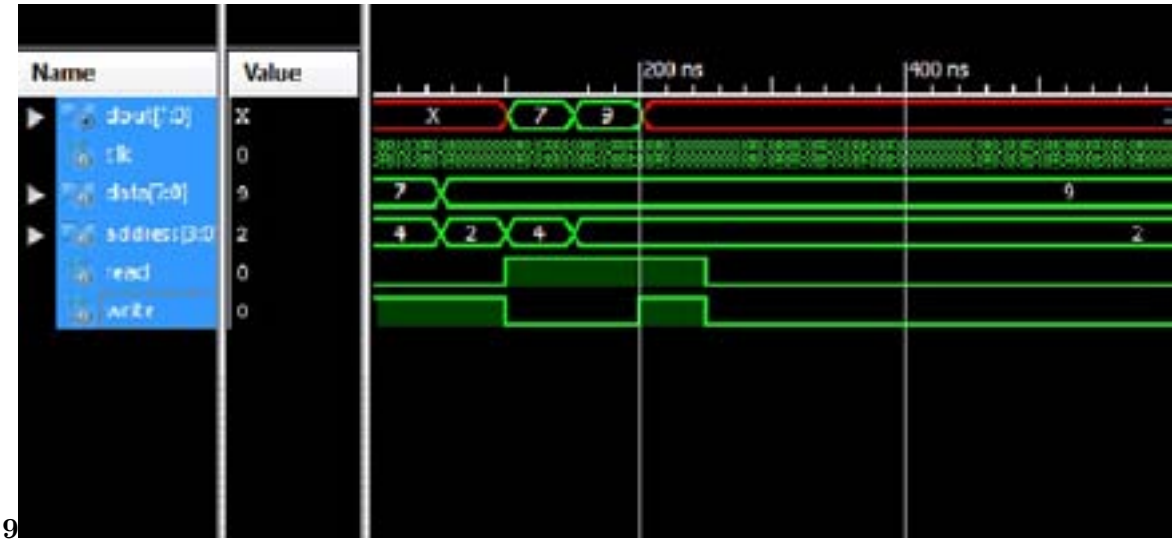
[3]Year 2017 F © 2017 Global Journals Inc. (US) Fig. 11:

[4]Year 2017 F



88

Figure 8: Fig. 8 :Fig. 8 .



9

Figure 9: Fig. 9 :

10312

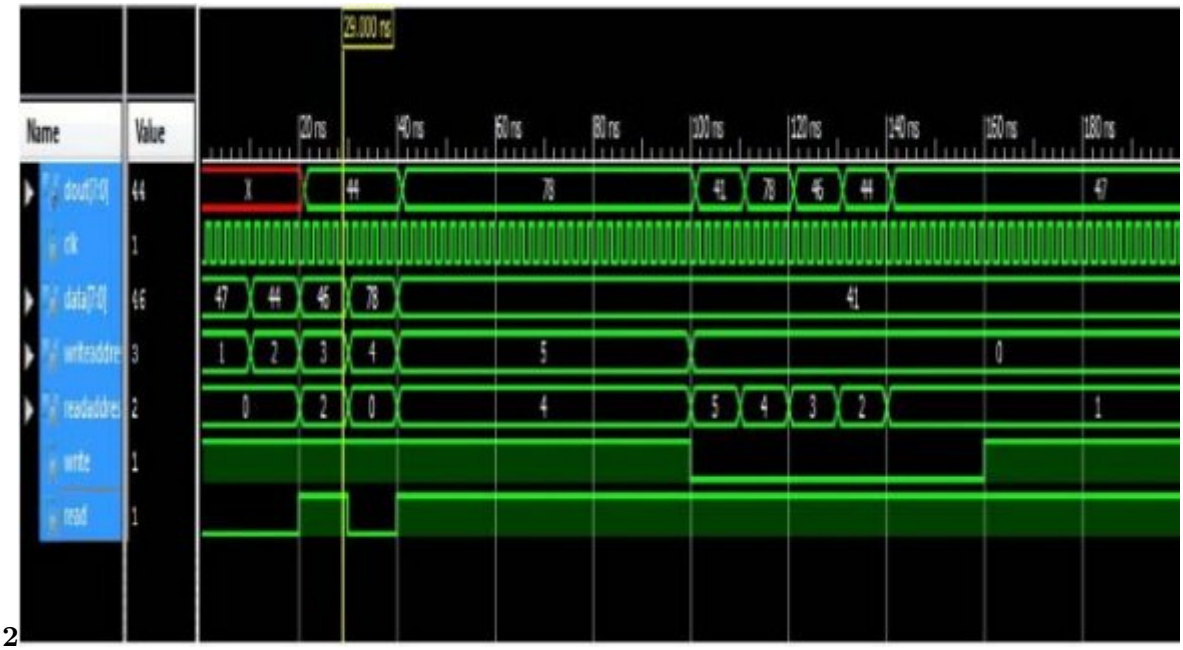


Figure 10: Fig. 10 :F 3 .Fig. 12 :

Year 2017
22
II Version I

		Data	R/W signal
( ) Volume XVII Issue	MBIST Controller	Input Multiported	MUX
Journal of Researches in Engineering	Redundancy circuit	Memory Output Data Out	MUX

Global

[Note: F i. If there is request from Microcode Instruction Storage (MIS) to Pulse generator (PG), then PG sends Start Pulse to MIS to start the asynchronous operation. In next step MIS checks for request from Test Collar (TC), if so it sends microcode instructions to TC. TC then sends the acknowledgement signal to pulse generator indicates that TC is getting instructions from MIs. ii. Output of TC Data which includes test address, corresponding data and R/W control signals send to input multiplexer (MUX) if MUX sends high pulse of request. Multiplexer is originally not a multiplexer but concept used for this block is according to working of normal multiplexer. Here mode signal is select line for MUX. iii. If mode=1then PMBIST works in test mode then it selects TC data. If mode=0 then it is in normal mode, during this mode test circuitry is in ideal condition and memory works as normal memory without under test and sends output of external Address, corresponding data and R/W control signal. When MUX is under test mode then it sends TC data to memory if request signal is high from memory to MUX.]

Figure 11:

.1 Global

[Hassenmestiri et al. ()] 'A high speed AES design resistant to fault injection attacks'. Fatmakahri Hassenmestiri , Mohsen Belgacembouallegue , Machhout . *Microprocessors and Microsystems journal* 2016. Elsevier. p. .

[Bernardi et al. ()] 'A programmable BIST for DRAM testing and diagnosis'. P Bernardi , M Grosso , M S Reorda , Y Zhang . *Test Conference (ITC)*, 2010. 2010. p. .

[Malazgirt et al. (2014)] 'Application specific multi-port memorycustomization in FPGAs'. G A Malazgirt , H E Yantir , A Yurdakul , S Niar . *Proc. IEEE Int.Conf. Field Program. Logic Appl. (FPL)*, (IEEE Int.Conf. Field Program. Logic Appl. (FPL)) Sep. 2014. p. .

[Lai et al. ()] 'Efficient Designs of Multiported Memory on FPGA'. Bo-Cheng Charles Lai , Ieee Member , Jiun-Liang Lin . *ieee transactions on very large scale integration (vlsi) systems*, 2016.

[Laforest and Steffan] *Efficient multiported memories for FPGAs*, C E Laforest , J G Steffan . (inProc. 18th Annu)

[Int ()] Acm/Sigda Int . *Symp. Field Program.Gate Arrays*, 2010. p. .

[Hamdioui ()] 'Memory Test Optimizationfor Parasitic Bit LineCoupling in SRAMs'. *IEEE International Test Conference*, Sandra Irobi Zaid Al-Ars Said Hamdioui (ed.) 2010.

[Dr et al. ()] 'Modeling and Simulation of Multi-Operation Microcode based Built-In Self Test for Memory Fault Detection and Repair'. R K Dr , Sharma Aditi , Sood . *IEEE Annual Symposium on VLSI* 2010.

[Haron et al. ()] 'Modelling and Simulation of Microcode Built-In Self test Architecture for Embedded Memories'. N Z Haron , S A M Junos , A S A Aziz . *Proc. of IEEE International Symposium on Communications and Information Technologies*, (of IEEE International Symposium on Communications and Information Technologies) 2007. p. .

[Laforest et al. ()] 'Multi-ported memories for FPGAs via XOR'. C E Laforest , M G Liu , E Rapati , J G Steffan . *Proc. 20th Annu. ACM/SIGDA Int. Symp. Field Program. Gate Arrays (FPGA)*, (20th Annu. ACM/SIGDA Int. Symp. Field Program. Gate Arrays (FPGA)) 2012. p. .

[Prof et al. ()] 'Optimization of Microcode Built-In Self Test By Enhanced Faults Coverage for Embedded Memory'. Vinod Prof , Mohammed Kapse , Arif . *IEEE Students' Conference on Electrical, Electronics and Computer Science*, 2012.

[Xilinx (2016)] *Series FPGAs Configurable Logic Block User Guide,accessed on*, Xilinx . `http://www.xilinx.com/support/documentation/user_guides/ug474_7Series_CLB.pdf` May 30, 2016.

[Hamdioui et al. ()] 'State-of-art and Future Trends in Testing Embedded Memories'. S Hamdioui , G N Gaydadjiev , A J Van De Goor . *International Workshop on Memory Technology, Design and Testing (MTDT'04)*, 2004.