FPGA Based Hybrid Digital PWM for DC-DC Voltage Regulator

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Abstract

This In general, telecommunication applications require low voltage, high current and reduced size power supplies. Selection of high switching frequency helps in the reduction of the DC-DC converter size. In this work, Digital PI (DPI) enables the Digital Pulse Width Modulation (DPWM) generator for generating high switching frequencies are developed and implemented using VHDL coding and Xilinx Spartan 3A DSP Field Programmable Gate Array (FPGA) kit. Hardware result of voltage regulation depicts the superiority and robustness of the proposed DPI enabled DPWM (MD-DPWM) methods under line and load disturbances. The MD-DPWM technique can be used to generate a very high switching frequency up to 1 MHz and more. Also the MD-DPWM proves to be cost effective, as it consumes low power and area.

Index terms— digital pulse width modulation, digital proportional integral-dc-to-dc buck converter, xilinx spartan 3A DSP field programmable gate array.

1 I. Introduction

uck converter is a circuit which step downs the voltage and step ups the current. A basic buck converter circuits requires inductor, diode and transistor as switch. As per the control of the switch by the PWM signals the inductor acts against the input voltage. The DPWM design involves digital circuits like adders, flip-flops, multiplexers, counters and shift registers.

DPWM has advantages like easy design, high accuracy, low area and low power consumption. High resolution digitally controlled DC-DC buck converter is designed without the use of high frequency clock [1]. FPGA based implementation of the DPWM is very simple comparatively consuming of few memories, multipliers and adders [2]. DPWM architecture developed with FPGA implies high reliability, linearity and low latency [3]. A brushless DC machines can be digitally controlled by FPGA implementation with no additional hardware and hence has low design complexity [4].

A DPWM technique in [5] gives consistent offtime and on-time control under heavy load and light load conditions with reduced switching losses. FPGA based high resolution DPWM designed using a digital clock manager and I/O delay elements have low cost and higher clock frequency [6]. In this work, the performances of the DC-DC buck converter with the DPWM as voltage regulator is analyzed.

2 II. Dc -Dc Buck Converter

The closed loop DC-DC buck converter with the proposed DPI enables the DPWM technique is shown in the Fig. 1.

3 DC-DC Buck Converter

4 Analog to Digital

Converter AD7266 The output voltage of the buck converter is less than the input voltage and is controlled by the duty cycle "d". The duty cycle "d" is the ratio of the ON period to the total period cycle of the controlling square pulse.

5 Modified

6 d = T on T

Where "Ton"refers to the ON period. "T" refers to the total time period of the cycle. The operation of the buck converter is related to the duty cycle as given belowV out = d. V in

Where "d" is the duty cycle. "Vin" is the input voltage of the buck converter. "Vout" is output voltage of the buck converter.

The digital switching control has more advantages like easy designing, high manipulation power, upgradable, immune to environmental changes, easy debugging.

In our work, the FPGA based DPWM DC-DC buck voltage regulator, is implemented which satisfies the demand of low voltage and high current application. ADC is utilized for the purpose of acquiring the feedback values of the DC-DC buck converter into the FPGA. ADC IC AD7266 has Successive Approximation Circuit (SAC) and is used for real time implementation. The FPGA based ADC architecture helps in the evaluation of digital error with high accuracy [7]. The Digital PI (DPI) control algorithm is designed using VHDL coding enables the DPWM. The Modified DPI enabled DPWM (MD-DPWM) generators are implemented by FPGA and found to perform efficiently for the disturbances and component variation. The AD7266 is provided to access the analog value in the form of digital equivalence (2N).

7 III. Digital Pulse Width Modulation Methods

The Digital Pulse Width Modulated (DPWM) signal is generated using logical design. The DPWM is generated by three methods. They are i) Counter DPWM method. (CDPWM) ii) Delay line DPWM method. (DDPWM) iii) Hybrid DPWM method. (HDPWM) Using ModelSim, the three DPWM methods are simulated. From the simulated results, the HDPWM generator is found to be advantages when compared to the CDPWM and DDPWM. The CDPWM require high frequency system clock and thus has high power consumption. The DDPWM occupies more area increasing the cost. The relationship of the clock frequency and the switching frequency for the DPWM generator is Resolution refers to the number of bits used in the design. In this work, the three MD-DPWM generators are designed using 2 11 bit resolution. The MD-CDPWM generator uses a 2 11 bit (2047 count) counter. The MD-DDPWM generator uses the 2048:1 multiplexer. The MD-HDPWM generator uses 2 11 bit resolution in which 2 5 bit is used for the MD-DDPWM generation part and 2 6 bit is used for the MD-CDPWM generation part. The frequency of the DPWM generator is 12.5 KHz in the hardware due to the limitations in frequency range with the laboratory prototype. To achieve this frequency, the VHDL coding utilizes the scaled value given by the formula.F CLK = F SW x 2 n F SW -

8 Scaled_value

= 1 2 n X Output frequency X Clock period

Where Clock period is 100 ns Output frequency is 12.5 KHz

9 V. HARDWARE DETAILS

The Xilinx Spartan 3A DSP FPGA is used for the design of the DC-DC buck type voltage regulator using MD-HDPWM. The Xilinx Spartan 3A DSP has IC AD7266 for the design of ADC. The set point variations are provided by the two variable push switches. The 16*4 LCD display is activated by the VHDL code. The VHDL codes for the DPI and ADC are designed with 10 times of the actual values to accomplish the FPGA requirements. This scaling is done to make sure that the fractional changes of the ADC and DPI are considered in the design, as the Xilinx Spartan 3A DSP kit do not support the float value implementation.

The AD7266 is 8 channels SAR ADC with IC which operates from 2.7V to 5.25V of supply. The ADC performs two functions of sampling and conversion of two channels simultaneously. These conversion values are concurrently accessible in separate data lines. When operated at 3V, the AD7266 gives a throughput rate of 1.5 MSPS with maximum power dissipation of 11.4 mW. Thus low power consumption for high throughput is achieved. The AD7266 has zero pipeline delay; since the sampling control of the two SAR ADCs are accurate. The ADC has two input ranges like 0V to VREF and 2*VREF

10 VI. RESULTS AND DISCUSSIONS

the set-point change and Fig. 13 shows experimental DSO output for the positive and negative line disturbances. Fig. 14&15 indicate the performance of the MD-HDPWM based DC-DC buck converter in closed loop with load disturbances from 445? to 595? and 595? to 445? respectively. The set point is 10 V and input voltage is 20V. The settling time measured during the negative load disturbance with MD-HDPWM seems to be very minimal. Fig. 16&17 show the experimental DSO response of load disturbance from 445 ? to 595? and from 595? to 445? respectively for the MD-HDPWM in closed loop. Fig. 18 shows experimental output response when the load is changed from 470 ? to 495? and from 495? to 470? using MD-DDPWM. Fig. 19 shows experimental output for the negative load disturbance from 445? to 295? using MD-DDPWM. The RTL schematic for the MD-HDPWM technique is presented in Fig. **??**0. Fig. 21,22,&23 show the design utilization chart for the

MD-CDPWM, MD-DDPWM and MD-HDPWM respectively. The experimental setup of DC-DC buck converter using the Xilinx Spartan 3A DSP is shown in Fig. 24.

11 VII. COMPARISON AND ANALYSIS

Table **??** shows that the Modified DPI enabled HDPWM has lower steady state error and low settling time for the step change variation. The peak overshoot percentage is also less in MD-HDPWM. Table **??**

12 b) Experimental Results

The simulation outputs of the MD-DPWM generator using the above mentioned three techniques are given below in Fig. 4,5,&6 using ModelSim. The open loop response under line disturbance for the DC-DC buck converter is given for the three MD-DPWM techniques in Fig. **??**(a),(b)&(c). Fig. **??**(a),(b)&(c) depict the open loop response under load disturbance for the DC-DC buck converter for the three MD-DPWM techniques. Fig. **??** show the start-up transient response along with the set-point variation of closed loop DC-DC buck converter using MD-HDPWM. The CSV file format is plotted using excel sheet format. The time transient parameters like settling time (t s), rise time (t r), delay time (t d), peak time (t p) and overshoot percentage (%MP) are also calculated and displayed in the graph. The input voltage is 20V.The set point variation is from 11V to 12.8 V for MD-HDPWM.

Fig. 10 shows the analysis for the closed loop response under increased line disturbance from 10.4V to 12V and Fig. 11 shows the analysis for the closed loop response under decreased line disturbances from 10.4V to 8.8V for the MD-HDPWM technique. The line voltage in this work are suddenly increased from 18V to 20V and decreased from 20V to 18V. Timing performance indices of the hybrid method are found to have less settling time comparatively and hence hybrid is selected. Fig. 12 shows experimental DSO response for

13 VIII. CONCLUSION

Simulation results show the possibilities of achieving high switching frequency up to 16MHz DPWM. Hardware results show the feasibility of the proposed technique for the available prototype model in our laboratory and found to be satisfactory. The Modified DPI enabled DPWM generators also perform voltage regulation of the power supply. The FPGA based Modified DPI enabled Hybrid based DPWM voltage regulator is found to be immune to circuit component variations, and also to line-load disturbances. [1] [2] [3]

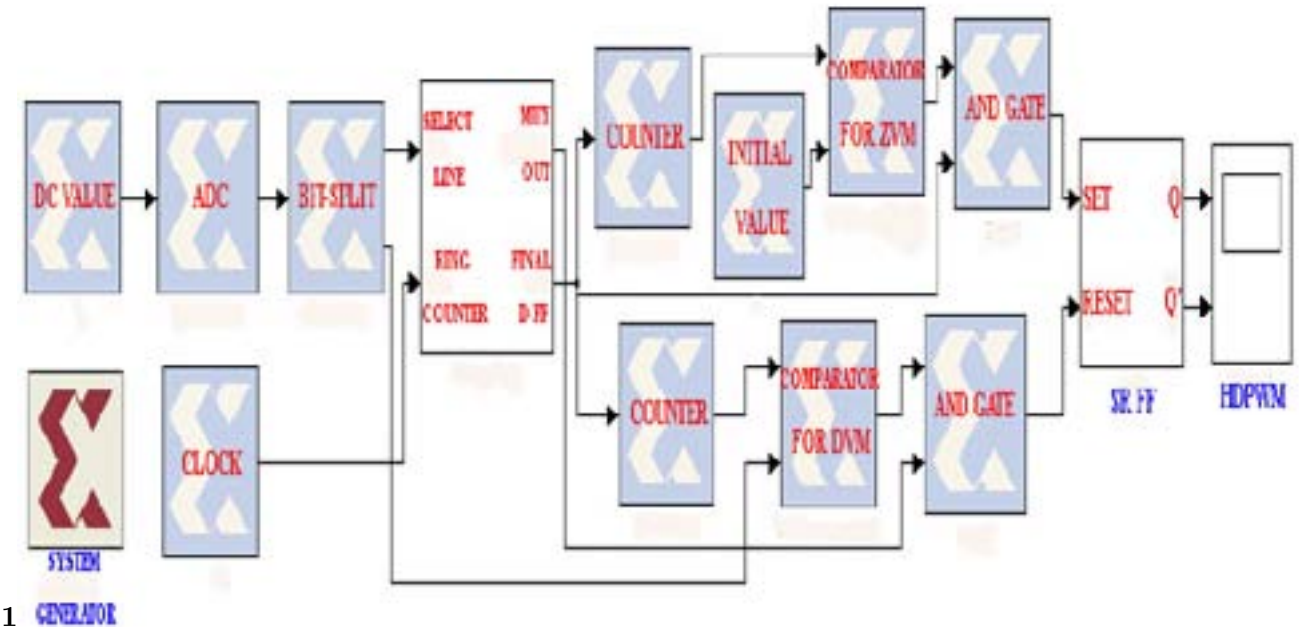

Figure 1: Fig. 1 :

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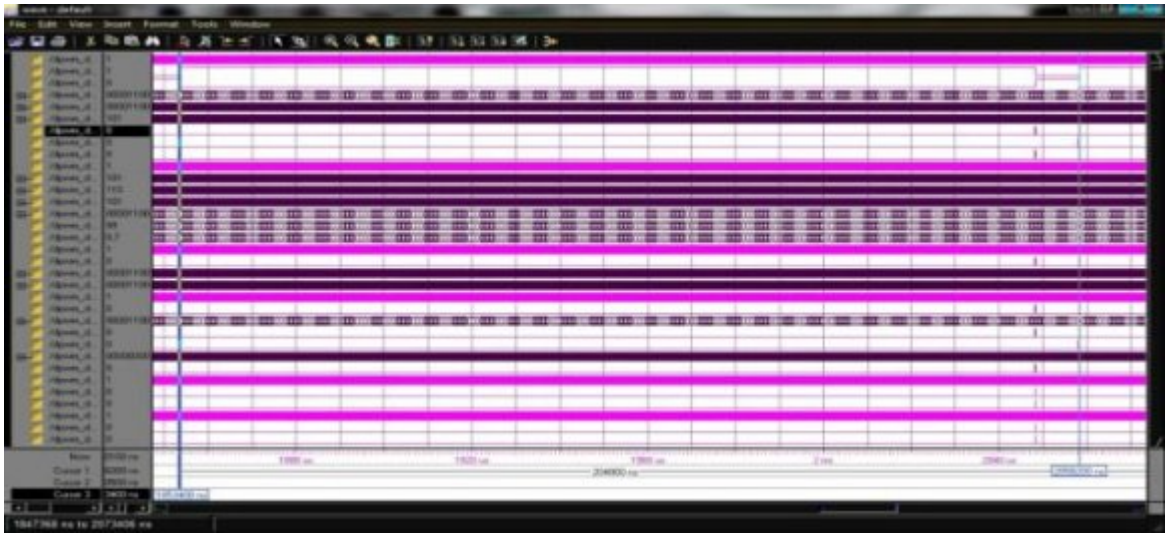

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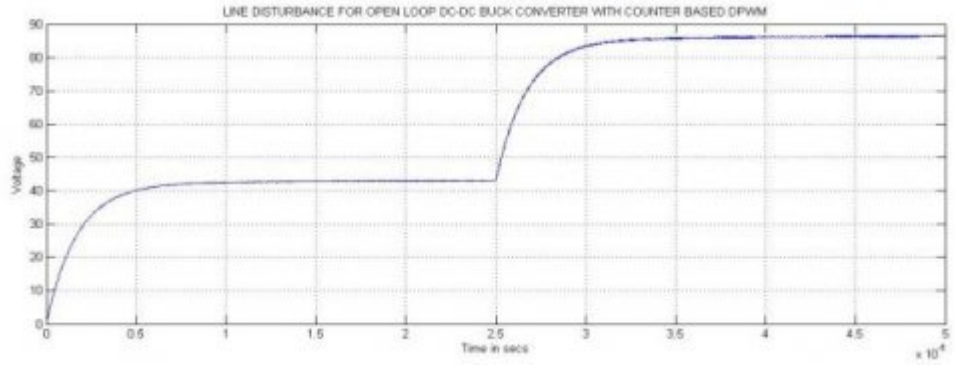

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Figure 3: Fig. 2 :Fig. 3 :

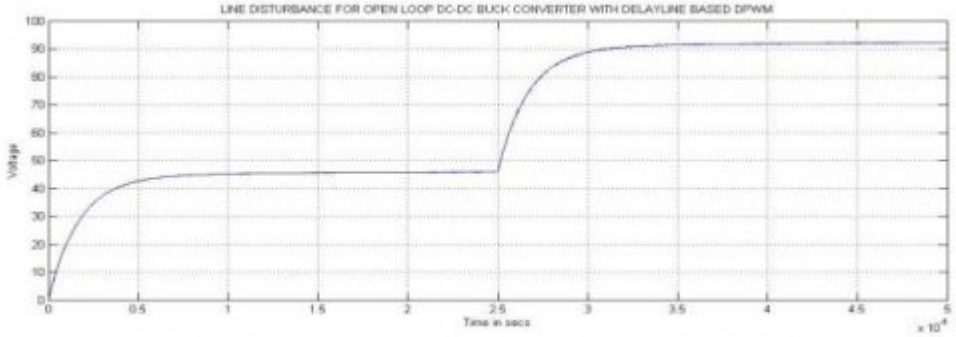

Figure 4:

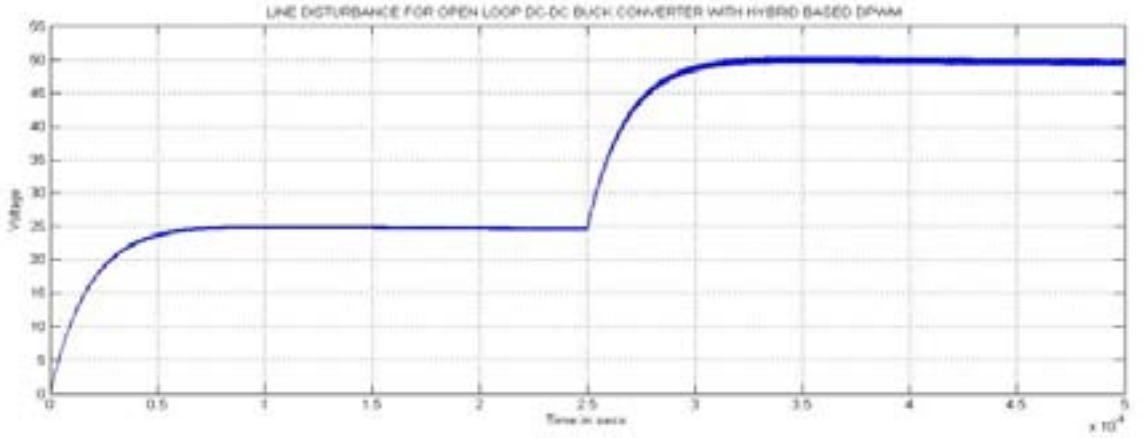

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Figure 5: Fig. 4 :

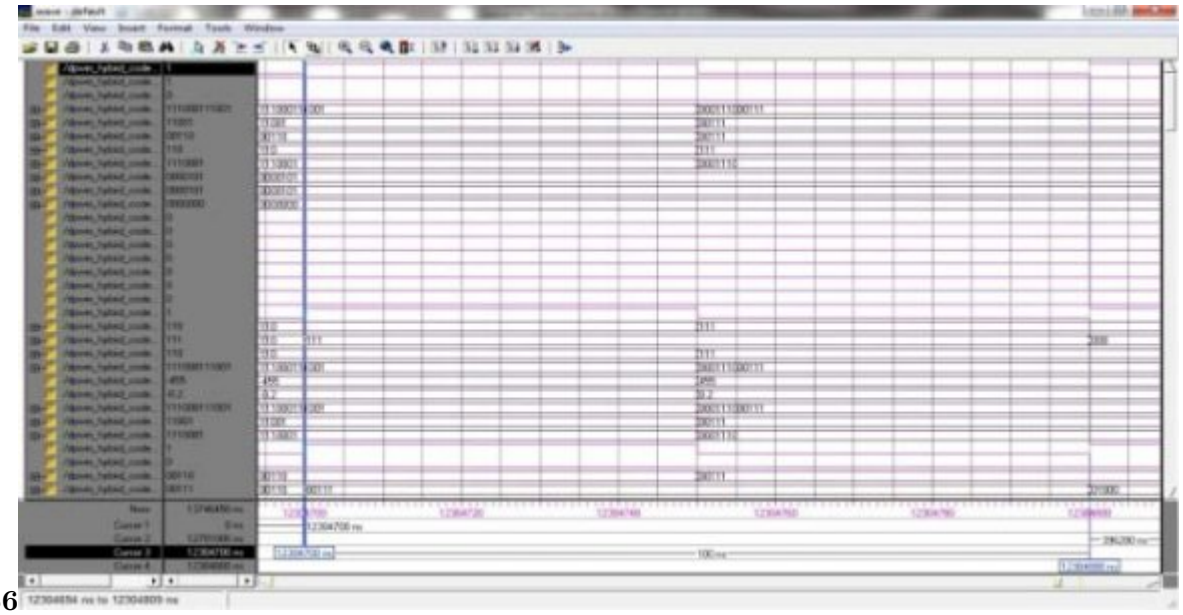

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Figure 6: Fig. 5 :Fig. 6 :

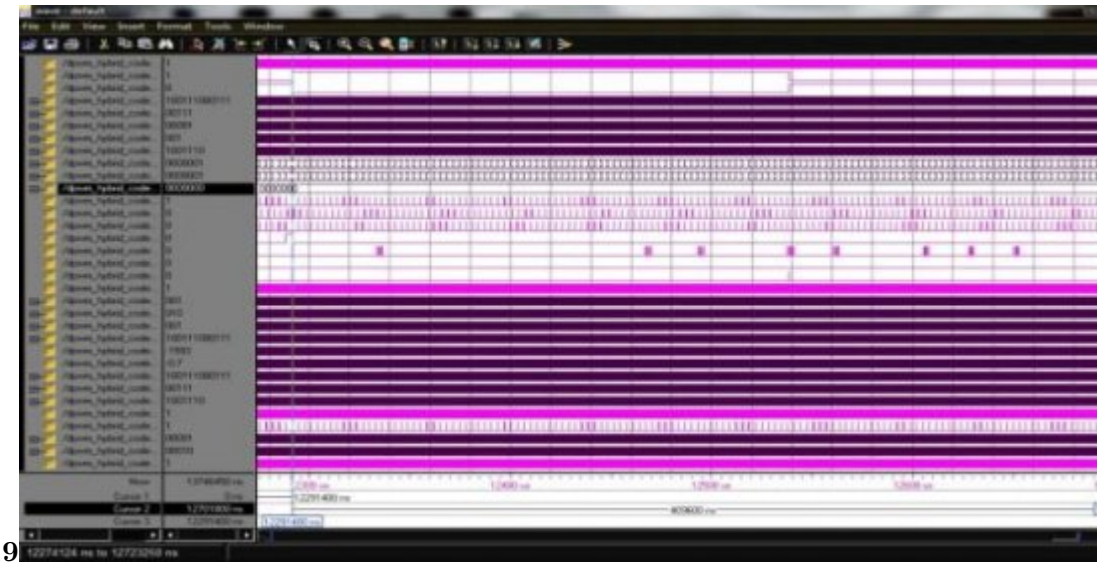

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Figure 7: Fig. 7 :Fig. 8 :Fig. 9 :Fig. 10 : 2017 F©Fig. 11 :Fig. 14 :GlobalFFig. 16 :Fig. 18 :Fig. 19 :

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Method	MD-CDPWM	MD-DDPWM	MD-HDPWM
Settling Time (ts)	4.71	6.2	5.1
Rise Time (tr)	0.035	0.002	0.0419
Delay Time (td)	0.032	0.023	0.0385
Peak Time (tp)	0.04	0.03	0.164

[Note: Table for MD-CDPWM in Xilinx Spartan 3A FPGA Fig. 22: Design Utilization Table for MD-DDPWM in Xilinx Spartan 3A FPGAFig. 23: Design Utilization Table for MD-HDPWM in Xilinx Spartan 3A FPGA Fig. 24: Experimental setup for the Modified DPI enabled DPWM based DC-DC buck converter using FPGA]

Figure 8: Table 1 :

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Increased Line Disturbance Methods	MD-CDPWM	MD-DDPWM	MD-HDPWM
Rise Time in s (tr)	0.2	0.3	0.2
Time Delay in s (tp)	0.1	0.1	0.1
Settling Time in s (ts)	3.8	2.7	1.6
Percentage Overshoot(%MP) 14.286%		17.647%	15.38%
Output Voltage Ripple	0.04	0.04	0.03846
Initial Value before disturbance	9.8 V	10.2 V	10.4 V
Peak Value at disturbance	11.2 V	12 V	12 V

Methods	MD-CDPWM	MD-DDPWM	MD-HDPWM
Rise Time in s (tr)	0.2	0.2	0.23
Time Delay in s (tp)	0.142	0.135	0.13
Settling Time in s (ts)	3.26	2.82	2.62
Percentage Overshoot (% MP)	14.2857%	13.725%	15.38%
Output Voltage Ripple	0.04	0.04	0.04
Initial Value before disturbance	9.8 V	10.2 V	10.4 V
Minimum Value at disturbance	8.4 V	8.8V	8.8 V

Methods	MD-CDPWM	MD-DDPWM	MD-HDPWM
Resolution with specification	2 11 -bit Counter De-signed	2 11 2048 : 1 Mux Designed	(2 6 -bit Counter & 32:1 Mux Designed)
Number of Sliced Flip Flops	665	2716	697
Number of 4 input LUTs	1633	2670	1657
Number of occupied slices	1090	3659	1130
Number of bonded IOBs	37	41	37
Average Fan-out of Non-clock nets	2.96	2.59	2.95

Figure 9: Table 2 :

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Figure 10: Table 3 :

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Figure 11: Table 4 :

[Li et al. (2012)] 'A Digital Dual-State-Variable Predictive Controller for High Switching Frequency Buck Converter With Improved ?-DPWM'. Bo Li , Xuefang Lin-Shi , Bruno Allard , Jean-Marie Rétif . *IEEE Transactions on Industrial Informatics* August 2012. 8 (3) p. .

[Barai et al. (2010)] 'Digital Controller for DVS-Enabled DC-DC Converter'. Mukti Barai , Sabyasachi Sengupta , Jayanta Biswas . *IEEE Transactions on Power Electronics* March 2010. 25 (3) p. .

[Yeh and Lai (2012)] 'Digital Pulse width Modulation Technique for a Synchronous Buck DC/DC Converter to Reduce Switching Frequency'. Chia-An Yeh , Yen-Shin Lai . *IEEE Transactions on Industrial Electronics* January 2012. 59 (1) p. .

[Corradini et al. (2011)] 'Fully Digital Hysteretic Modulator for DC-DC Switching Converters'. Luca Corradini , Aleksandar Bjeleti´c , Regan Zane , Dragan Maksimovi´c . *IEEE Transactions on Power Electronics* October 2011. 26 (10) p. .

[Costinett et al. (2013)] 'Simple Digital Pulse Width Modulator under 100 ps Resolution Using General-Purpose FPGAs'. Daniel Costinett , Miguel Rodriguez , Dragan Maksimovic . *IEEE Transactions on Power Electronics* October 2013. 28 (10) p. .

[Milivojevic et al. (2012)] 'Stability Analysis of FPGA-Based Control of Brushless DC Motors and Generators Using Digital PWM Technique'. Nikola Milivojevic , Mahesh Krishnamurthy , Yusuf Gurkaynak , Anand Sathyan , Young-Joo Lee , Ali Emadi . *IEEE Transactions on Industrial Electronics* January 2012. 59 (1) p. .

[Navarro et al. (2012)] 'Synchronous FPGA-Based High-Resolution Implementations of Digital Pulse-Width Modulators'. Denis Navarro , Luis Angel O´ Scar Luc´?a , Jose´ Ignacio Barraga´n , Isidro Artigas , Urriza , Jime´nez Scar . *IEEE Transactions on Power Electronics* May 2012. 27 (5) p. .