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¹ Thermal Effect in Underfill Encapsulation of Ball Grid Array

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6 Abstract

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Current trend in the industry has seen multi-stacks ball grid array (BGA) being introduced to 7 fulfill the increasing demands of the customer to includes both high performance and smaller 8 size chip package. Conventional underfill encapsulation process on multi-stack BGA to to 9 enhance the reliability of the package is still prone to undesired drawbacks of prolonged 10 encapsulation time and incomplete filling. Accordingly, thermal energy is introduced by 11 preheating the chip prior the underfill process is seen as a viable option to solve the slow 12 filling time issue. A comparative experimental study is conducted on a scaled-up multi-stack 13 BGA model for the cases at two distinct setups; at room temperature of 25°C and pre-heated 14 at 70°C respectively. Decisive data has concluded that the setup with elevated temperature 15 has prominently increase the filling rate by 75.2 16

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18 Index terms—

¹⁹ 1 I. Introduction

all Grid Array (BGA) is a type of surface-mount packaging for integrated circuits (IC) in which the chip device at the printed circuit board (PCB utilizes the connection of square grid array of solder balls. Generally, BGA is much more advantageous compared to Pin Grid Array (PGA) and Chip-scale Package (CSP), in terms of reliability, durability and manufacturability [1].In contrast, Multi-stack BGA device is a renovated design of conventional BGA flip chip, aimed to multiply the performance of device by slightly sacrificing its height while still retaining its small compact structure. Various researches on the structural and underfilling flow aspects in the multi-stack chip device have been extensively conducted **??2** -5].

The underfill encapsulation process is of utmost important to enhance the package reliability as well as serve as 27 protection to the flip chip device. Moreover, it may also act as heat sink to dissipate thermal stress away from the 28 solder joints [6]. The manufacturing process involving underfill process must be properly considered and designed 29 to achieve highest state of reliability. In achieving this target, the underfilling process of multi-stack BGA or 30 generally the BGA flip chip devices usually suffer problems relating to extended filling time and incomplete 31 filling. These defects are generally undesirable which critically impart the quality of the encapsulation process. 32 Subsequently, this will lengthen the lead time and incur additional manufacturing costs. The optimization studies 33 of underfilling flow through BGA device have been comprehensively studies by Aizat et al., from various aspects 34 namely encapsulant dispensing methods, bump orientation and sizes ??7 -9]. They concluded that the U-type 35 36 dispensing method and perimeter bump arrangement yields the shortest filling time.

It is usually a practice in industry to pre-heat the chip device at about 60°C ? 80°C prior to the underfilling process. The aim however is to ensure the encapsulant does not solidify before the curing process [6]. Several experimental and numerical simulation researches have been carried out to investigate the thermal properties of the stacked chip device, from the perspective of heat power dissipation [10], effective thermal coefficient [11] and heat distribution in the package [12]. These studies have emphasized the particular importance of temperature in optimizing the underfill encapsulation process.

Previous literatures showed that the underfill process can to be optimized through proper introduction of heat to the different layers of the package. Therefore, a simple comparative study is required to justify the influence of temperature on the underfill flow for multi-stack BGA device based on scaleup experimental model. This scaled-up BGA model has been utilized by various researchers ??3 -5, 7 -9] and proven viable in improving the visualization of the encapsulant flow through the solder bumps that is similar to the actual industrial setup. To date, no comparative study has been carried out to identify the contribution of thermal energy to accelerate the encapsulant flow in multi-stack BGA device using experimental approach. Essentially, this paper is aimed to provide useful information for the manufacturer in an attempt to optimize the underfill process using thermal approach.

⁵² 2 II. Methodology

A scale up model of multi-stack BGA was constructed using clear Perspex and plastics beads. Several 53 considerations were made during the design process of the experimental setup and after countless of iterations 54 and improvements, the final design of the experimental setup will rely on four walls that is confined around the 55 multi-stacked BGA. This setup will mimic industrial barrier used in encapsulation process to prevent spillage of 56 the fluid outside the integrated chip (IC) package. The advantages of such barrier set up is to ensure simultaneous 57 flow of fluid into all layers of the multi-stacked BGA model, as well as to minimize the waste of underfilling fluid 58 due to spillage and overflow [13]. The barrier and three BGA plate models were constructed using clear Perspex 59 and plastic beads that is jointed together using super glue. Excess glue strains on the Perspex were removed for 60 better appearance and smoother surface to eliminate future possible sources of error. Figure 1 Each BGA model 61 plate is then immersed in hot water bath at 70°C for around 20 seconds to reach thermal equilibrium. After being 62 soaked in hot water, a dry cloth is used to remove some of the excess water from the BGA plate. The heated 63 plates were then carefully put into the barrier that is stacked on top of each other. Two videos cameras were 64 used to record the flow of fluid across the multi-stack BGA in both top and side views simultaneously. Later, 65 non-Newtonian fluid with similar fluid properties was used to mimic the industrial encapsulant. The encapsulant 66 were carefully poured into the inlet of barrier to enable it flows into the multi-stack BGA. The replacement 67 fluid is poured thoroughly at constant rate so that it is able to flow in at each layers without any spillage or 68 bubble formation inside the encapsulant. Afterwards, the videos obtained were analyzed and the filling times 69 for the encapsulant to attain filling of 20%, 40%, 60%, 80% and finally the completion 100% at each layers were 70 tabulated and presented in suitable graphical forms. 71

⁷² 3 III. Results and Discussions

73 There are total of two distinct sets of experiments with varying parameter scarried out to justify the impact of 74 thermal on the underfill encapsulant flow through the BGA. The main difference between these set sis depicted 75 as follow: Set A: Reference set with all three layers at room temperature of 25°C Set B: Pre-heated set with all 76 three layers at 70°C

The video recordings of the underfill flow through the BGA are analyzed and subsequently the results of the filling time at certain filling percentage for both experimental sets A and B were tabulated in Table 1(i) and Table 1(ii) respectively. Subsequently, a corresponding filling time plot is constructed and presented in Figure 2. Similar procedures were being used to study the encapsulant flowin the BGA at normal conditions without introducing heat energy. This experiment is repeated with a pre-arranged three layers of BGA layers at room

temperature without adding heat on it.

(ii) Set B at elevated temperature of 70°C By comparing the filling times for both experimental sets in Table 1(i) and Table 1(ii), it appeared that the flow tends to be faster a tall three layers of Set B. Thus, the filling time
gap between top and middle layers were reduced and all three layers appeared to have almost similar flowing
rate. So it is deduced that the increase in underfilling temperature willincreases the flow rates of the underfilling
mold.

The underfillflow rate appeared to be inconsistent throughout the whole underfilling process. From Figure 2, the encapsulant generally flows faster at the beginning and the flow rate reduces near completion. This is essentially due to the cumulative solder bump resistance that gradually built up as the encapsulant advances. Nonetheless, it can be approximated that the average flow rate of the underfilling process can be approximated through gradient calculation for the whole segment of the graph. The average flow rate, ?? ? is in fact inversely

through gradient calculation for the whole segment of the graph. The average flow rate, ?? ? is in fact inversely proportional to the gradient of the graph and can simply be approximate dusing the formula:?? ? = 0.8 ?? ,

⁹⁴ with?? being the time taken for the encapsulant flow from 20% filling until 100% filling.

95 4 IV. Conclusion

96 Based on the comparative experimental study conducted, it was shown that the introduction of thermal energy 97 had increased the overall encapsulant flow rate across all layers of the multi-stack BGA with an averagely of 75.2% 98 upon comparison with the standard setup at normal condition. Therefore, it is justified that the temperature has played a significant role in accelerating the underfill encapsulation process. The BGA flip chip is required 99 to be heated to a sufficient high temperature prior the commencement of underfilling process. This will ensure 100 substantial filling rate and prevent the solidification of the underfill mold. Additionally, this research has also 101 provided some insights regarding the trend of underfill flow across multi-stack BGA regardless of its thermal 102 source. The encapsulant tends to flow faster at the bottom layer followed by middle layer and lastly the top 103

layer. It was also shown that the underfill flow also gradually decelerates as it progresses through the array of solder bumps towards the outlet vent. 1^{2} 104 solder bumps towards the outlet vent.



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Figure 1: BFeiChong

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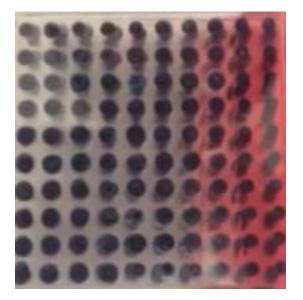


Figure 2:

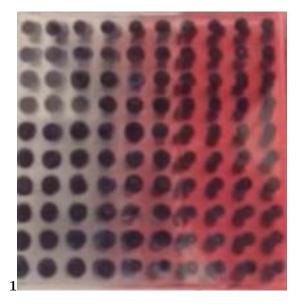


Figure 3: Figure 1 :

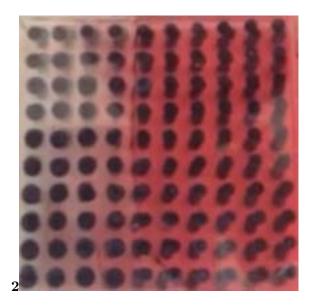


Figure 4: Figure 2 :

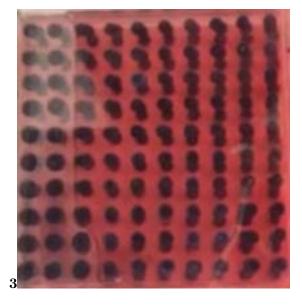


Figure 5: Figure 3



Figure 6: Figure 3 :

4 IV. CONCLUSION

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		(i) Set A at room temperature of 25° C			
Layers	20%	Filling time at different filling percentages (s) 40% 6	0%	80%	100%
Top	14	42	78	120	170
Middle	12	26	53	94	125
Bottom	8	17	35	63	98

Figure 7: Table 1 :

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Layer	Average Flow Rate, ?? ? (s -1) S	Set A (At 25° C) Set B (At 70° C)
Top	5.128×10 ?3	$9.091 \times 10 \ ?3$
Middle	7.080×10 ?3	12.50×10 ?3
Bottom	8.889×10 ?3	15.38×10 ?3
Average	7.032×10 ?3	12.32×10 ?3

Figure 8: Table 2 :

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- [Ernest et al. ()] 'Analysis of encapsulation process in 3D stacked chips with different micro bump array'. E S
 Ernest , M Z Ong , C Y Abdullah , Khor . International Communications in Heat and Mass Transfer, 2012.
- 111 39 p. .
- [Ardebili and Pecht ()] Chapter 3 Encapsulation Process Technology, Encapsulation Technologies for Electronic
 Applications, H Ardebili , M G Pecht . 2009. Elsevier. p. .
- 114 [Abas et al. ()] 'Effect of ILU dispensing types for different solder bump arrangements on CUF encapsulation
- process'. Aizat Abas , M S Haslinda , M H H Ishak , A S Nurfatin , M Z Abdullah , F Che Ani . *Microelectronic Engineering* 2016.
- [Fei et al. ()] 'Effect of thermo capillary action in the underfill encapsulation of multi-stack ball grid array'. Chong
 Fei , Aizat Ng , Mhh Abas , Ishak , Abdul Abdullah , Aziz . *Microelectronics Reliability*, 2016.
- [Ramdan and Abdullah ()] Effects of outlet vent arrangement on air traps in stacked-chip scale package
 encapsulation, D Ramdan , M Z Abdullah . 2012. 39 p. . (International Communications in Heat and Mass
 Transfer)
- [Ernest et al. ()] 'Fluidstructure interaction analysis on the effect of chip stacking in a 3D integrated circuit
 package with through-silicon vias during plastic encapsulation'. E S Ernest , M Z Ong , C Y Abdullah , Khor
 Microelectronic Engineering 2014. 113 p. .
- [Melamed and Fumitoimura ()] 'Impact of die thinning on the thermal performance of a central TSV bus in a
 3D stacked circuit'. Samson Melamed , Fumitoimura . *Microelectronics Journal* 2015.
- 127 [Abas et al. ()] 'Lattice Boltzmann and finite volume simulations of multiphase flow in BGA encapsulation 128 process'. Aizat Abas, Mhh Abdullah, Ishak. ARPN Journal of Engineering and Applied Sciences 2015.
- [Abas et al. ()] 'Lattice Boltzmann Method of Different BGA Orientations on I-Type Dispensing Method'. Aizat
 Abas , Mhh Gan , Ishak . *PLoS ONE* 2016. 11 (7) p. e0159357.
- 131 [Liu et al. ()] 'Plastic ball grid array (PBGA) overview'. J J Liu , H Berg , Y Wen , S Mulgaonker , R Bowlby ,
 132 A Mawer . Mater. Chem. Phys 1995. 40 p. .
- [Liu and Xu ()] 'Stacked solder bumping technology for improved solder joint reliability'. Xingsheng Liu ,
 Shuangyan Xu . *Microelectronics Reliability*, 2001. 41 p. .
- [Naito and Fujishiro ()] 'Thermal conductivity of single and multi-stacked DI-BSCCO tapes'. Tomoyuki Naito ,
 Hiroyuki Fujishiro . Cryogenics 2009. 49 p. .
- [Chen and Chen ()] 'Thermal resistance of side by side multi-chip package: Thermal mode analysis'. Dao-Long
 Chen , Tei-Chen Chen . *Microelectronics Reliability*, 2015. 55 p. .