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A Current Balanced Logic Buffer based Time-To-Digital Converter with Improved Resolution

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Pooja Saxena [α], K. Hari Prasad [σ] & V. B. Chandratre [ρ]

Abstract- This paper presents design and implementation of TDC based on time stamping using current balanced logic (CBL) buffer in 0.35 μm CMOS technology. The CBL logic buffer provides smaller delay compared to widely used current starved inverter, allowing better resolution in a given technology node. The CBL buffer based tapped delay line (TDL) provides accurate reference timing signals for time stamping through latching their status by event signal. The time stamping is designed with dynamic range of 40 μs and allows tunable resolution with minimum value of 136 ps by varying CBL delay using off-chip reference voltage. Across process voltage & temperature (PVT) variations, by stabilizing the CBL delay with the help of delay lock loop (DLL), the attained resolution is 174 ps. This TDC is designed to work in two modes- Time Interval (TI) measurement mode and common stop multi-hit mode to enhance scope of its utilization.

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I. Introduction

Time-to-digital converter (TDC) is an important functional unit for accurate time interval (TI) measurement between 'start' and 'stop' events in HEP experiments. In India based Neutrino Observatory (INO) HEP experiment, TI measurement between 'start' & 'stop' with resolution better than 200 ps is required. Also, multiple start transitions along with width of 'start' signal need to be measured over dynamic range (DR) of 32 μs. The measurement of multiple start transitions is used to find delayed events. The width of 'start' signal is used for 'time over threshold' [1] implementation required in time walk error correction.

To cater to above stated requirements in 0.35 μm CMOS technology, this paper presents a design & implementation of TDC based on time stamping [2]. This TDC stamps arrival time of events with respect to reference clock (100 MHz) using tapped delay line (TDL) combined with a counter. The number of bits in counter is chosen as 12 to achieve time stamping range of (212-1) ×10 ns = 40.95 μs, which is higher than the required value of 32 μs. The resolution of TDC depends on the least delay provided by the delay element, used to realize TDL. In the chosen technology, the least achievable delay in current starved inverter based delay element is ~ 400 ps, which does not fulfill the required resolution of TI measurement. To achieve resolution better than that attainable in a given technology in the earlier reported TDCs [3] [4], a delay interpolation technique has been used. This technique requires multiple DLLs to interpolate the delay of current starved inverter, leading to large power & area consumption. In second approach used in [5], a high speed differential delay element has been used, which requires high static current (~1 mA) to provide small delays. In this design, with constrained requirement of low power due to millions of detector channels, a high speed voltage controlled buffer based on Current Balanced Logic (CBL) [6][7] is designed. It has advantages of small area (4 transistors), identical edge transition delays, wide delay regulation range (~1.6 ns) and propagation delay (136 ps), which is smaller than that (~ 400 ps) in current starved inverter. Also, the CBL delay element has less design complexity as both transition delays are controlled by single bias voltage whereas in current starved inverter two bias voltages are needed to control the rising and falling edge delays.

This paper is organized in three sections. Section-II discusses the design and implementation of time stamping based TDC ASIC. The simulation results in support of performance validation of this design are discussed in section-III. Finally, conclusions are drawn in section-IV.

II. TDC ASIC Architecture

The TDC ASIC is designed to work in two measurement modes: 8-channel TI and 4-channel multi-hit, by stamping the arrival time of events with respect to a reference clock (100 MHz). It consists of following blocks: control logic block, Pre-processor, CBL based TDL along with DLL, transition detector, 12-bit coarse counter, 17 fine & 17 coarse registers, memory & its interface logic and readout interface, as shown in Fig. 1(a).

The logic control block enables a 'clock' for TDL and counter on an external 'event reset' signal to initialize the time stamping. Subsequently, it opens a 'dynamic range (DR) window' of duration 40 μs to enable the pre-processor block. It processes the inputs 'start', 'stop' and 'trigger' events for stamping their arrival times within DR window in both the modes of TDC.

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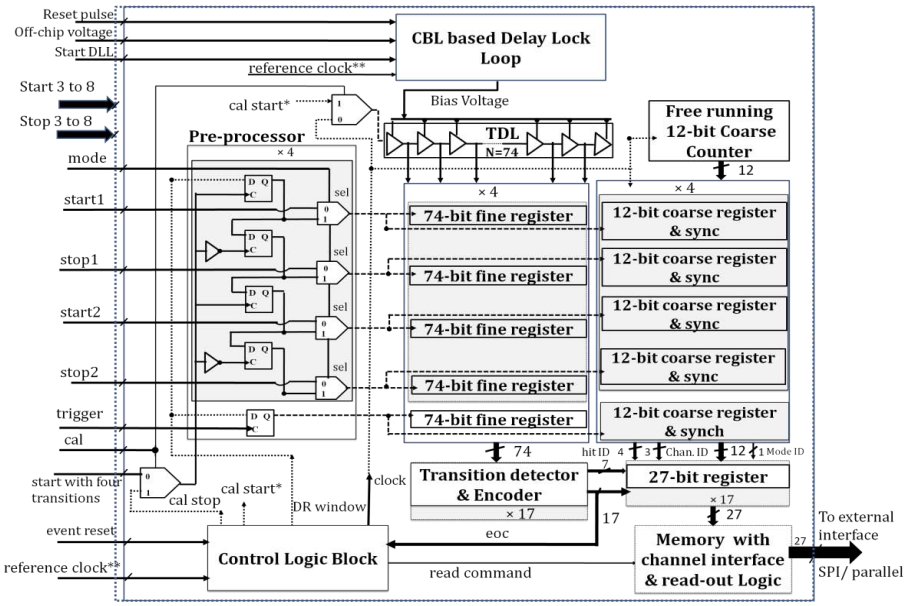
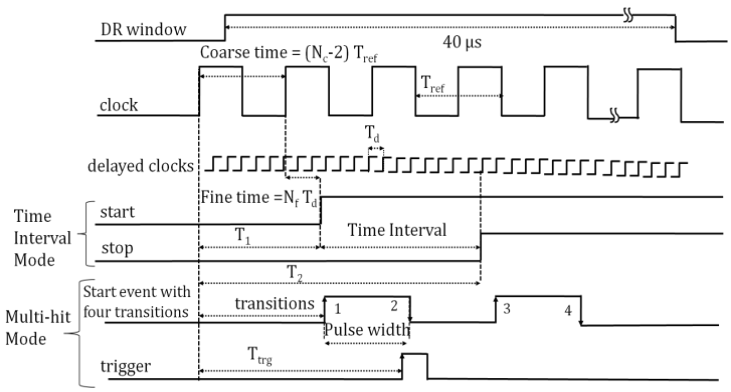
In TI mode, each pre-processor block is dedicated for two channels of TDC. In each channel, arrival times (T1 and T2) of 'start' and 'stop' is stamped independently with respect to clock as shown in Fig. 1(b). The difference of their time stamped values is used to measure TI between them.

In multi-hit mode, each preprocessor block is dedicated to the single channel of TDC to separate out the four transitions (1, 2, 3, & 4) in the 'start' signal. The arrival time of each transition is stamped independently with respect to clock. The difference in time stamped values corresponding to first two transitions is used to measure pulse width of 'start' signal. The stamped times of third and fourth transitions are used to find delayed events. The time of trigger is also stamped with respect to clock to find its associated events within DR window. The design aspects of time stamping are given in sub-section A.

The time stamped data from each channel of TDC is transferred to inbuilt memory. The data transfer is controlled by the logic control block. It issues a read command to the memory; to read the channels only if stop and trigger is present in the window in TI and multi-hit modes respectively. In their absence, the channel data is discarded. The TDC channel data from memory is transferred to external interface by using either Serial Peripheral Interface (SPI) or parallel interface based read-out logic. The resolution of TDC is defined by the CBL delay, which is stabilized across PVT variations by the control voltage provided by DLL. The DLL and time stamping blocks are designed in close proximity of each other to minimize the process induced CBL delay mismatch in both the blocks. Along with DLL, an optional provision for CBL delay tuning by using off-chip reference voltage is designed. To find the tuned CBL delay value, a calibration scheme is designed. The design and implementation of CBL delay stabilization, tuning, & calibration is discussed in sub-section B.



(a)



(b)

Fig. 1 : TDC Architecture (a) Block Diagram (b) Timing Diagram

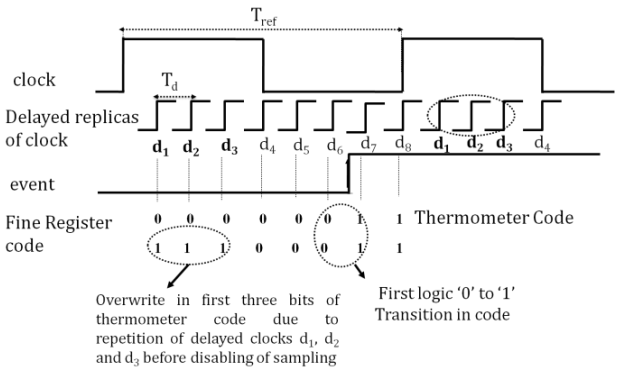
a) Design aspects of Time stamping

The occurrence time of event (start/stop/trigger) is stamped in two parts- coarse and fine (Fig. 1(b)). The coarse time, corresponding to the elapsed full cycles of clock till the occurrence of event, is measured by using 12-bit counter. The fine (fractional) time within one clock period (T_{ref} =10 ns) covered by an event is measured by using TDL.

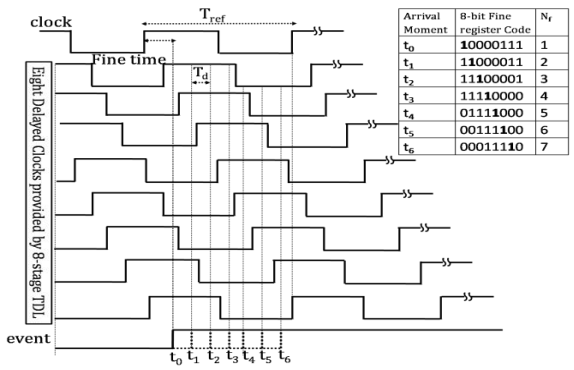
The TDL is realized by a chain of cascaded 'N' number of CBL buffers each with delay 'T_d', which defines the resolution of time stamping. For stabilized CBL delay of 174 ps, 58 number of CBL buffers are required for TDL to cover a range of one clock period T_{ref} = 10 ns, by using equation (1). However, in this design to allow the least tunable CBL delay of 136 ps at V_{dd} = 3.6 V as resolution for time stamping, 74 CBL delay elements are used in TDL. It provides 74 uniform delayed replicas of applied 'clock' signal with TI of T_d. These delayed clocks are shared among 17-fine registers, 16 for measurement channels (4 channels in multi-hit or 8-channels in TI) and one for trigger channel to measure fine time of events.

$$T_{ref} = N \times T_d \quad (1)$$

The fine time of each event is measured by finding the elapsed number of delayed clocks till its occurrence. To determine this number, two architectures of fine time measurement are analyzed. In the first, the delayed clocks sample and latch the status of event signal in fine register as shown in Fig. 2(a). The first logic '0' to '1' transition count in the thermometer code of fine register gives fine count (N_f). For correct fine count, it is desired to disable the sampling of 'event' status before next clock cycle. However, due to uncontrolled processing delays, the first few bits of fine register in the thermometer code are overwritten before sampling gets disabled.



(a)

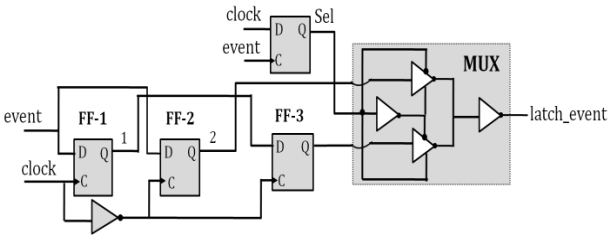


Arrival Moment	8-bit Fine register Code	N_f
t_0	10000111	1
t_1	11000011	2
t_2	11100001	3
t_3	11110000	4
t_4	01111000	5
t_5	00111100	6
t_6	00011110	7

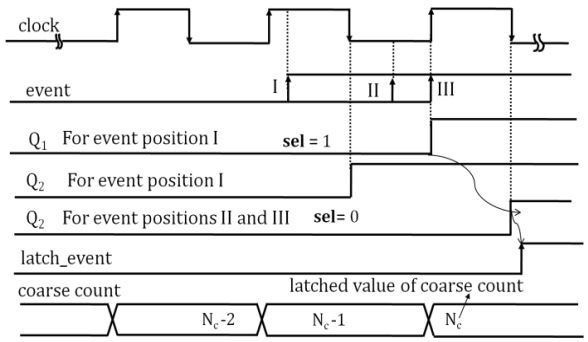
(b)

Fig. 2 : Timing Diagram of fine time measurement for N= 8 delay elements (a) first architecture (b) second architecture

This issue of code overwrite is avoided in second architecture of fine time measurement. Here, the 'event signal samples and latches the status of 74-delayed clocks in fine register as shown in Fig. 2(b). The first logic '1' to '0' transition count in the fine register non-thermometer code gives the fine count (N_f). This transition count is detected by using a transition detector based on magnitude comparison between two consecutive bits of fine register. Further, the encoder converts the 74-bit fine count to 7-bit binary value to reduce the number of bits of fine count. This 7-bit fine count (N_f) multiplied with CBL delay 'T_d' (≥ 136 p s) evaluates the fine time of event with respect to the rising edge of clock cycle in which it lies. The elapsed full clock cycles before arrival of event is measured by coarse time.



(a)



(b)

Fig. 3 : Dual Edge Synchronizer (a) Timing Diagram of (b) Schematic Diagram

In coarse time measurement of event, it samples and latches the status of free running counter. While sampling if event occurs during switching of counter, the latched count will be incorrect due to setup time violation or dead zone in the coarse register. Also, the coarse and fine counts need to be synchronized to avoid an error of one coarse count. To address these issues, a dual edge synchronizer based on the dual synchronization scheme [8] is designed as shown in Fig. 3(a). This synchronizer samples & latches the status of counter when it is in idle state, thereby avoids timing violations in coarse register. The latched count of elapsed clock periods has one extra count, which is irrespective of event position (I, II & III) within a clock period as shown in Fig. 3(b). This is carried out by synchronizing the 'event' signal to both the rising and falling edges of clock, resulting in the generation of latched signals Q_1 and Q_2 respectively. A MUX selects the signals 'Q_1' or 'Q_2' as per the 'event' position to obtain the 'latch_event' at falling edge of clock in next cycle. It samples and latches the count status 'N_c'.

The measured coarse count (N_c) and fine count (N_f) are used in calculation of arrival time (T) of event with respect to clock by using equation (2). The considered value of coarse count is 'N_c-2' as two counts are subtracted- one due to synchronization scheme and other due to addition of fine time with coarse time (Fig. 1(b)).

$$T=(N_c-2)\times T_{ref}+N_f\times T_d \quad (2)$$

b) CBL delay stabilization & Tuning

The CBL delay in time stamping block is stabilized across PVT variations by the control voltage obtained from DLL as shown in Fig. 4. The DLL is enabled by applying a rising edge of 'start DLL' signal in the 'start control circuit'. It provides a clock (clock_TDL) for reference TDL, whose initial delay is set to minimum value (4.09 ns) by pre-setting the capacitor voltage through 'preset switch' to avoid false locking in DLL. The feedback loop consisting of phase detector, charge pump and filter capacitor, locks the TDL delay to the half clock period (5 ns) of reference clock (complementary clock_TDL) across PVT variations in acquisition time of 124 cycles of clock. The attained stable voltage across filter capacitor is used to stabilize the CBL delay to 174 ps across PVT variations.

The half clock period locking in DLL is designed to reduce its acquisition time. To further reduce the acquisition time, the initial delay of reference TDL can be fixed nearer to the target value by 'preset switch'. Thus, the present architecture achieves better performance as compared to earlier reported architecture [9][10], where the TDL delay with load of fine register channels is locked to reference clock period in long acquisition time. Along with CBL delay stabilization, an option for its delay tuning using off-chip reference voltage is designed. It is selected by resetting the D flip-flops used in start control circuit. It turns on the 'preset switch' as well as disables DLL, so that the filter capacitor is charged to the off-chip reference voltage.

The voltage across filter capacitor is applied to TDL (time stamping block) for delay stabilization or tuning through bias circuit [8]. The purpose of bias circuit utilization is to avoid the loading of long delay lines on filter capacitor (C) by charge sharing with the parasitic capacitances of TDL.

The tuned value of CBL delay is determined by measuring on-chip generated time intervals of 10 ns and 5 ns in between 'calstart' and 'calstop' signals (Fig. 1(a)). These time intervals are generated by using reference clock. The calibration mode is selected by 1-bit 'cal' signal. The CBL delay 'T_d' is given by the difference of measured time intervals by using equation (3), where N_{f1} and N_{f2} are the counts of fine registers corresponding to 10 ns and 5 ns time intervals respectively. The calibrated CBL delay is used to calculate the final stamped time of event using equation (2).

$$T_d = \frac{(10-5)ns}{(N_{f1}-N_{f2})} \quad (3)$$

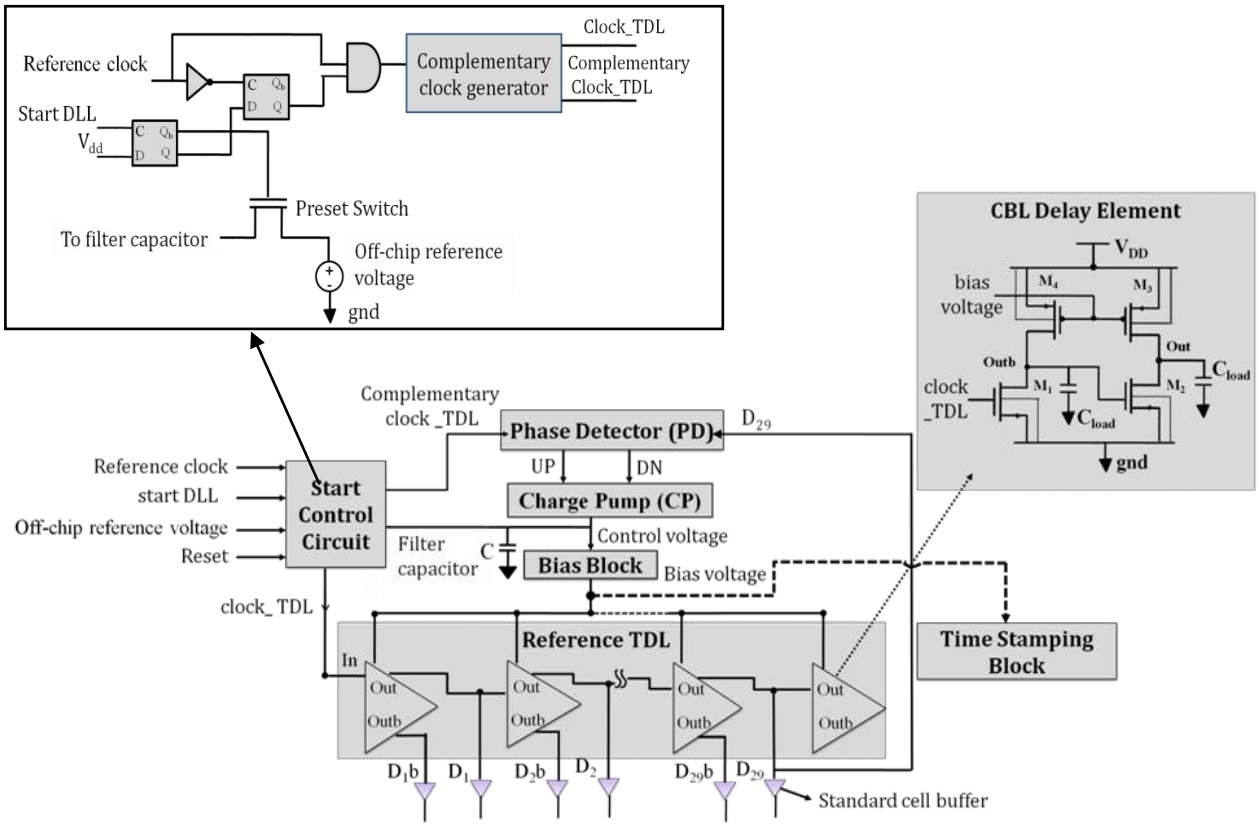
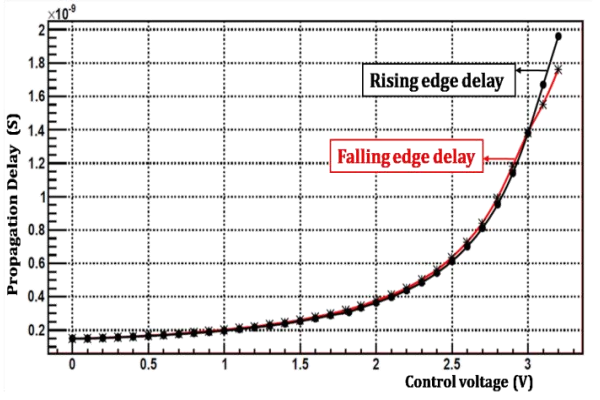


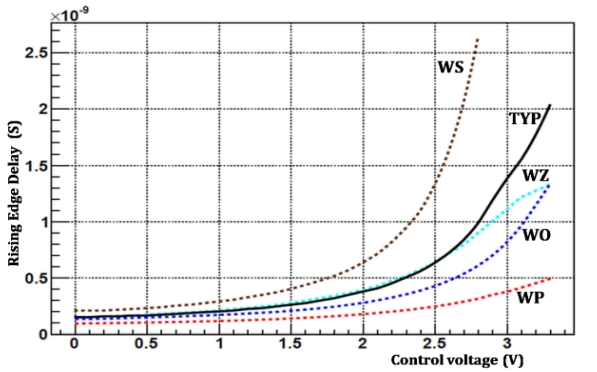
Fig. 4 : Block Diagram of CBL delay element based DLL with start control circuit

III. Simulation Result

The post layout performance of CBL delay element is verified by using Spectre simulator across design process corners. The CBL delay characteristic for both rising and falling edge transitions is shown in Fig. 5(a) on typical corner. Fig. 5(b) depicts the CBL rising edge delay across process corners, where on the worst case slow corner (WS), the smallest attainable delay is 200 ps. The performance of post layout CBL based DLL is also verified using specter simulator across design process corners for CBL delay of 174 ps at clock frequency of 100 MHz. Fig. 6 shows the profile of control voltage versus acquisition time.



(a)



(b)

Fig. 5 : Delay versus Control Voltage Characteristic of CBL DE at 3.3 V supply voltage (a) Typical corner (b) Design Process Corners

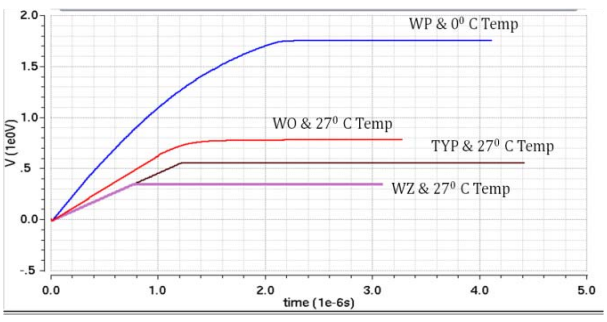


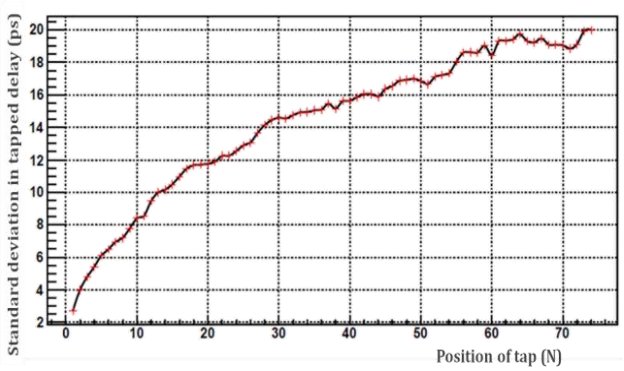
Fig. 6 : Control voltage vs. acquisition time

The variation in tapped delays for 74-stage TDL due to local process variations is evaluated by using Monte Carlo simulator for 100 runs. The standard deviation of delay variation on each tap of TDL is shown in Fig 7(a). The maximum standard deviation of delay at the end (output of 74th tap) of TDL is 20 ps.

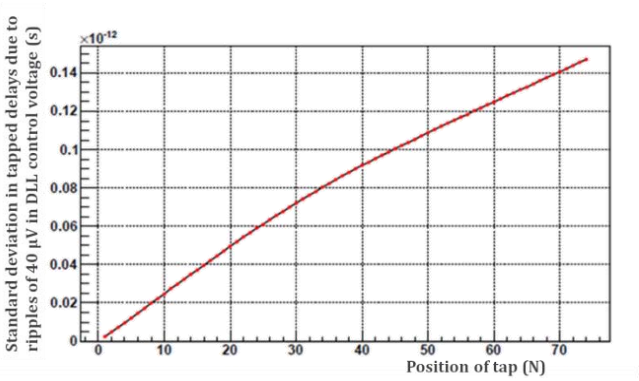
The ripple of 40 µV in the DLL control voltage after attaining the locked state also causes variation in tapped delays. This is evaluated by simulating the extracted netlist of TDL with DLL for 1000 number of clock cycles. The standard deviation of delay variation is shown in Fig. 7(b) with maximum value of 0.14 ps at the end of delay line.

To find the variations in tapped delays due to device component noise, noise coupling through parasitics and variation in layout drawing, the extracted netlist of TDL is accurately simulated by Spectre simulator with transistor noise models. The maximum delay variation is 17 ps as shown in Fig. 7(c) and its RMS value is 10 ps.

The RMS quantization error for the resolution of 174 ps is evaluated by: 174 ps/$\sqrt{12}$ = 50.28 ps. The total theoretical RMS error in TI measurement, considering above evaluated RMS delay variations and quantization error, is calculated as 55.02 ps.



(a)



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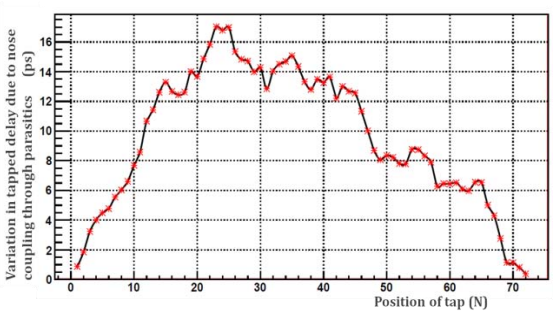
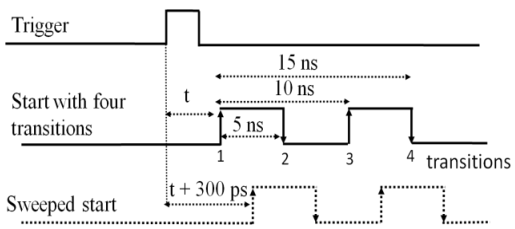


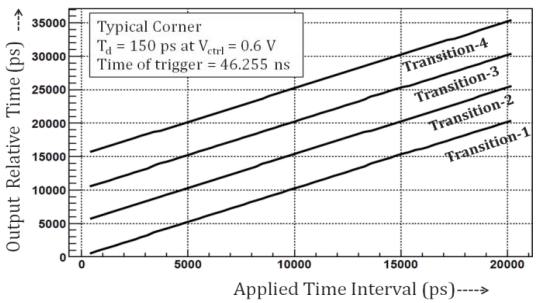
(c)

Fig. 7 : Standard deviation of tapped delays versus Position of Tabs (a) due to device mismatch using Monte Carlo simulator (b) due to ripples of 40 µV in control voltage provided by DLL (c) variation in tapped delay due to noise coupling and device component noise

The performance of time stamping is verified by using Spectre Verilog simulator. The linearity of measured output versus applied input characteristic is verified by applying a linear sweep of start event (Fig.8 (a)) in steps of 300 ps with respect to trigger over 20 ns with the help of Verilog test bench. On typical (TYP) corner, the measured relative time of hits is in agreement with the applied time steps as shown in Fig. 8(b). This test is also successfully carried out on slow (WS) corner for CBL delay of T_d = 200 ps (control voltage = 0.1 V) as shown in Fig. 9(a). The linearity of time stamping over full dynamic range of 40 µs is also verified by applying a linear sweep of 'start' with time steps of 223 ns with respect to trigger. Fig. 9(b) shows the plot of relative time versus applied time step for first transition on TYP corner.

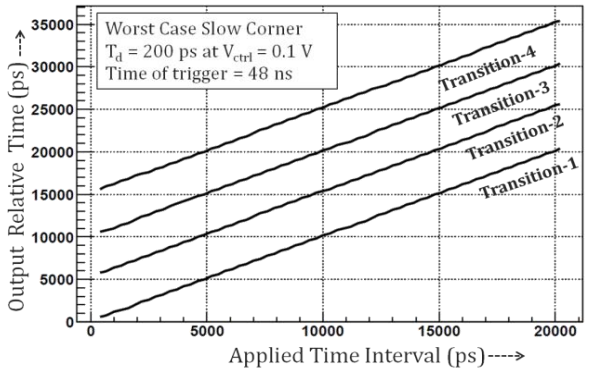


(a)

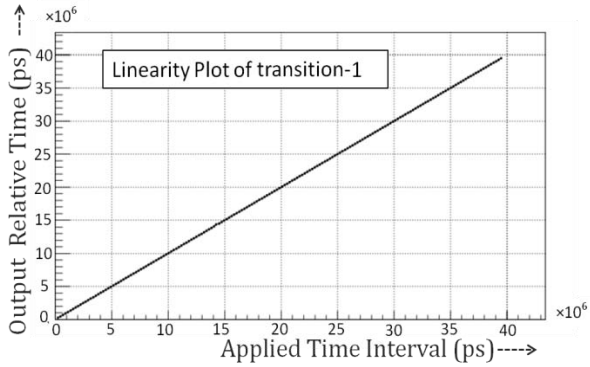


(b)

Fig. 8 : (a) Applied Input pattern of 'start' signal (b) Plot between Relative Time versus Applied Time on typical corner



(a)



(b)

Fig. 9 : Plot between Relative Time versus Applied Time (a) on WS corner with Td = 200 ps over 20 ns range (b) On typical corner with resolution of 150 ps over 40 μs range

IV. Conclusions

The TDC based on CBL logic achieves improved resolution in 0.35μm CMOS technology. The designed architecture of time stamping allows tunable resolution with least value of 136 ps. Across PVT variations; the attained resolution is 174 ps by stabilizing the CBL delay with the help of DLL. The CBL buffer provides identical rising and falling edge delays, which enables to control both delays with a single DLL feedback loop which in turn reduces design complexity. The designed TDC can be utilized in TI and Multi-hit operating modes with dynamic range of 40 μs. The multi-hit operating mode features pulse width measurement of 'start' signal with duration better than ~5 ns, which is independent of used clock frequency. Also, it enables measurement of delayed events over range of 40 μs. This design is successfully tested for its linearity as well as robustness across design process corners. The theoretical RMS error in time interval measurement is calculated as 55.02 ps.

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