

Designing of 3D Transistor based Home Appliances for Low Power Dissipation through Cost Analysis

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Abstract

With the reference for need of human beings to develop the low power dissipation based device which operates in very low power and reduce the cost for operation and design of device. This paper is an attempt to introduce the reader into the world of VLSI Technology and its implementation on Fabrication for designing the device. Our endeavor is to create the new invention on device which features very low power dissipation and cost reduction in designing this type of transistor through fabrication process for starting the revolution in the field of consumer electronics.

Index terms— introduction, description of 3D transistor, critical role of transistor, application in home appliances, theoretical specification and analysis, pract

1 Introduction

The Electronic devices play a very important role in fabrication and designing through operation in VLSI Technology as the feature of Low Power Dissipation and Size Reduction in Device. This VLSI Technology provides the various future aspects for Low Power Dissipation and Cost Reduction in operation or design aspects for fabrication. This technology provides the platform for various Researchers to enable this technology operating on nano watts of power with very small size performing the features.

The fabrication of VLSI Technology based on the Compact Size, Integration of Components and packaged Multiple Components in a Silicon Chip with Silicon Vias Technology. The 3D Transistor provides the fabrication up to 16 nm technology through feasibility in consumer electronics based devices. The present Fabrication Technology which fabricates up to 32 nm of technology for designing the layout of transistor. The components used for fabrication of Home Appliances based device is a microcontroller based application that provides the key features for using very less components and reduction in size of transistors.

This technology provides the various concepts for designing aspect, low power dissipation and reduction in size for packaging of transistors. The packaging of transistor is based on various aspects for designing, small size and low power dissipation in transistor characteristics.

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2 Description of 3D Transistor

The 3D Transistor is the transistor that supports the 16 nm technology for designing aspects through packaging and integration density of Integrated Circuits. The 3D Transistor provides the technology for operating the home appliances based devices like Television, Cell Phone, Refrigerator, Air Conditioner, Computer Peripherals and Electronic Tablets to perform this technology with low cost design, transistor packaging and reduction in size of transistors. The term low cost design refers to that its manufacturing cost will be very less and it can be around 10% of original price. The design and implementation process for making 3D Transistor is based on the software based fabrication process which provides the novel 3D Transistor at 22 nm technology for provide the computer

applications in microprocessor based devices. The 3D Transistor provide this features for 16 nm technology at home appliances based applications in microcontroller based devices. The 3D Transistor is the transistor that provides the VLSI Technology up to 22 nm size for microprocessor based devices and 16 nm for microcontroller based devices.

The 3D Transistor is based on Three Dimensional View for changing the structure of Gate with increasing its height and reducing its length for inventing the features of operation of two transistor in single Silicon Substrate. This terminology provide the various features for reduction in size, low power dissipation, less packaging density and easily designing of circuits that give the digital processing for operation of signals. The manufacturing device from this technology (3D Transistor) is based on digital aspects for analyzing and removes the analog system portion in the electronic circuits. This technology provide the easy level for processing of digital signals that would be much easier for analyzing and synthesizing the electronic circuits through this technology of 3D or FinFET Transistor in the application of consumer electronics based device. This 3D Transistor has shown similarities as FinFET Transistor because its size of "Gate" Structure which structured as "Fin" shape of fish that provide the practical aspects view for designing this T type of transistor in different fabrication labs of different countries. The Critical Role of Transistor depends on the designing of "Gate" Structure which tends to change the structure of transistor for performing the new invention in this transistor that can work in all electronic circuits based on home appliances. This is the Critical Role of Transistor that performs the changing of Gate Structure provide the new structure and operation of this new innovative 3D Transistor.

3 Critical Role of Transistor

In our Human Body, the Brain is the most essential and important organ for controlling all the body parts. This terminology also related with 3D Transistor for the designing of "Gate" Structure (main part of transistor) tends to change the structure, operations and size density of this innovative 3D Transistor which is applicable for operating a Home Appliances based device in the field of Consumer Electronics. The use of this technology in Consumer Electronics will reduce its manufacturing cost or original price for less operations, reduction in size of transistor and easy smooth designing of electronic circuits through using this Silicon Vias Technology in fabrication of 3D Transistor based Home Appliances. The 3D Transistor provides the various aspects and features in applications of home appliances. The device which has fabricated from 3D Transistor through Silicon Vias Technology provide the feature of high speed efficiency, increasing clock speed, low power consumption, very low manufacturing cost, easy smooth designing of circuits, enable of digital processing, unsupported the analog components, reduction in size, easy analyzing and synthesizing of electronic circuits. The application of 3D Transistor provides the various features and advantages: a) Television This device provide the high speed efficiency, very low power dissipation, high screen resolution display, high graphics and improvement in visualization characteristics for better quality videos and pictures.

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5 Application in Home Appliances

6 b) Cell Phone

Cell Phone provide the features of high speed processing, ultra low power dissipation, high screen display resolution, very high speed signal processing, implement to 5G and 6G mobile communication technology for future prospective. c) Electronic Tablet Electronic Tablet performs the high speed internet processing, high screen resolution display, better quality resolution of video and pictures, virtual gaming zone, implement to 5G and 6G mobile communication for processing of networks.

7 d) Computer Peripherals

The Computer Peripherals perform the high speed processing, increase the clock speed up to 20-50 GHz, increase the RAM (processing speed) and implement Fifth Generation of Humanoid Computing Devices.

8 e) Air Conditioner and Refrigerator

Air Conditioner and Refrigerator perform the various features for digital processing, very low power dissipation (enable for operation through DC Source) and sixth sense features for operating the device through user friendly manner and cost reduction for manufacturing the device.

V.

9 Theoretical Specification and Analysis

The theoretical specification and analysis of 3D Transistor based on the various features for designing, operations, implement on fabrication and change the fabrication structure. This strategy provide the theoretical details for the operation of present layout of 2D Transistor and design prospective layout of 3D Transistor. The 3D Transistor provides increase in height of Gate which tends to increase in height of Oxidation Layer and operating this 3D Transistor as operation of two transistors in single Silicon Substrate for the enhancement of Source and Drain

in 3D Transistor which will have fabricated by Silicon Vias Technology. The 2D Transistor provides the Gate designing on the basis of MOSFET or MESFET or IGFET Structure which could developed by fabrication process.

10 Practical Specification and Analysis

11 Process of Fabrication

The process of fabrication is based on the following features that implements through Silicon Vias Technology for converting the design layout of project to fabrication of transistors. These processes can be defined in various small following points which tend to characterize this process are:

12 Result and Conclusion

From here, I have now discussed all the points related to 3D Transistor based Home Appliances for low power dissipation, reduction in size through cost analysis and synthesis for the testing of electronic circuits fabricated from layout of 3D Transistor to become the most efficient technologies in future prospective. This terminology will create a new revolution in the production of Consumer electronics based devices which reduces manufacturing cost, high processing speed of device and easiest complexity of transistor to be packaged on a electronic circuit through inventing the digital revolution of generation in the field of electronics.

The 3D Transistor based Home Appliance is the starting era of technology for designing the home appliance based devices which invents for being applicable this technology to home appliances. The present scenario of technologies which are applicable for this Silicon Vias Process manufactures the Microprocessor, Microcontroller, Integrated Circuits and Embedded System based Devices which is a very complex processing device. This technology of 3D Transistor provide the various aspects for designing and implementing the electronic circuit through Silicon Vias Technology which tends to low power dissipation, high processing speed, easier packaging of device and reduction in size to become the digital generation of revolution in the world.



Figure 1: Fe

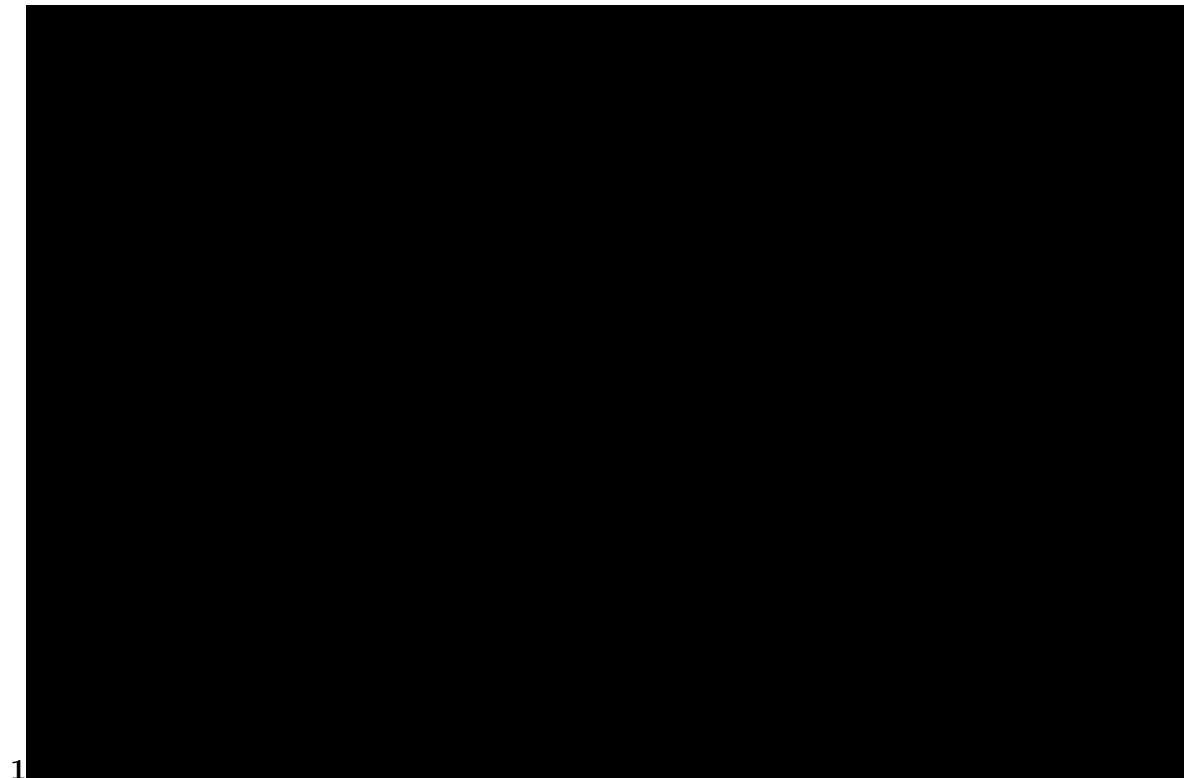


Figure 2: Figure 1 :

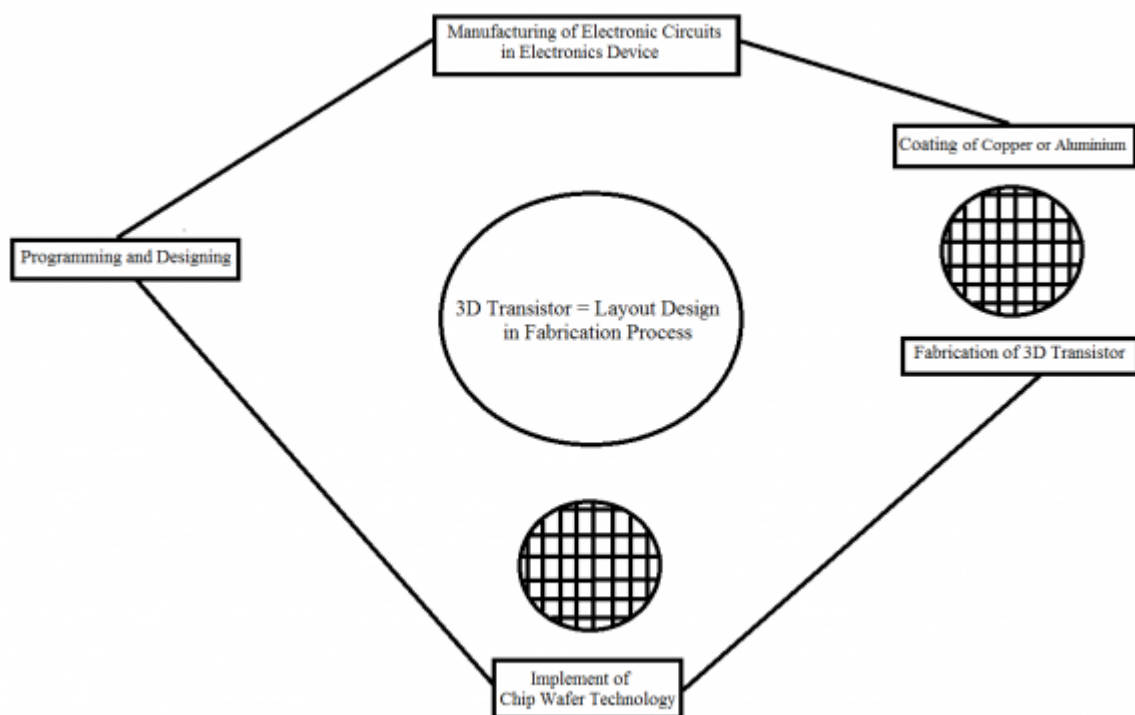


Figure 3: (

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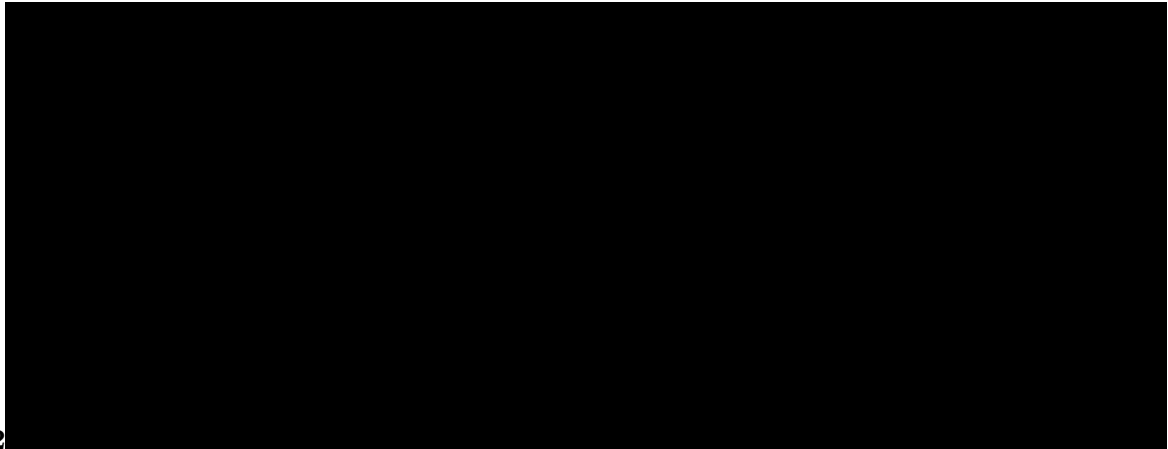
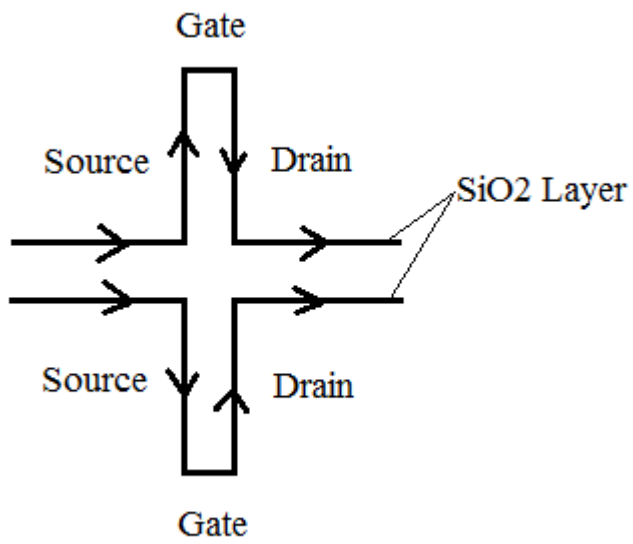


Figure 4: Figure 2 :



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Figure 5: FFigure 3 :

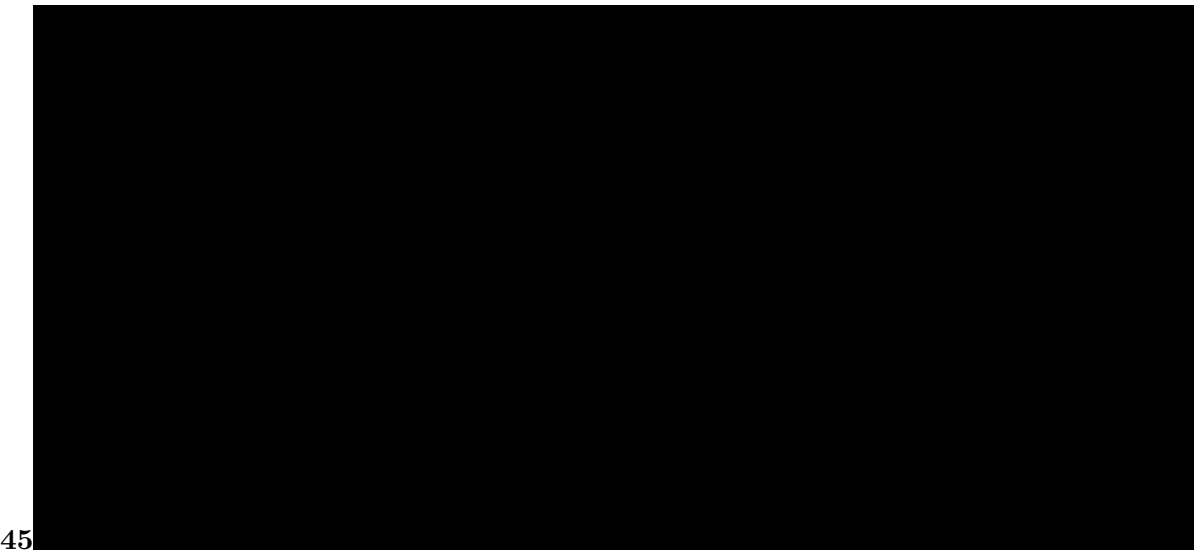


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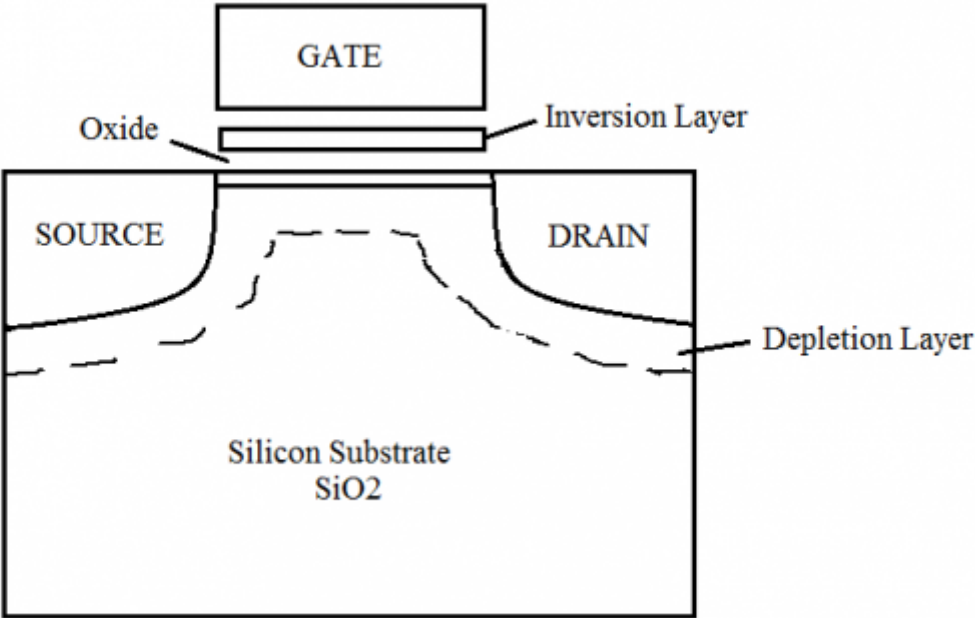


Figure 7: FFigure 7 :

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Figure 8: Year 2015 FFigure 8 :

.1 Global Journal of Researches in Engineering () Volum

Year 2015

- [Goorey and Poole] ‘An Introduction to High Performance Laminates and the Importance of Using Chemical Process in PCB Fabrication’. M Goorey , M Poole . *Rohm and Haas Electronic Materials*,
[Chen et al. (2007)] ‘Analysis and Suppression of Inductive Interference in Active Integrated Power Electronics Module’. Qiaoliang Chen , Xu Yang , Zhaoan Wang , Lianghua Zhang . *Power Electronics Specialists Conference 2007 (PESC’07)*, June 2007. p. .
[Berti and Muraka (1995)] ‘Characterization of PVD-TiN as the Diffusion Barrier/Adhesion Promoter for use in a multilevel copper Interconnection Technology’. A Berti , S P Muraka . *University/ Government/ Industry Microelectronics Symposium*, 1995. May 1995. p. . (Proceedings of the Eleventh Biennial)
[Simonot et al.] *Design and Characterization of an Integrated CMOS Gate Drive for Power MOSFETs*, T Simonot , N Rouger , J C Creiber . ECCE 2010.
[Kong et al. (2007)] ‘Design of a Synchronous -Rectified Back Bootstrap MOSFET drives for Voltage Regulator Module’. Ming Kong , Wei Yan , Wenhong Li . *ASIC 2007, ASICON’07, 7 th International Conference*, October 2007. p. .
[Hopkins ()] ‘Designing with Thermal Impedance’. T Hopkins . *SGS-Thompson Application Note AN261/0189, Semitherm Proceeding*, 1988.
[Kengen et al.] ‘Development of Matrix Clip Assembly for Power MOSFET Packages’. M Kengen , W Peels , D Heges . *Microelectronics and Packaging Conference 2009 (EMPC’09)*, (European Voulme 4)
[Stockneier (2008)] ‘From Packaging to ”Un”-Packaging Trends in Power Semiconductor Modules’. T Stockneier . *Power Semiconductor Devices and IC’s 2008, ISPSD’08, 20 th International Symposium*, May 2008. 1 p. .
[Scott Bruce Clendenning et al. (2011)] ‘Indian Patent Office: 790/DEL/2013; Inventor: Prashant Kumar’. Niloy Scott Bruce Clendenning , Ravi Mukherjee , Pillarisetty . Patent: US 7964 490 B2. *Methods of Forming Nickel Sulfide Film on a Semiconductor Device*, June 21, 2011. March 19, 2013. 18. (Application of Innovative 3D Transistor in Home Appliances)
[Kliger (2003)] ‘Integrated Transformer -Coupled Isolation’. R Kliger . *IEEE Xplore* March 2003. 6 (4) p. . (Instrumentation and Measurement Magazine)
[Liu et al. ()] R S Liu , C C You , M S Tsai , S F Hu , K Lee , J Lu . *Growth of Nano Sized Copper Seed Layer on TiN and TaSiN by new Non-Toxic Electroless Plating*, 2002. 2002. 2002. p. . (Proceedings 2002, 2 nd IEEE Conference)
[Creiber and Rouger (2008)] *Loss Free Gate Driver Unipolar Power Supply for High Side Power Transistors*, J C Creiber , N Rouger . May 2008. 23 p. .
[Luechinger (2007)] ‘Ribbon Bonding -A Scalable Interconnect for Power QFN Packages’. C Luechinger . *Electronics Packaging Technology Conference (EPTC) 2007*, December 2007. 9 p. .
[Sage and Gross] M G Sage , D R Gross . *Trends in MCM and Microelectronics Assembly*, MCB Up Limited.
[Weide (2008)] ‘Simulation of Migration Effect in Solder Bumps, Device and Material Reliability’. K Zaage Weide . *IEEE Transactions*, September 2008. 8 p. .
[Rouger and Crebier (2008)] ‘Toward Generic Fully Integrated Gate Driver Power Supplies’. N Rouger , J C Crebier . *Power Electronics on IEEE Transactions*, July 2008. 23 p. .
[Rochr and Shiner ()] ‘Transisient Thermal Resistance -General Data and Its Use’. Bell Rochr , Brycer Shiner . *AN569 in Motorola Power Applications Manual*, 1990. p. .