

Area Efficient Layout Design of Multiply Complements Logic (MCL) Gate using QCA Technology

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Abstract

Quantum dot Cellular Automata (QCA) is one of now popular technology for its highly scalable feature and ultra low power consumption that made its one of the promising alternatives to CMOS technology. This paper present a new layout design of Multiply Complements Logic (MCL) gate based on QCA inverter (INV), QCA wire and QCA majority voter (MV) gates. To verify and simulate the proposed gate QCA Designer and Microwindlite tools are employed. The simulation result confirmed the correctness of the proposed circuits and comparison shows the area efficiency of QCA over CMOS technology. This proposed design layout has a promising future in constructing ultra low power exhausting information processing system and can stimulate higher digital applications in QCA.

Index terms— QCA inverter (INV), QCA wire, QCA majority voter (MV) gate, QCA Designer and MICROWIND.

1 Introduction

anotechnology provides new possibilities for computing due to the unique properties that arise at such reduced feature sizes. Among this new devices, Quantum-dot Cellular Automata (QCA) [1,2] relies on new physical phenomena (such as Coulombic interactions), and innovative techniques that radically depart from a CMOS-based model. QCA not only gives a solution at nano-scale, but it also offers a new method of computation and information [3,4]. Consider the processing features of QCA technology, the basic element is cell that can be used as an information processing unit (perform logical operation), while others (i.e. wires) are used for information transfer and communication. In information processing reversible logic circuit made a great attention in recent years. It is addressed that the reversible logic gates are promising computing paradigm with applications in emerging technologies such as quantum computing, quantum dot cellular automata, optical computing, etc. [5][6][7][8]. In Quantum computing we found there are many proposals on Reversible Logic Gate (RLG) design like Feynman Gate [9], Toffoli Gate [10], Fredkin Gate [11], NFT Gate [12] but very few of them are being designed in QCA [13,14].

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2 Materials and Methods

The QCA cell is the basic building block of QCA. Four quantum dots that consist of a QCA arranged in a square pattern. These quantum-dots are sites in which electrons are able to tunnel between them but cannot leave the cell. The basic cell constructed from four quantum dots with two mobile electrons which can move to different quantum dots by means of electron tunneling. Columbic repulsion will cause the electrons to always occupy diagonally opposite dots.

The two stable polarization of electrons $P = +1.00$ and $P = -1.00$ of a QCA cell represents logic '1' and logic '0' respectively, shown in figure 1. QCA wires can be either made up of 90 0 cells or 45 0 cells. 45 0 cells are

used for coplanar wire crossings (Figure ??). In case of Inverter, if place two cells at 45 0 with respect to each other they interact inversely. An array of QCA cells acts as a wire and is able to transmit information from one end to another, i.e., all the cells in the wire will switch their polarizations to follow that of the input or driver cell. $P = -1$ $P = +1$ Quantum dot Electron (a) (b)

3 Mcl Gate

In this section describe the 3×3 MCL (Multiply Complements Logic) Gate. Reversible Logic gate is defined as input vector and output vector must be with one to one correspondences. The MCL gate maps the inputs A, B, C to $P = (B+C)?$, $Q = (A+B)?$, $R = A$. Table ?? represents the truth table of this gate and figure 5 shows the QCA block diagram of MCL gate. QCA Designer [16,17] is the product of an ongoing effort to create a rapid and accurate simulation and layout tools for quantum-dot cellular automata (QCA). Figure 6 shows the simulated gate design of MCL gate, where A, B, C and P, Q, R are the input and output cell respectively. ii. CMOS simulation For design and simulation the MCL gate in CMOS we used PC tools MICROWIND [18]. This tool is very user-friendly to design and find out the covered area of any logic gate.

4 Table 1 : Truth Table of the MCL gate

A	B	C	P=B'C'	Q=A'B'	R=A
0	0	0	1	1	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1

5 Result Comparison

In this section show that, designed MCL gate in QCA, how much area efficient than CMOS. Here show the comparisons that have calculated area using QCA Designer and MICROWIND [18]. Table 2 shows the designing parameter Figure 9 shows the covered area comparison between CMOS technology and QCA technology. For this comparison different designing technology are employed in MICROWIND.

6 Conclusions

QCA is one of the emerging nano-technologies in computing paradigm which is capable to design highly saleable logic device also suitable for implementing reversible logic gates. This paper presented an area efficient layout design of Multiply Complements Logic (MCL) gate in QCA which is 118 times smaller in size than 45 nm CMOS technology. The simulation has done using QCA Designer and MICROWIND. ¹



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Figure 1: Figure 1 :

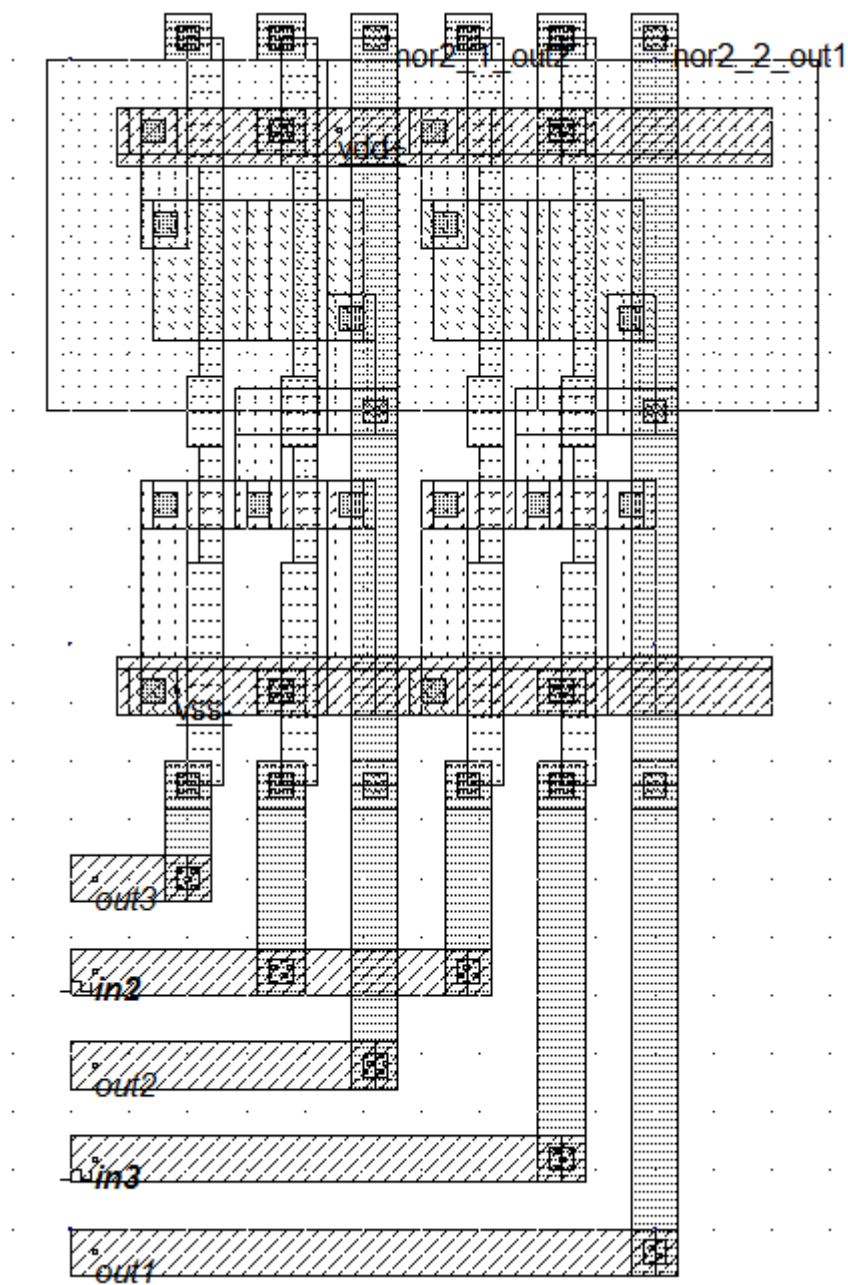


Figure 2:

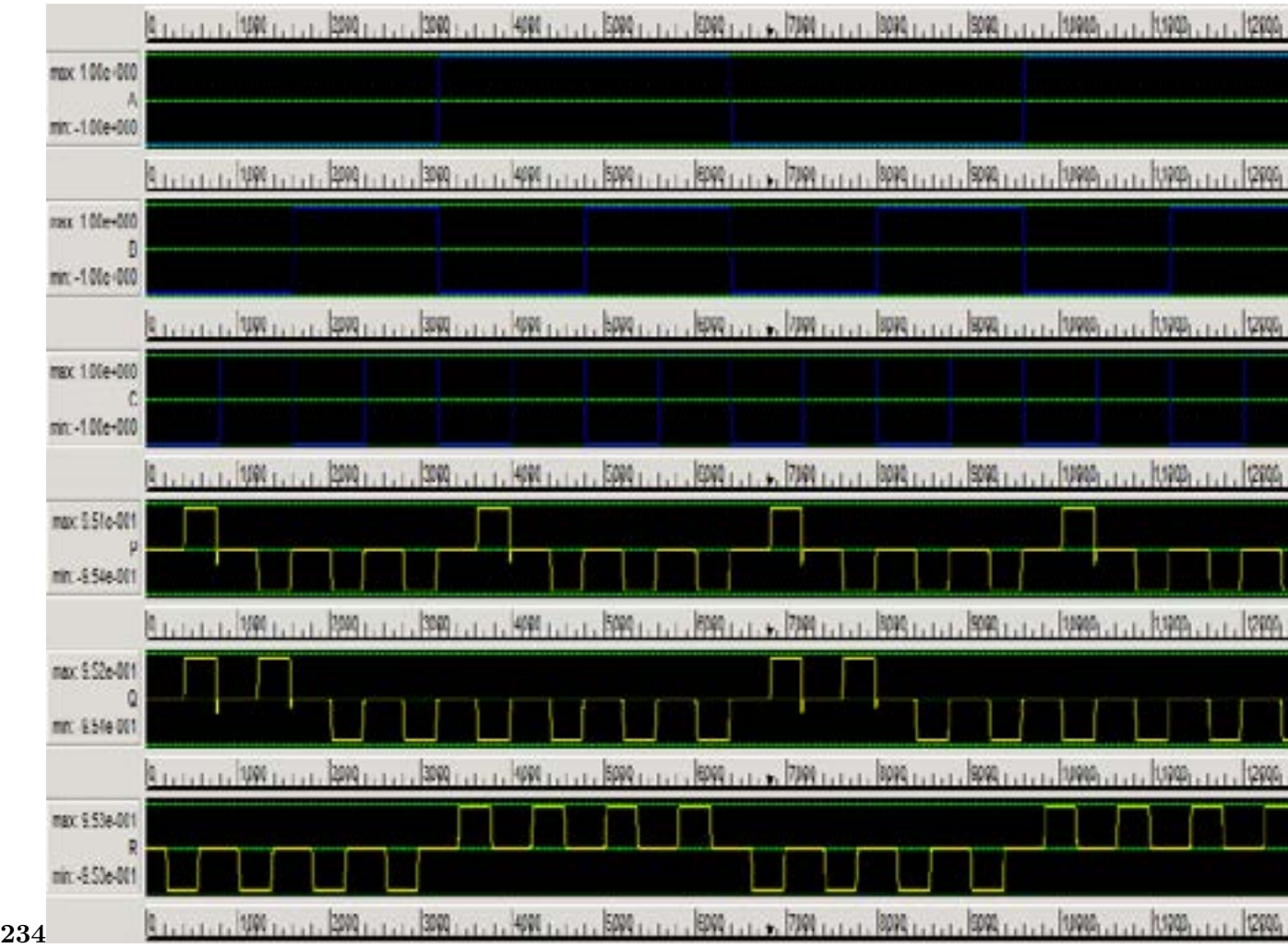


Figure 3: Figure 2 :Figure 3 :Figure 4 :

2

Parameters	CMOS technology			
	MCL Gate			
Number of cells	24			
Number of Majority Voter gate	2			
Time delay (clock cycle)	0.5			
Covered area (size) in QCA (μm^2)	0.038			
Covered area (size) in CMOS (μm^2)	4.5			
Improvement (in times)	118.42 times			
	18	17.8		
	16			
	14			
	12			
2)	6 8 10	8.7	4.5	
Covered area (μm^2)	4			
	2			
	0		0.038	
	90 nm	65 nm	45 nm	QCA
		Used Technology		

Figure 4: Table 2 :

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