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# Area Efficient Layout Design of Multiply Complements Logic (MCL) Gate using QCA Technology

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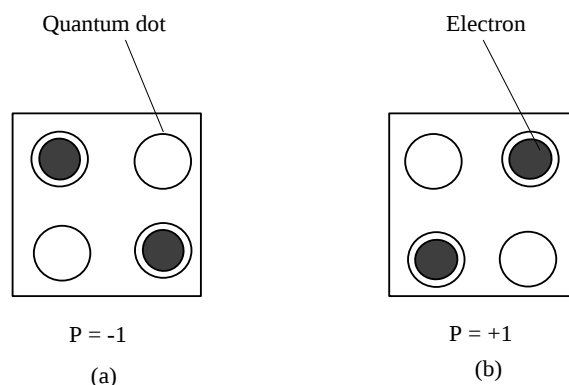
## I. INTRODUCTION

Nanotechnology provides new possibilities for computing due to the unique properties that arise at such reduced feature sizes. Among this new devices, Quantum-dot Cellular Automata (QCA) [1, 2] relies on new physical phenomena (such as Coulombic interactions), and innovative techniques that radically depart from a CMOS-based model. QCA not only gives a solution at nano-scale, but it also offers a new method of computation and information [3, 4]. Consider the processing features of QCA technology, the basic element is cell that can be used as an information processing unit (perform logical operation), while others (i.e. wires) are used for information transfer and communication. In information processing reversible logic circuit made a great attention in recent years. It is addressed that the reversible logic gates are promising computing paradigm with applications in emerging technologies such as quantum computing, quantum dot cellular automata, optical computing, etc. [5-8]. In Quantum computing we found there are many proposals on Reversible Logic Gate (RLG) design like Feynman Gate [9], Toffili Gate [10], Fredkin Gate [11], NFT Gate [12] but very few of them are being designed in QCA [13, 14].

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## II. MATERIALS AND METHODS

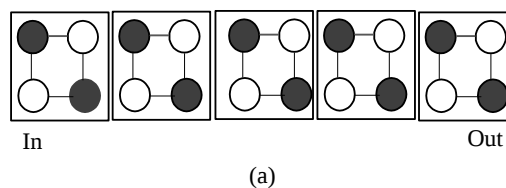
The QCA cell is the basic building block of QCA. Four quantum dots that consist of a QCA arranged in a square pattern. These quantum-dots are sites in which electrons are able to tunnel between them but cannot leave the cell. The basic cell constructed from four quantum dots with two mobile electrons which can move to different quantum dots by means of electron tunneling. Columbic repulsion will cause the electrons to always occupy diagonally opposite dots. The two stable polarization of electrons  $P = +1.00$  and  $P = -1.00$  of a QCA cell represents logic '1' and logic '0' respectively, shown in figure 1.



**Figure 1 :** Basic QCA cell and binary encoding (a) polarization=-1 and (b) polarization= +1

### a) QCA Wire

QCA wires can be either made up of  $90^\circ$  cells or  $45^\circ$  cells.  $45^\circ$  cells are used for coplanar wire crossings (Figure 2). In case of Inverter, if place two cells at  $45^\circ$  with respect to each other they interact inversely. An array of QCA cells acts as a wire and is able to transmit information from one end to another, i.e., all the cells in the wire will switch their polarizations to follow that of the input or driver cell.



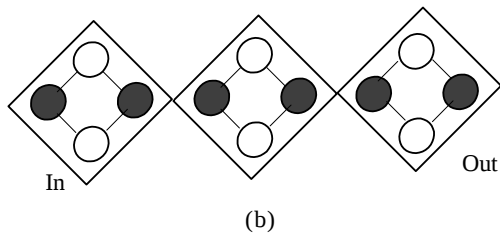


Figure 2 : QCA (a) 90° wire (b) 45° wire

### b) QCA Inverter

QCA Inverter returns the opposite value of input value. This inverter is made of eight cell or four QCA wires. The input polarization is split into two polarizations and in the end, two wires join and make the reverse polarization shown in figure 3.

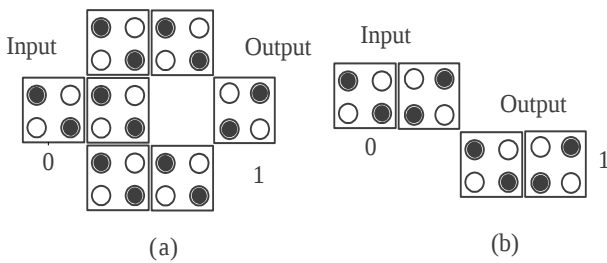


Figure 3 : QCA inverter

### c) Majority Voter

Majority Voter [15] (MV) is described as logic function  $MV(A, B, C) = AB + BC + CA$ . MV can be realized by 5 QCA cells, as shown in Figure 4 (a). Using QCA majority voter two basic gates “AND” and “OR” can be implemented by setting one of the input fixed to 0 or 1 value. Figure 4 (b) Shows when  $C=0$  then Output is  $AB$  that indicates the AND operation and when  $C=1$  then Output is  $A+B$  that means OR operation shown in figure 4(c).

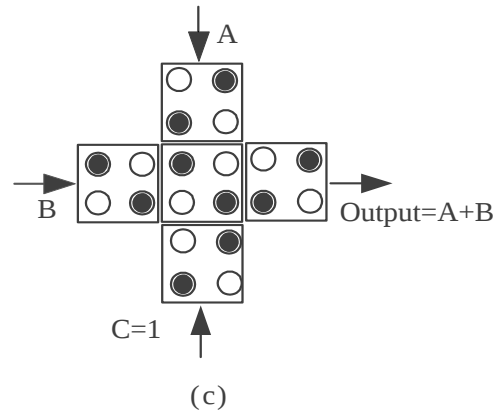
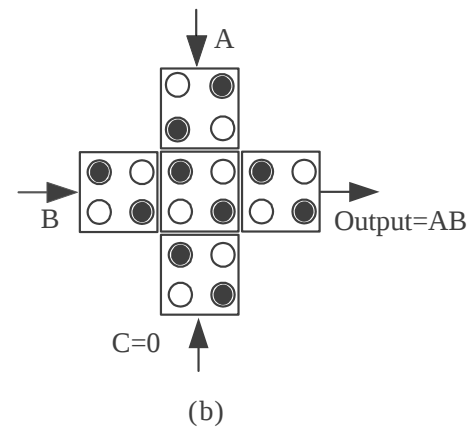
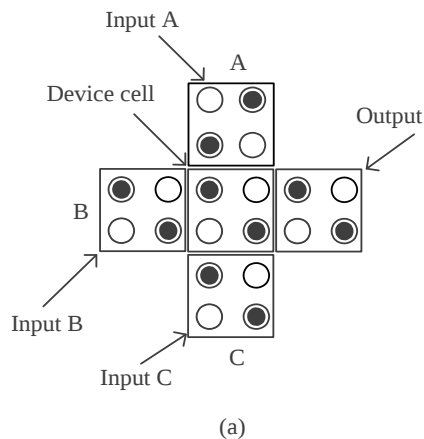


Figure 4 : (a) Majority Voter Gate (b) perform AND operation ( $c=0$ ) and (c) OR operation ( $c=1$ )

## III. MCL GATE

In this section describe the  $3 \times 3$  MCL (Multiply Complements Logic) Gate. Reversible Logic gate is defined as input vector and output vector must be with one to one correspondences. The MCL gate maps the inputs  $A, B, C$  to  $P = (B+C)'$ ,  $Q = (A+B)'$ ,  $R = A$ . Table 1 represents the truth table of this gate and figure 5 shows the QCA block diagram of MCL gate.

Table 1 : Truth Table of the MCL gate

| A | B | C | $P = B'C'$ | $Q = A'B'$ | $R = A$ |
|---|---|---|------------|------------|---------|
| 0 | 0 | 0 | 1          | 1          | 0       |
| 0 | 0 | 1 | 0          | 1          | 0       |
| 0 | 1 | 0 | 0          | 0          | 0       |
| 0 | 1 | 1 | 1          | 0          | 0       |
| 1 | 0 | 0 | 1          | 0          | 1       |
| 1 | 0 | 1 | 0          | 0          | 1       |
| 1 | 1 | 0 | 0          | 1          | 1       |
| 1 | 1 | 1 | 1          | 1          | 1       |

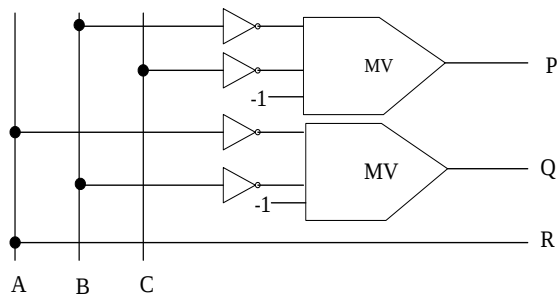


Figure 5 : QCA block diagram of MCL gate

#### a) Characterization of MCL Gate

As MCL gate is a reversible gate so it has equal number of inputs A, B, C and outputs P, Q, R. QCA block diagram of MCL gate shows that two majority gates and four not gates are used to perform logical operation. Output P obtained from the AND operation of B NOT and C NOT. Output Q obtained from the AND operation of A NOT and B NOT. Output R obtained from the input A.

#### b) Simulated Design Layout Of MCL Gate In QCA And CMOS

##### i. QCA simulation

QCA Designer [16, 17] is the product of an ongoing effort to create a rapid and accurate simulation and layout tools for quantum-dot cellular automata (QCA). Figure 6 shows the simulated gate design of MCL gate, where A, B, C and P, Q, R are the input and output cell respectively.

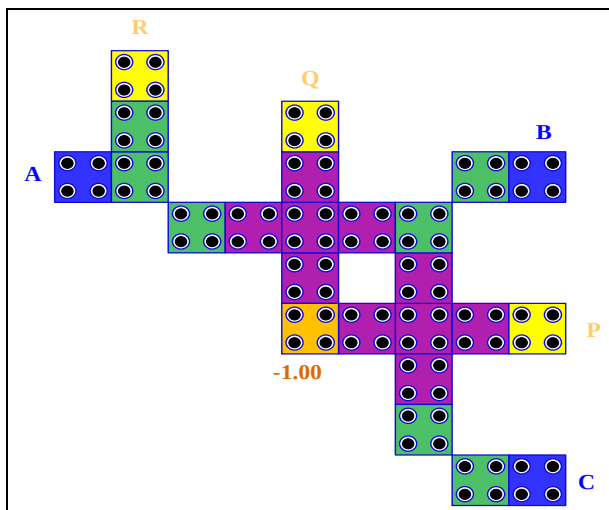


Figure 6 : Simulation of MCL Gate using QCA Designer

In figure 7, the simulated input output waveforms of MCL gate using QCA Designer is shown. In the output P has pass-through two clock zone, it indicates that P has a time delay of 0.5 (clock cycle) and on the other Q and R has no time delay. In figure 7 circle indicate the time delay in the output signal.



Figure 7 : Simulated input output waveforms of MCL gate with 0.5 clock cycle delay

##### ii. CMOS simulation

For design and simulation the MCL gate in CMOS we used PC tools MICROWIND [18]. This tool is very user-friendly to design and find out the covered area of any logic gate.

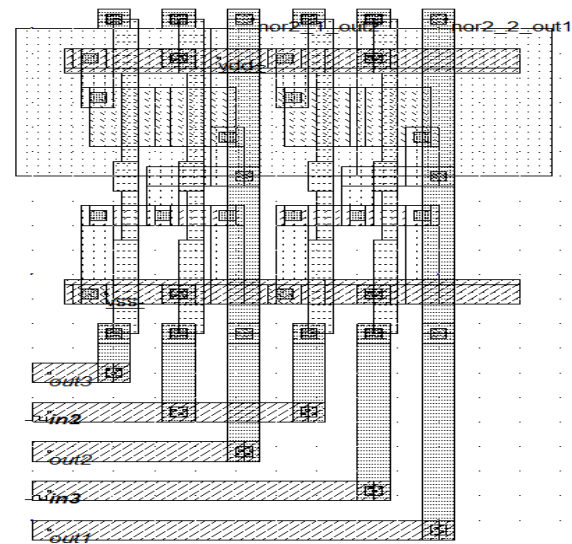


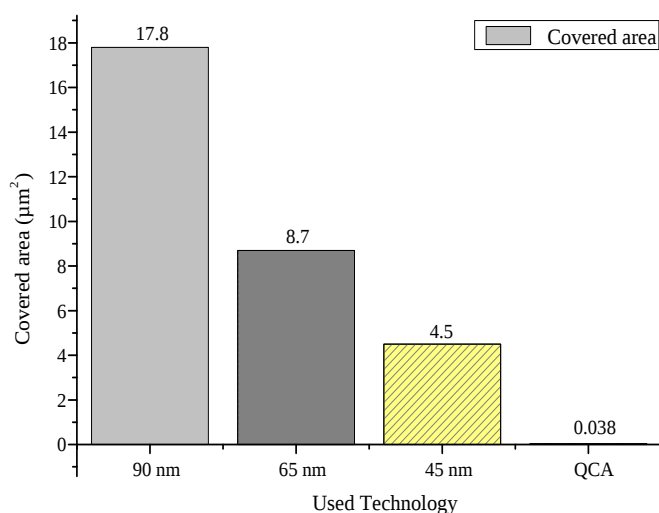
Figure 8 : Simulated gate layout of MCL gate in CMOS

## IV. RESULT COMPARISON

In this section show that, designed MCL gate in QCA, how much area efficient than CMOS. Here show the comparisons that have calculated area using QCA Designer and MICROWIND [18]. Table 2 shows the designing parameter Figure 9 shows the covered area comparison between CMOS technology and QCA technology. For this comparison different designing technology are employed in MICROWIND.

**Table 2 :** Designing Summary of MCL gate in QCA and CMOS technology

| Parameters                                      | MCL Gate     |
|-------------------------------------------------|--------------|
| Number of cells                                 | 24           |
| Number of Majority Voter gate                   | 2            |
| Time delay (clock cycle)                        | 0.5          |
| Covered area (size) in QCA ( $\mu\text{m}^2$ )  | 0.038        |
| Covered area (size) in CMOS ( $\mu\text{m}^2$ ) | 4.5          |
| Improvement (in times)                          | 118.42 times |

**Figure 9 :** Area in different versions of CMOS technology and QCA

## V. CONCLUSIONS

QCA is one of the emerging nano-technologies in computing paradigm which is capable to design highly saleable logic device also suitable for implementing reversible logic gates. This paper presented an area efficient layout design of Multiply Complements Logic (MCL) gate in QCA which is 118 times smaller in size than 45 nm CMOS technology. The simulation has done using QCA Designer and MICROWIND.

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