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Design of Low Power 4-Bit CMOS Braun Multiplier based on Threshold Voltage Techniques

Dayadi Lakshmaiah[1]

[1] CJITS,JANGON,WARNAGAL

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Abstract

A circuit design for a new Low Power 4-bit Braun Multiplier is presented. The multiplier is implemented by using different Threshold Voltage techniques. Power reduction techniques are proposed for 4-bit Braun Multiplier which is designed by Full Adders. To get Optimum design low threshold voltages are used at critical paths similar way high threshold voltages are used at non critical paths. The design uses CMOS digital circuits in order to reduce the power dissipation while maintaining computational throughput. This architecture is simulated at 90nm Technology with 1.2v power supply. The power dissipation of nearly 46

Index terms— braun multiplier, full adder,

1 Introduction

n order to achieve the high speed and low power demand in DSP applications Braun's multiplier are broadly used. The Braun's multiplier is generally called as the Carry Save Array Multiplier. The architecture of a Braun's multiplier consists of AND gates and full adders. The prolific growth in semiconductor device industry has been Indicates to the high performance portable systems with enhanced reliability in data transmission. In order to maintain the high performance fidelity applications, emphasis will be on incorporation of low power modules in future system design [1][2][3][4][5]. The design of such modules power consumption or dissipation in fundamental arithmetic computation units such as adders and multipliers. This implies a need to design low power multipliers towards the development of efficient power & high-performance systems. The selection of the most efficient implemented multiplication has continually challenge DSP system designers [6][7]. Every system designer offers a wide range of tradeoffs in terms of speed, complexity and power consumption. Input sequences to the multiplier can be fed in parallel, serial or a hybrid (parallel serial) this proposal approaches gives high processing speed. Usually Parallel multipliers are adopted at the expense of high area complexity.

2 Multiple

parallel multiplications Algorithms (architectures) [8] have been proposed to reduce the chip area increase the speed of the multipliers' and reduce the power dissipation using various techniques. Several of these techniques reduce the power dissipation by eliminating spurious transitions in the circuit [9,11]. The architecture is simulated with the cadence micro wind software. As shown in the above Table .1. The proposed work of the MOS transistors with normal threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work4 Power Delay Product 119 femito (10 -15), with Reference paper [11], it is observed that 46% of power Delay Product has been reduced.

3 II.

4 Proposed Work

( ) ( ) in in Sum A B C A B C = ? + ? (1) ( ) ( ) out in C A B C A B A = ? + ?**(2)**

As shown in the above Table .2. The proposed work of the MOS transistors with low threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work2 we got Power Delay Product 111 femito (10 -15), but comparatively to the Reference paper [11], it is 51% of power Delay Product has been reduced.

As shown in the above Table .3. The proposed work of the MOS transistors with high threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work1 Power Delay Product 120 femito (10 -15), with Reference paper [11], it is observed that 47% of power Delay Product has been reduced.

As shown in the above Table

5 Conclusion

The present paper demonstrated the improvement in parameters v/s, Area, power, and delay with reduction in number of transistors to implement Full adder circuits. The simulations were performed using 90nm Micro wind 3 CMOS layout CAD Tool In this paper power consumption & Power Delay Product is calculated the results are optimized power consumption of 46% and Power Delay Product is 56 % still the performance of 4-Bit CMOS Braun Multiplier is improved by incorporating techniques which support reduced transistor implementations.

Figure 1: A

[1]

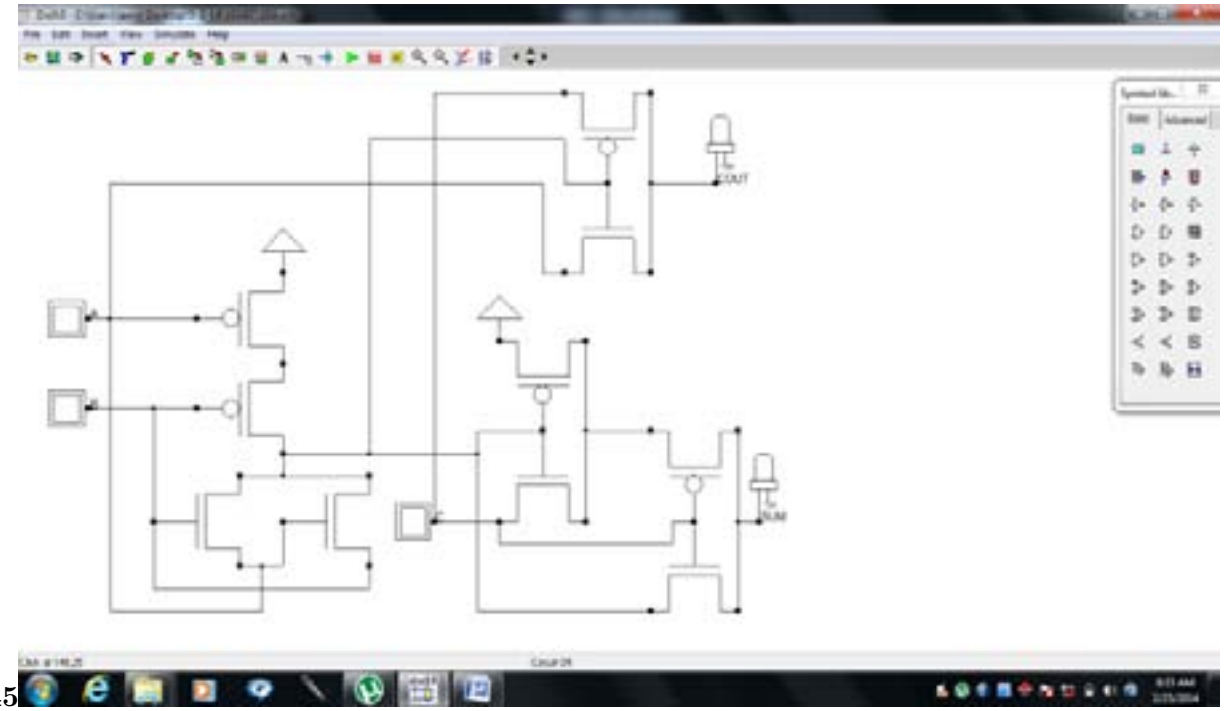

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Figure 2: Fig. 1 :Fig. 2 : 2 Fig. 3 : 3 Fig. 4 : 4 Fig. 5 :

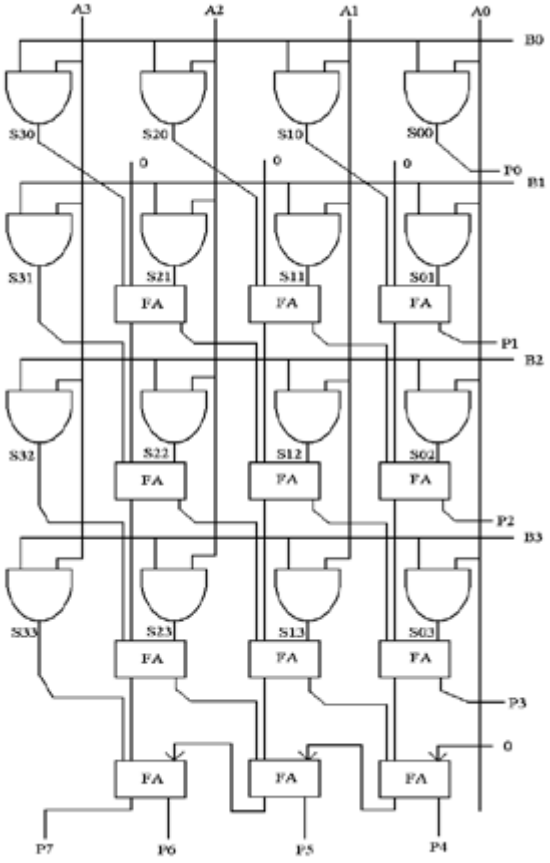

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Figure 3: Fig. 6 :

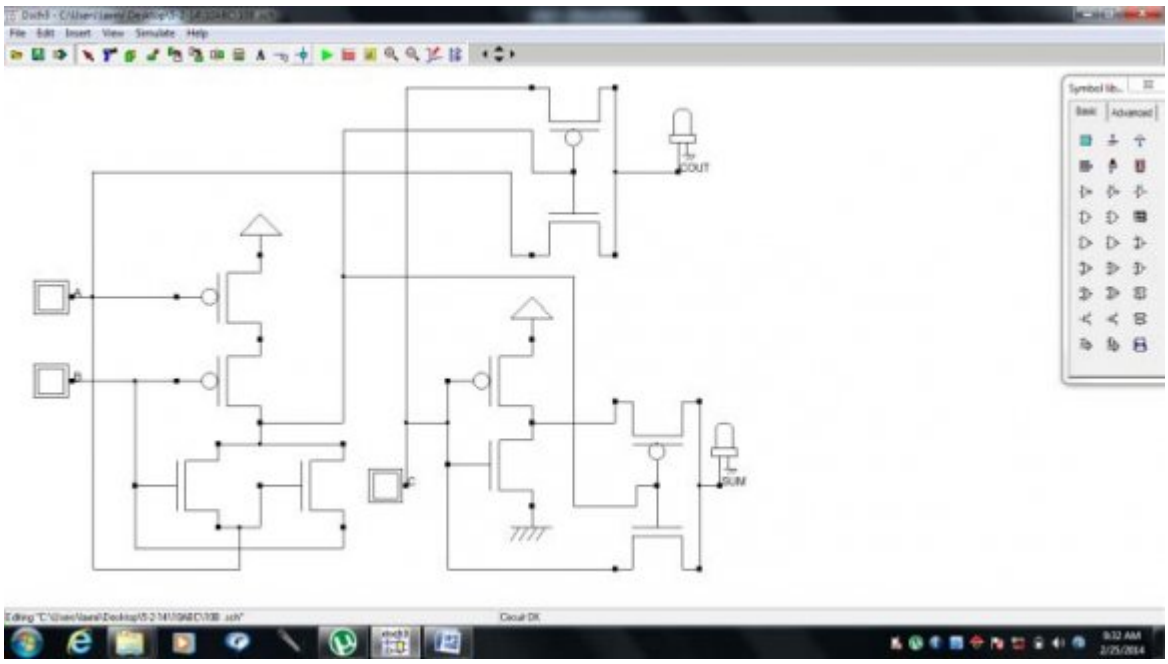

Figure 4:

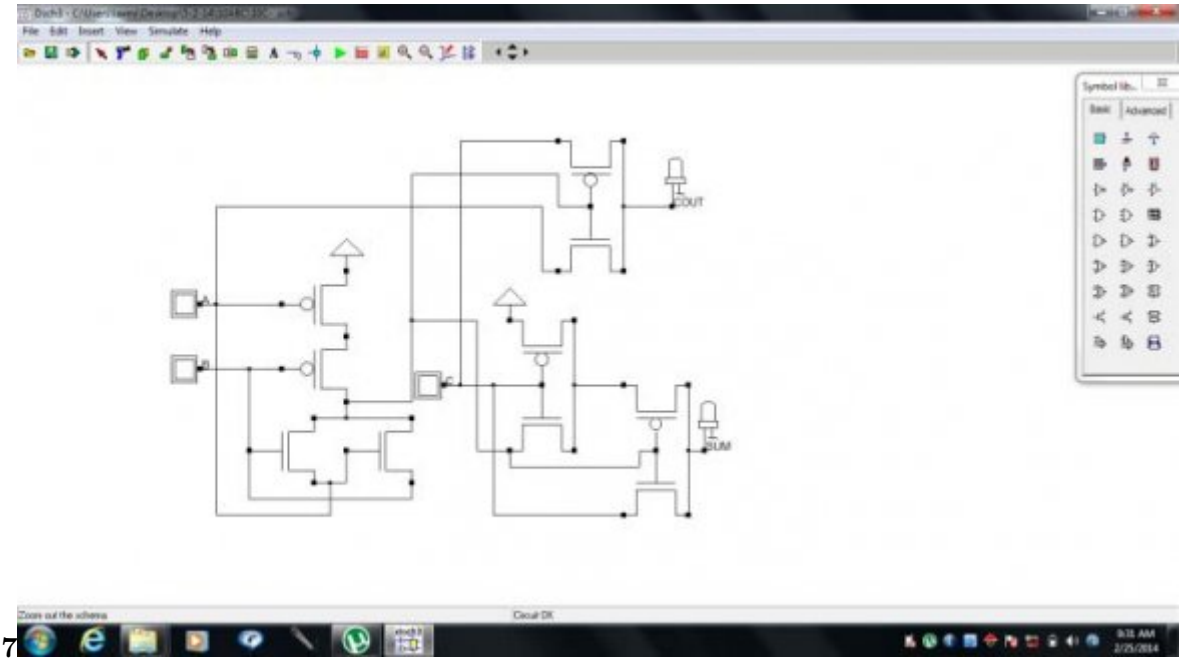

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Figure 5: Figure 7 :

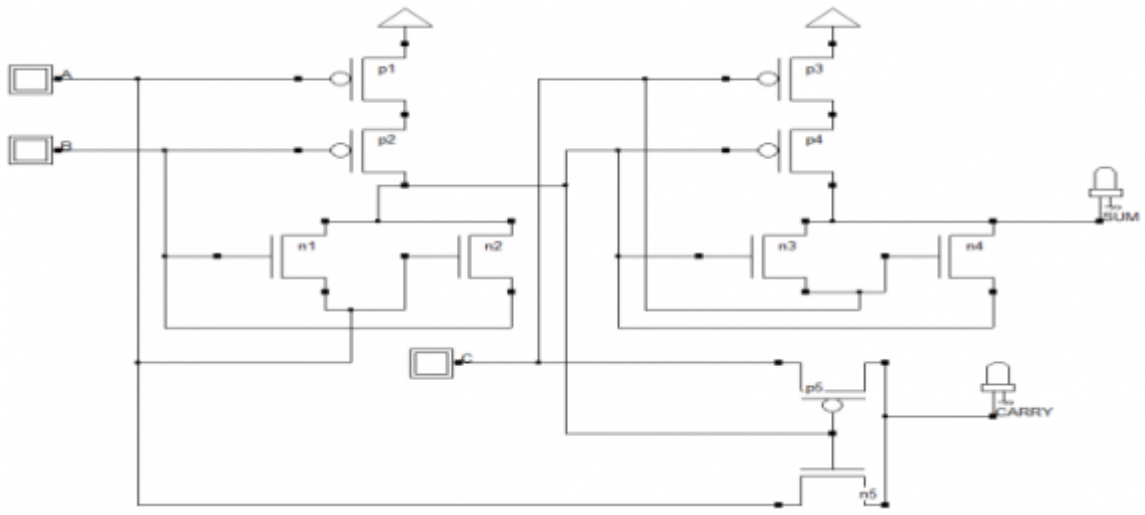

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Figure 6: Figure 8 : 4 -

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4-bit Multiplier proposed work2	60.055	4.270	256
4-bit Multiplier proposed work3	25.594	4.695	120
4-bit Multiplier proposed work4	74.600	6.860	511
4-bit Multiplier proposed work5	24.524	6.025	147

Proposed 4-bit Braun Multiplier Low V T (Low Threshold voltage) & High V T (High Threshold voltage) T

Multipliers Proposed	Power(µw)	delay(ns)	femito(10 -15) Power Delay
Proposed 4x4 Multipliers 2011 IEEE paper 4-bit Multiplier proposed work1 4-bit Multiplier proposed work2 2011 IEEE 4-bit Reference Multipliers paper 4-bit Multiplier proposed work1 4-bit Multiplier proposed work2 4-bit Multiplier proposed 2011 IEEE paper 4-bit Multiplier proposed work1 4-bit Multiplier proposed work2 4-bit Multiplier work3 4-bit Multiplier proposed work4 4-bit Multiplier proposed work5 work5 proposed work3 4-bit Multiplier proposed work4 proposed 4-bit Multiplier	Power(µw)	delay(ns)	Power Delay Product femito(10 -15) 237 144 111 237 Product femito (10 -15) 254 138 133 237 104 125 415 119 136 151 137
	45.686	5.270	
	30.702	4.691	
	25.992	4.277	
	45.686	5.270	
	54.302	4.695	
	30.089	4.615	
	28.404	4.695	
	45.686	5.270	
	24.448	4.270	
	26.743	4.695	
	64.600	6.435	
	25.063	4.785	
	27.444	4.990	
	28.321	5.340	
	29.235	4.695	
4-bit Multiplier proposed work3 4-bit Multiplier proposed work4 4-bit Multiplier proposed work5	26.194	4.690	122 136
	28.475	4.785	149
	29.586	5.055	

Braun Multiplier High V T (High Threshold voltage) Table.3

Proposed	Power(µw)	delay(ns)	Power Delay
4-bit Multipliers			Product femito(10 -15)
2011 IEEE paper	45.686	5.270	237
4-bit Multiplier proposed work1	26.553	4.695	124

Figure 7: Table . 1

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