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Design of Low Power 4-Bit CMOS Braun Multiplier based on Threshold Voltage Techniques

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I. Introduction

In order to achieve the high speed and low power demand in DSP applications Braun's multiplier are broadly used. The Braun's multiplier is generally called as the Carry Save Array Multiplier. The architecture of a Braun's multiplier consists of AND gates and full adders. The prolific growth in semiconductor device industry has been Indicates to the high performance portable systems with enhanced reliability in data transmission. In order to maintain the high performance fidelity applications, emphasis will be on incorporation of low power modules in future system design [1-5]. The design of such modules power consumption or dissipation in fundamental arithmetic computation units such as adders and multipliers. This implies a need to design low power multipliers towards the development of efficient power & high-performance systems. The selection of the most efficient implemented multiplication has continually challenge DSP system designers [6-7]. Every system designer offers a wide range of tradeoffs in terms of speed, complexity and power consumption. Input sequences to the multiplier can be fed in parallel, serial or a hybrid (parallel serial) this proposal approaches gives high processing speed. Usually Parallel multipliers are adopted at the expense of high area complexity.

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Multiple parallel multiplications Algorithms (architectures) [8] have been proposed to reduce the chip area increase the speed of the multipliers' and reduce the power dissipation using various techniques. Several of these techniques reduce the power dissipation by eliminating spurious transitions in the circuit [9,11].

II. Proposed Work

A full adder has been designed with 10 MOS Transistors for the implementation of logic expression of Eq. (1) & Eq. (2). The 1-bit full adder circuit consists of three modules, XNOR-I, XNOR-II, and MUX. The XNOR-I and XNOR-II modules are designed using 4 MOS transistors considering two inputs and one output, and MUX module is designed with two MOS transistors for optimum operation. The implementations of full adders are shown in Fig .1 to Fig.4 the XNOR and XOR logic is combined with 6 MOS transistors and MUX logic with 2 MOS transistors for optimum operation. The implementation of full adder with 10 MOS transistors is shown in Fig.5 Full Adders propose were is presented in the reference paper [10]

$$Sum = \left(A \bar{\oplus} B\right) C_{in} + \left(A \oplus B\right) \bar{C}_{in} \quad (1)$$

$$C_{out} = \left(A \oplus B\right) C_{in} + \left(A \bar{\oplus} B\right) A \quad (2)$$

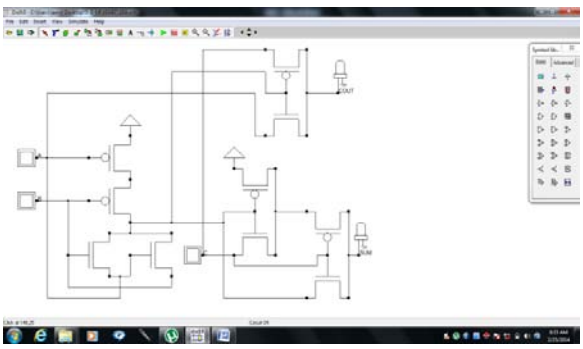

Fig. 1 : Full adder proposed work 1

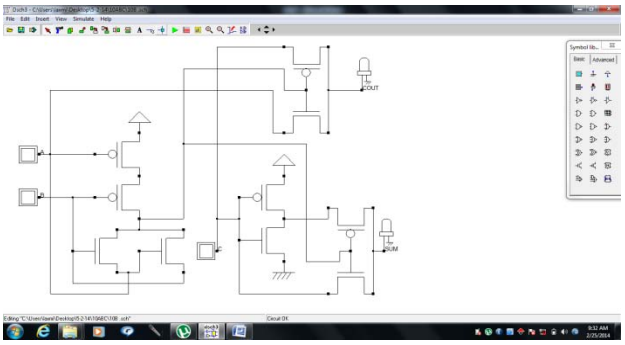

Fig. 2 : Full adder proposed work 2

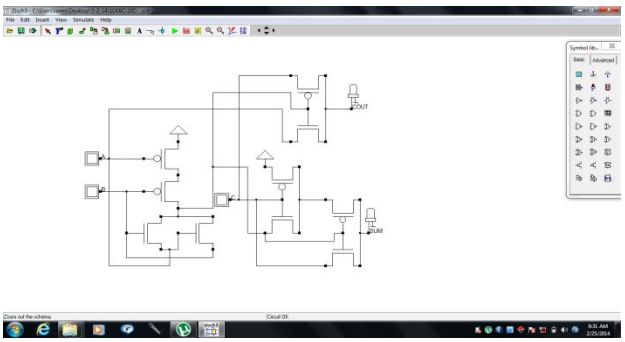

Fig. 3 : Full adder proposed work 3

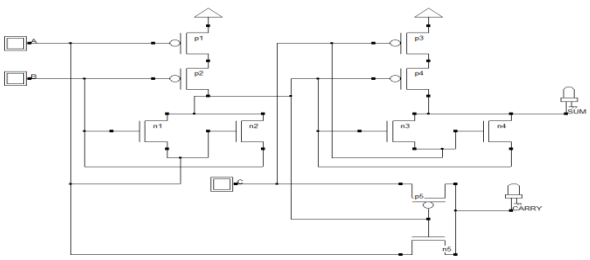

Fig. 4 : Full adder proposed work 4

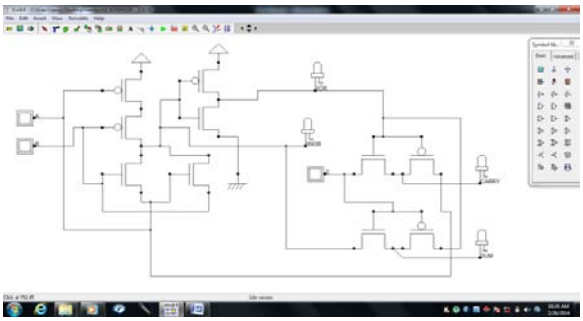

Fig. 5 : Full adder proposed work 5

a) Braun Multiplier

Consider the multiplication two un-signed 4- bit numbers

A= a3, a2, a1, a0

Multiplier is given by

B=b3, b2, b1, b0

Then product will be

P=p7, p6, p5, p4, p3p2, p1, p0

A			a3	a2	a1	a0	
	B x			b3	b2	b1	b0
				. a3b0	a2bo	a1b0	a0b0
			. a3b1	a2b1	a1b1	a0b1	
		. a3b2	a2b2	a1b2	a0b2		
	.a3b3	a2b3	a1b3	a0b3			
P7	p6	p5	p4	p3	p2	p1	p0

This simplest parallel multiplier is the Braun array. All the partial products are computed in Parallel, then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. Note that this multiplier is only suited for positive operands. The structure of the Braun algorithm for the unsigned binary multiplication is shown in Fig.6

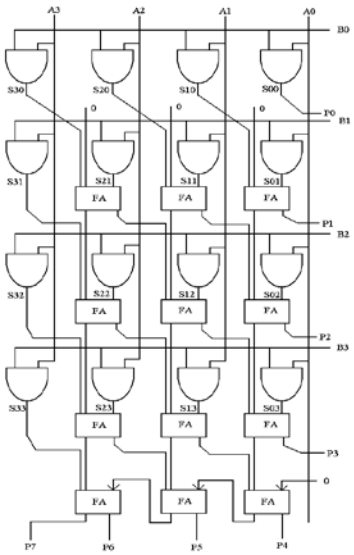

Fig. 6 : 4-Bit CMOS Braun multiplier Block Diagram

III. Performance and Simulation Results

Technology 90nm, Normal Threshold voltage =0.5v, High Threshold voltage=0.8v, Low threshold voltage=0.3v, VDD=1.2v.

Proposed work is implemented with the 210 MOS transistors parameters like power, area, Power Delay Product are compared with the reference paper

[11].proposed results are matched with the reference paper. The architecture is optimized to less MOS Transistors compared to reference paper [11]. Where same architecture is implemented with 222 MOS Transistors The architecture consists the 15 AND gates and 12 Full Adders which is shown in the above Fig.6. The product Boolean equation is shown in below .Where A_0 to A_3 and B_0 to B_3 are inputs and p_1 to p_7 are product of outputs.

$S_0=(A_1B_0).(A_0B_1)$, $S_1=(A_1B_1)$ XOR (A_1B_0), $S_2=(A_2B_0).(A_1B_1)$, $S3=(A_2B_1)$ XOR (A_3B_0), $S_4=(B_0A_3).(A_2B_1)$
$S_5=(A_0B_2).S_0+(A_0B_2).S_1+(S_0)(S_1)$, $S_6=(S_2)$ XOR (S_3) XOR (A_1B_2), $S_7=S_3.S_2+(A_1B_2).S_3+(A_1B_2).S_2$
$S_8=(A_2B_2)$ XOR(B_1A_3) XOR(S_4), $S_9=S_4.(A_2B_2)+S_4.(A_2B_1)+(A_2B_2)(A_3B_1)$, $S_{10}=S_5.S_6+S_5.(A_0B_3)+(A_0B_3).S_6$
$S_{11}=(A_1B_3)$ XOR S_7 XOR S_8, $S_{12}=(A_1B_3).S_7+S_7.S_8+S_8.(A_1B_3)$, $S_{13}=(A_1B_3)$
$S_{14}=(A_2B_3).S_9+(S_9)(B_2A_3)+(A_2B_3)(B_2A_3)$, $S_{15}=S_{11}.S_{10}$, $S_{16}=S_{13}.S_{12}+S_{13}.S_{15}+S_{12}.S_{15}$
$P_0=A_0B_0$ ---------- (1)
$P1=(A_0B_1)$ XOR (A_1B_0) ---------- (2)
$P2=(A_0B_2)$ XOR (S_0) XOR (S_1) ---------- (3)
$P_3=(A_0B_3)$ XOR $(S5)$ XOR (S_6) ---------- (4)
$P_4=S_{10}$ XOR S_1 ---------- (5)
$P_5=S_{15}$ XOR S_{12} XOR S_{13} ---------- (6)
$P_6=S_{16}$ XOR S_{14} XOR (A_3B_3) ---------- (7)
$P_7=(A_3B_3).S_{14}+S_{14}.S_{16}+S_{16}.(A_3B_3)$ ---------- (8)

Braun Multiplier Normal V_T (Normal threshold voltage) Table.1

Proposed 4-bit Multipliers	Power(μw)	Delay(ns)	Power Delay Product femito(10^{-15})	Area (μm^2)
2011 IEEE Reference paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	54.302	4.695	254	5712
4-bit Multiplier proposed work2	30.089	4.615	138	5456
4-bit Multiplier proposed work3	28.404	4.695	133	5910
4-bit Multiplier proposed work4	25.063	4.785	119	5661
4-bit Multiplier proposed work5	27.444	4.990	136	5700

Braun Multiplier Low V_T (Low threshold voltage) Table.2

Proposed 4x4 Multipliers	Power(μw)	delay(ns)	Power Delay Product femito(10^{-15})	Area (μm^2)
2011 IEEE paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	30.702	4.691	144	5354
4-bit Multiplier proposed work2	25.992	4.277	111	5654
4-bit Multiplier proposed work3	26.194	4.690	122	5504
4-bit Multiplier proposed work4	28.475	4.785	136	5500
4-bit Multiplier proposed work5	29.586	5.055	149	57.26

Braun Multiplier High V_T (High Threshold voltage) Table.3

Proposed 4-bit Multipliers	Power(μw)	delay(ns)	Power Delay Product femito(10^{-15})	Area (μm^2)
2011 IEEE paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	26.553	4.695	124	5530

4-bit Multiplier proposed work2	60.055	4.270	256	5534
4-bit Multiplier proposed work3	25.594	4.695	120	5516
4-bit Multiplier proposed work4	74.600	6.860	511	5660
4-bit Multiplier proposed work5	24.524	6.025	147	5752

Braun Multiplier Low V_T (Low Threshold voltage) & High V_T (High Threshold voltage) Table.4

Proposed 4-bit Multipliers	Power(μw)	delay(ns)	Power Delay Product femito (10^{-15})	Area (μm^2)
2011 IEEE paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	24.448	4.270	104	5524
4-bit Multiplier proposed work2	26.743	4.695	125	5918
4-bit Multiplier proposed work3	64.600	6.435	415	5706
4-bit Multiplier proposed work4	28.321	5.340	151	5959
4-bit Multiplier proposed work5	29.235	4.695	137	5736

The architecture is simulated with the cadence micro wind software. As shown in the above Table.1. The proposed work of the MOS transistors with normal threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work4 Power Delay Product 119 femito (10^{-15}), with Reference paper [11], it is observed that 46% of power Delay Product has been reduced.

As shown in the above Table.2. The proposed work of the MOS transistors with low threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work2 we got Power Delay Product 111 femito (10^{-15}), but comparatively to the Reference paper [11], it is 51% of power Delay Product has been reduced.

As shown in the above Table.3. The proposed work of the MOS transistors with high threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work1 Power Delay Product 120 femito (10^{-15}), with Reference paper [11], it is observed that 47% of power Delay Product has been reduced.

As shown in the above Table.4. The proposed work of the MOS transistors with low threshold voltage was used at critical path and high threshold voltage at non critical path. It is observed that 4-bit Braun multiplier using proposed Work1 Power Delay Product 104 femito (10^{-15}), with Reference paper [11], it is observed that 56% of power Delay Product has been reduced. Simulation results are using Micro wind Tool.

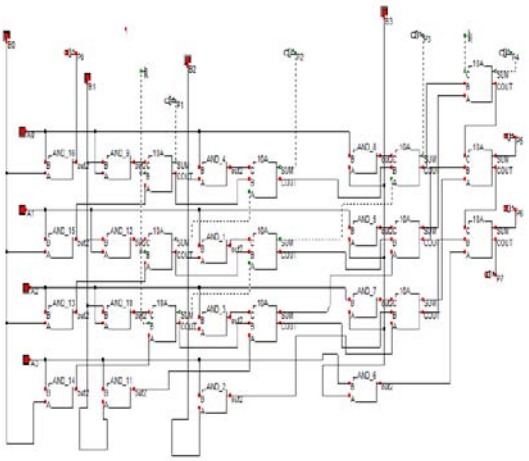

Figure 7 : Braun 4-Bit Multiplier using Micro wind Tool

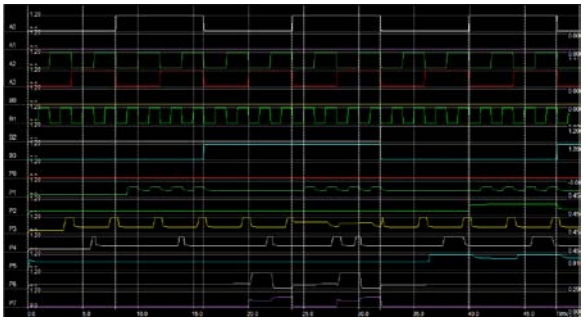

Figure 8 : 4-Bit CMOS Braun Multiplier Reference paper simulation result

IV. Conclusion

The present paper demonstrated the improvement in parameters v/s, Area, power, and delay with reduction in number of transistors to implement Full adder circuits. The simulations were performed using 90nm Micro wind 3 CMOS layout CAD Tool In this paper power consumption & Power Delay Product is calculated the results are optimized power consumption of 46% and Power Delay Product is 56 % still the performance of 4-Bit CMOS Braun Multiplier is improved by incorporating techniques which support reduced transistor implementations.

References Références Referencias

1. M.J.Liao, C.F. Su, C.Y. Chang, and A.C.H.Wu, A carry-selectadder optimization technique for high-performance booth-encoded wallace-tree multipliers. *IEEE International Symposium on Circuits and Systems ISCAS* (2002), pp.I-81–I-84.
2. K.Z.Pekmestzi, Multiplexer-based array 9. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, (Eds.), *Digital Integrated Circuits*, Prentice Hall Publications (2003).
3. M. C. Wen, S. J. Wang and Y. M. Lin, "Low power parallel multiplier with column bypassing," IEEE International Symposium on Circuits and Systems, 2005.
4. J. Ohban, V. G. Moshnyaga, K. Inoue, "Multiplier energy reduction through Bypassing of partial products", IEEE Asia-Pacific Conference on Circuits and Systems.
5. J. T. Yan, Z. W. Chen, "Low-power multiplier design with row and column bypassing," IEEE International SOC Conference, pp. 227-230, 2009.
6. G. N. Sung, Y. J. Ciou, C. C. Wang, "A power aware 2-dimensional bypassing multiplier using cell – based design flow", IEEE International Symposium on Circuits and Systems, 2008.
7. Muhammad H. Rais, "Hardware Implementation of Truncated Multipliers Using Spartan-3AN, Virtex-4 and Virtex-5 FPGA Devices", Am. J. Engg. & Applied Sci., 2010.
8. R. Anitha, V. Bagyaveereswaran, "Braun's Multiplier Implementation using FPGA with Bypassing Techniques", International Journal of VLSI Design and Communication Systems (VLSICS) Vol. 2, No. 3, September, 2011.
9. S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multi-threshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.
10. D. Lakshmaiah, Dr. M. v. Subramanyam, Dr. k. Satya Prasad design of Low power 1 bit ALU, IJETS, Volume 6, 2014.
11. Deepa Sinha, Tripti Sharma, K. G. Sharma, Prof. B. P. Singh Design and analysis of low power 1- bit full adder cell volume 6IEEE paper 2011.