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Implementation and Experimental Validation of a Real-Time Discontinuous PWM Technique for VSI Fed IM Drives

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Received: 11 December 2013 Accepted: 3 January 2014 Published: 15 January 2014

Abstract

Adjustable speed drive system requires variable voltage and frequency supply which is invariably obtained from a three-phase voltage source inverter (VSI). A number of Pulse Width Modulation (PWM) schemes are used to obtain variable voltage and frequency supply from an inverter. The most widely used PWM schemes for a three-phase VSI are carrier-based sinusoidal PWM and space vector PWM (SVPWM). This paper develops discontinuous PWM (DPWM) techniques for a voltage source inverter (VSI). Performance is evaluated in terms of total harmonic distortion (THD) in the output phase voltages. A significant reduction in switching losses is observed by adopting the proposed PWM schemes. The simulation and experimental results are provided to validate the concept.

Index terms— space vector, PWM, voltage source inverter, discontinuous PWM.

1 Introduction

hree phase DC/AC Voltage Source Inverters (VSI's) are now used extensively in motor drives, active filters and unified power flow controllers in power systems and uninterrupted power supplies to generate controllable frequency and AC voltage magnitudes using various pulse-width modulation (PWM) strategies. Of the possible PWM methods, the carrier-based PWM is very popular due to its simplicity of implementation, defined harmonic waveform characteristics and low harmonic distortion. Two main implementation techniques exist for PWM: the direct digital method and the sine-triangle intersection scheme. In the traditional sine-triangle intersection PWM (SPWM) technique, three reference modulation signals are compared with a triangular carrier signal and the intersections define the switching instants of the controllable devices. PWM strategies are required for switching the devices in a VSI appropriately to generate variable voltage, variable frequency, 3-phase AC required for the variable speed induction motor drive. The performance of the drive strongly depends on the Pulse width Modulation (PWM) technique employed. At high power levels, the inverter distortion is quite high. Hence, PWM strategies for high-power drives must aim in reducing the inverter switching losses, harmonic distortion, subject to low switching frequencies of the inverter.

This zero sequence waveform is used to alter the duty cycle of the inverter switches. Adding the same zero sequence waveform to each of the three reference phase voltages does not change the inverter output lineline voltage per carrier cycle average value; however, if the waveform is properly selected, one can achieve any of the followings: switching losses can be drastically reduced, the waveform quality may be improved, the linear modulation range can be extended, and common mode voltage of motor drives can also be drastically diminished. These potentials have been explored leading to investigations into and determination of various zero sequence waveforms, resulting in a large number of published carrier-based PWM methods. When the augmenting zero sequence waveform is continuous, the continuous PWM (CPWM) scheme is produced; however when the zero sequence signal is discontinuous with a potential for the modulator to have phase segments clamped either to the positive or negative rails, the scheme is called the discontinuous PWM (DPWM).

The zero-voltage injection has been fully exploited but to different purposes: adding a zerovoltage sequence can serve not only to linearity extension, but also to reducing switching losses. In order to reduce switching losses

the simplest method is not to switch: the idea was possible using zero-voltage sequences that saturate one of the modulation wave of the three phases.

There are about six variations reported in the literature under the name Discontinuous Pulse Width Modulation (DPWM) viz., DPWM0, DPMW1, DPWM2, DPWM3, DPWMMAX and DPWMMIN. The basic idea behind all these variations are employing discontinuous modulating signal instead of basic sinusoidal signal while carrier remains the triangular function. DPWM modulation techniques have the advantage of eliminating one switching transition in each half carrier interval, which allows the switching frequency to increase by a nominal value of 3/2 accordingly for the same inverter losses. This may improve the harmonic performance of the inverter by virtue of the reduced The proposed carrier-based non-sinusoidal and discontinuous modulation schemes are experimentally implemented with an TMS320F2812 DSP Processor, intelligent power modules and used to modulate a threephase inverter feeding a three-phase induction machine.

2 Principle of Dpwm and its Variants a) 120 o Discontinuous Modulation

In this type of modulation, each phase leg in turn is now continuously locked to the upper or lower DC rail (whichever is chosen) for one-third of the fundamental cycle (120°).DPWMMAX and DPWMMIN strategies come under this category. In DPWMMAX, each phase around the peak is locked to the upper DC rail for one-third of the fundamental cycle (120 o) as shown in Figure 1(a) and hence the name. Each phase in DPWMMIN, is locked to the lower DC rail for one-third of the fundamental cycle (120 o) as shown in the Figure 1(b).Due to the asymmetry in line-to-line voltage , it has been expected that the harmonic performance of 120°d iscontinuous PWM will be suboptimal compared to continuous modulation strategies. However, it has been identified that to maintain the same effective phase leg switching frequency as for continuous modulation, the space vector calculation frequency (i.e. twice the carrier frequency) should be increased by approximately 50%, since each phase leg only switches during two-thirds of each fundamental cycle. It is trade-off between these two effects that offers potential advantages for 120°d iscontinuous PWM under some modulation conditions. A further limitation with this strategy is that one device of each phase leg is always turned off during its 120°u nmodulated region, while the other device is always conducting. Hence conduction losses are not shared equally across the two devices in each phase leg. Another improved discontinuous modulation strategy in which each phase leg is now unmodulated for only 60° at a time (alternately switched to the upper or to the lower DC rail).It has the particular benefit that the line-to-line switched voltages are symmetrical. This type of discontinuous switching pattern is termed as DPWM1 and centers the non-switching periods for each phase leg symmetrically around the positive and negative peaks of its fundamental reference voltage. This is the best position for resistive load, since the peaks of the line currents follow the peaks of the fundamental voltages. Therefore each phase leg does not switch just when the current is at its maximum value, and this obviously minimizes switching losses. The modulating waveform for DPWM1 is as shown in the Figure 2 It is viable to place each 60 ? non-switching period anywhere within the 120 ? region where the appropriate phase leg reference voltage is the maximum/minimum of the three-phase set. For example, the 60 ? "clamp to + dc V "non switching period for phase leg 'a' can be placed anywhere in the region This freedom allows alternative 60 ? discontinuous PWM strategies to be considered which minimize the switching losses for loads which are not unity power factor.

For a lagging power factor (pf) load, it is clearly preferable to retard the non-switching period by up to a maximum of 30 ? (pf of 0.866 lag), depending on the load current power factor. This is the discontinuous modulation strategy DPWM2 and its modulating waveform is as shown in figure 2(ii).For a leading power factor load, the non switching period can be advanced by up to 30 ? (pf of 0.866 lead).This is discontinuous modulation strategy DPWM0 and its modulating waveform is shown in Figure 3 In DPWM, the modulating signal is discontinuous in nature comprised of different functions for each section of time reference. There are six functions which are substituted in various sections of time reference. The differences among the DPWM schemes are just interchange of these sections. Table 1, 2, 3, 4, 5 and 6 details the expressions for the modulation waves of various DPWM variants for one complete cycle.

In all the cases, it has been understood that the phase leg reference segments are in fact sections of the required line-to-line voltage, referenced to the phase leg which is clamped to either the upper or the lower DC rail. The variation of M does not have any effect in the saturation region of the modulating wave.

3 Performance Evaluation

Parameters that is taken in consideration for performance evaluation of the proposed DPWM methods namely Total Harmonic Distortion (THD) is defined in by equations (**??**), (1) Where V n represents n th order harmonic component and V 1 represent fundamental output phase voltages. The lowest order harmonic contents (upto 25 th order) are considered for calculation of THD. The resulting THD are shown in Figure 4. Their measured %THDs is compared (Table **??** It is seen from that at low modulation index the THD of DPWMMAX is lowest compared to all other schemes and DPWM1 has highest THD. Since the DPWMMAX may not be employed for implementation purposes, thus the next best scheme is DPWM2. At high modulation index the value of THD is smaller compared to the value at lower modulation index, which implies that the output voltage is very near to

the sinusoidal. DPWM1 has the lowest THD and DPWM0 and DPWM3 has highest THD at high modulation index. iv.

4 Experimental Results

The proposed DPWM techniques has been implemented in real time using Texas Instrument TMS320F2812 DSP Processor, intelligent power modules and was programmed through the software Vissim. The DSP board is integrated interfacing communication board. The PC is connected to the DSP board through printer parallel port.

The DSP board is connected through cable to the Inverter intelligent power modules. Current sensors are used for feedback purposes. The code is run using Code Composer studio CCS 3.2V, and the .out file thus created is then converted to the ASCII file which is loaded to the DSP for further processing. The complete experimental set up is illustrated in Figure 5

5 Conclusions

The paper present PWM technique termed as Discontinuous PWM for voltage source inverter. This [1]

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Figure 1: Figure 1 :

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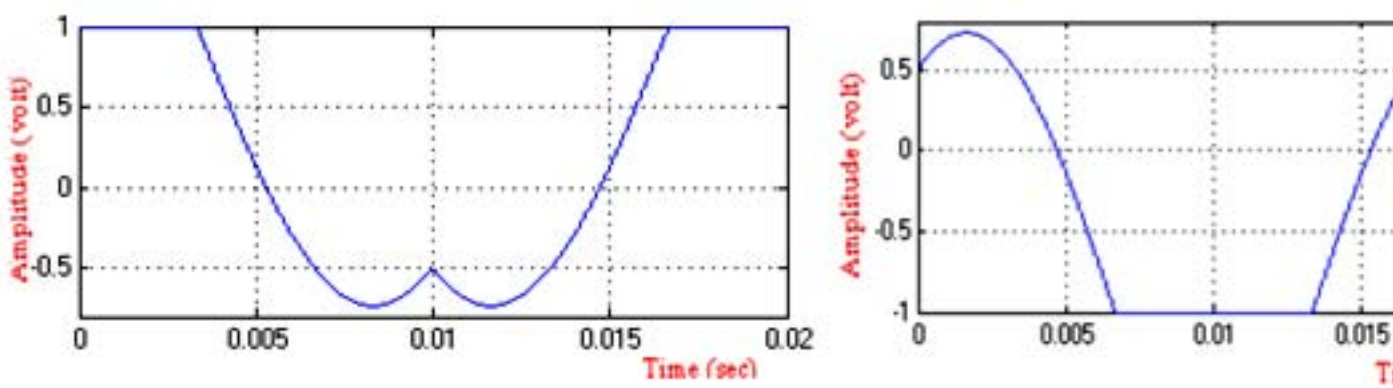

Figure 2:

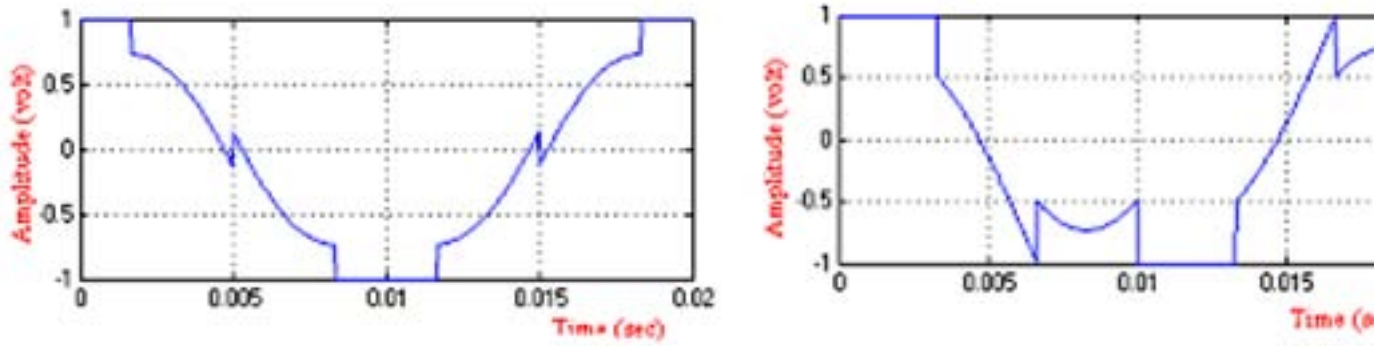

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Figure 3: Figure 2 :

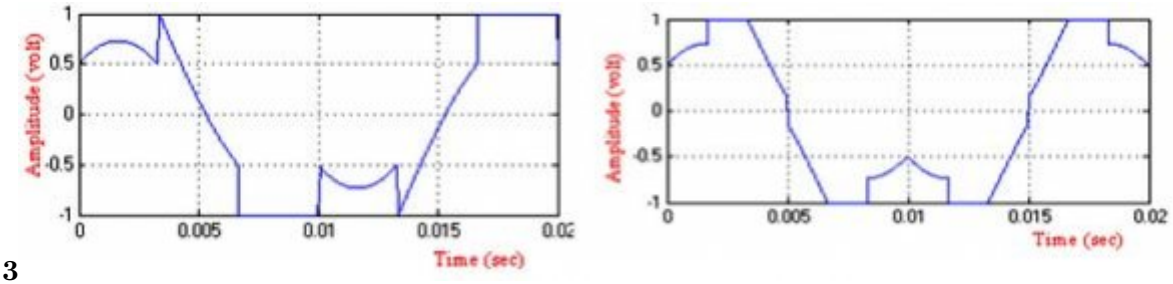

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Figure 4: 3 â??”

$$\text{THD} = \sqrt{\sum_{n=3,5,7..}^{\infty} \left(\frac{V_n}{V_1}\right)^2}$$

Figure 5:

			I[A]	Hdf[%]	Or.	I[A]	Hdf[%]
PLL	U1		0.329	----------	dc	-0.078	-23.83
Freq	30.01 Hz	1	0.276	83.97	2	0.125	38.06
		3	0.014	4.21	4	0.029	8.74
U1	0.0714kV	5	0.034	10.28	6	0.017	5.07
I1	0.329 A	7	0.009	2.67	8	0.025	7.60
P1	0.020kW	9	0.013	3.96	10	0.004	1.08
S1	0.021kVA	11	0.002	0.47	12	0.014	4.11
Q1	0.006kvar	13	0.007	2.13	14	0.007	2.21
λ1	0.9536	15	0.013	4.02	16	0.003	1.00
ϕ1	17.52 °	17	0.016	4.71	18	0.015	4.44
Uthd1	20 .07 %	19	0.003	0.99	20	0.007	2.22

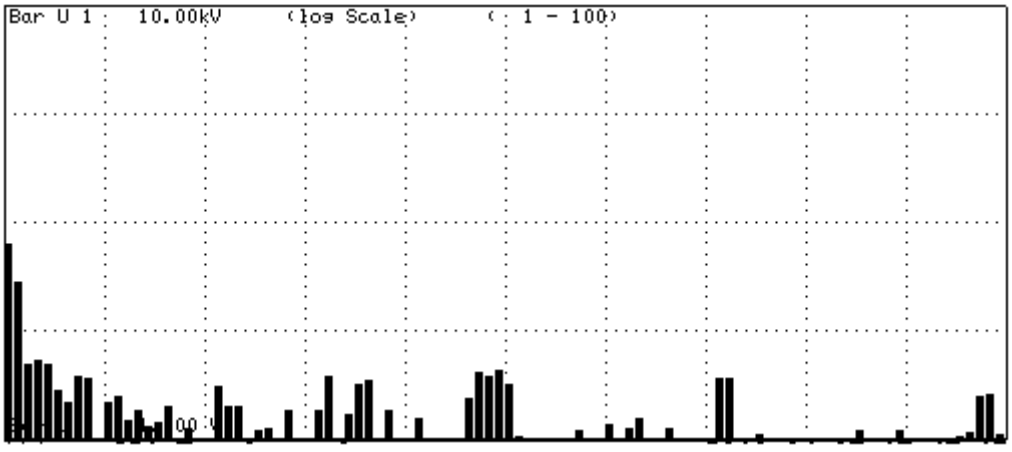

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Figure 6: Figure 3 :

			I[A]	Hdf[%]	Or.	I[A]	Hdf[%]
PLL	U1		0.190	---------	dc	0.118	61.97
Freq	30 Hz	1	0.060	31.36	2	0.071	37.09
		3	0.040	21.13	4	0.037	19.57
U1	0.0529kV	5	0.022	11.62	6	0.041	21.55
I1	0.190 A	7	0.021	11.22	8	0.013	6.66
P1	0.007kW	9	0.008	4.12	10	0.030	15.85
S1	0.007kVA	11	0.024	12.45	12	0.005	2.78
Q1	-0.002kvar	13	0.014	7.59	14	0.011	5.67
λ1	0.9739	15	0.006	2.93	16	0.017	8.98
ϕ1	346.87 °	17	0.005	2.73	18	0.007	3.75
Uthd1	20.10 %	19	0.003	1.59	20	0.013	6.88

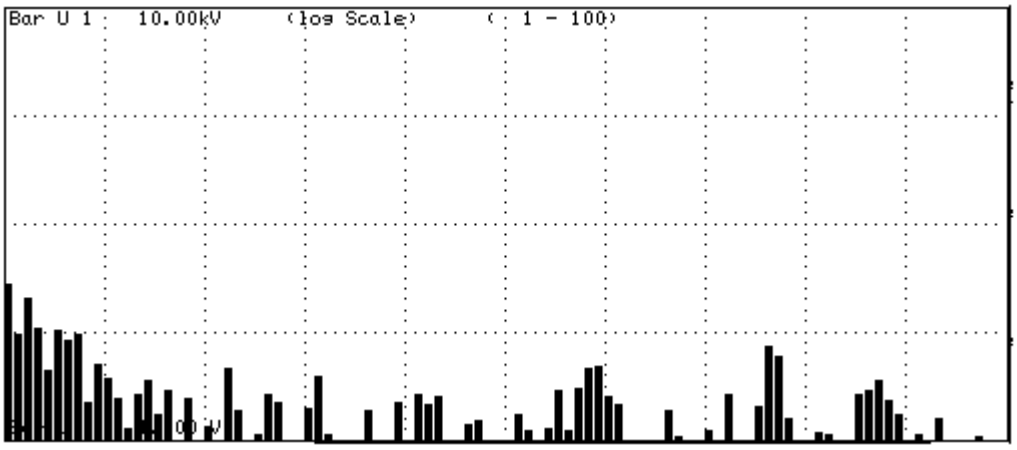

Figure 7: ?

		Or.	I[A]	Hdf[%]	Or.	I[A]	Hdf[%]
PLL	U1		0.246	---------	dc	0.042	17.17
Freq	29.995 Hz	1	0.016	6.54	2	0.175	71.05
		3	0.089	36.36	4	0.006	2.26
U1	0.0553kV	5	0.053	21.60	6	0.055	22.55
I1	0.246 A	7	0.029	11.88	8	0.025	10.27
P1	0.010kW	9	0.028	11.32	10	0.019	7.82
S1	0.010kVA	11	0.023	9.16	12	0.014	5.70
Q1	-0.003kvar	13	0.022	8.85	14	0.034	13.67
λ1	0.9512	15	0.039	15.79	16	0.010	3.95
φ1	342.03 °	17	0.011	4.51	18	0.007	2.66
Uthd1	11.07 %	19	0.013	5.35	20	0.011	4.66

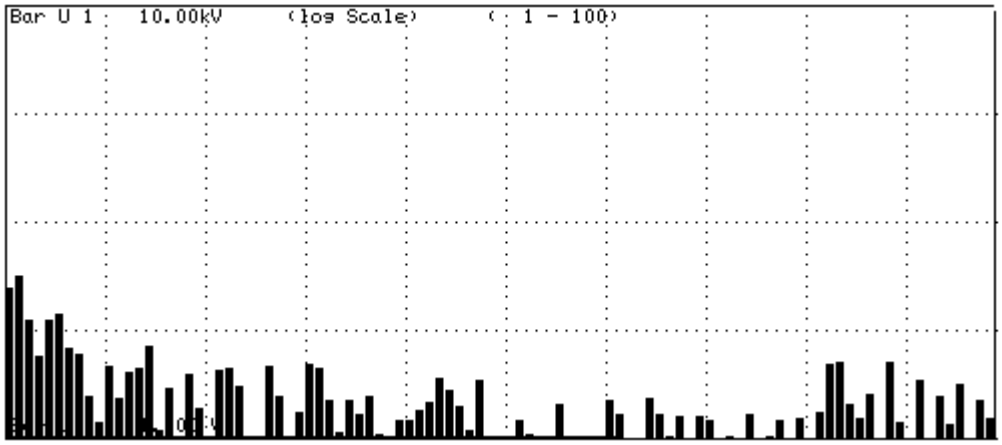

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Figure 8: 6 - 1 - 1 - 3 * 4 2014 Table 6 :

			I[A]	Hdf[%]	Or.	I[A]	Hdf[%]
PLL	U1		0.190	---------	dc	0.068	35.50
Freq	30 Hz	1	0.145	76.10	2	0.041	21.43
		3	0.030	15.98	4	0.008	4.34
U1	0.0426kV	5	0.011	5.70	6	0.022	11.53
I1	0.190 A	7	0.018	9.52	8	0.015	8.00
P1	0.006kW	9	0.011	5.72	10	0.005	2.74
S1	0.006kVA	11	0.036	18.69	12	0.036	18.86
Q1	0.003kvar	13	0.007	3.91	14	0.005	2.47
λ1	0.8972	15	0.008	4.43	16	0.016	8.38
ϕ1	26.20 °	17	0.016	8.17	18	0.010	5.39
Uthd1	11.31 %	19	0.006	3.36	20	0.020	10.46

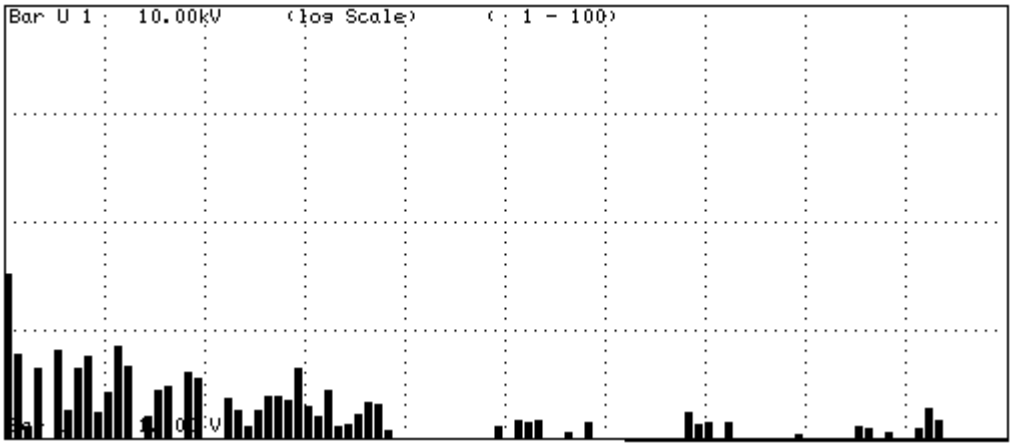

Figure 9:

			I[A]	Hdf[%]	Or.	I[A]	Hdf[%]
PLL	U1		0.402	---------	dc	0.376	93.49
Freq	30 Hz	1	0.075	18.59	2	0.043	10.57
		3	0.058	14.29	4	0.011	2.69
U1	0.0811kV	5	0.042	10.35	6	0.011	2.66
I1	0.402 A	7	0.030	7.50	8	0.004	1.10
P1	0.030kW	9	0.012	2.90	10	0.003	0.71
S1	0.030kVA	11	0.009	2.23	12	0.016	3.88
Q1	-0.001kvar	13	0.016	3.94	14	0.013	3.12
λ1	0.9989	15	0.008	1.87	16	0.015	3.74
ϕ1	357.30 °	17	0.004	0.90	18	0.008	1.99
Uthd1	10.42 %	19	0.006	1.37	20	0.010	2.54

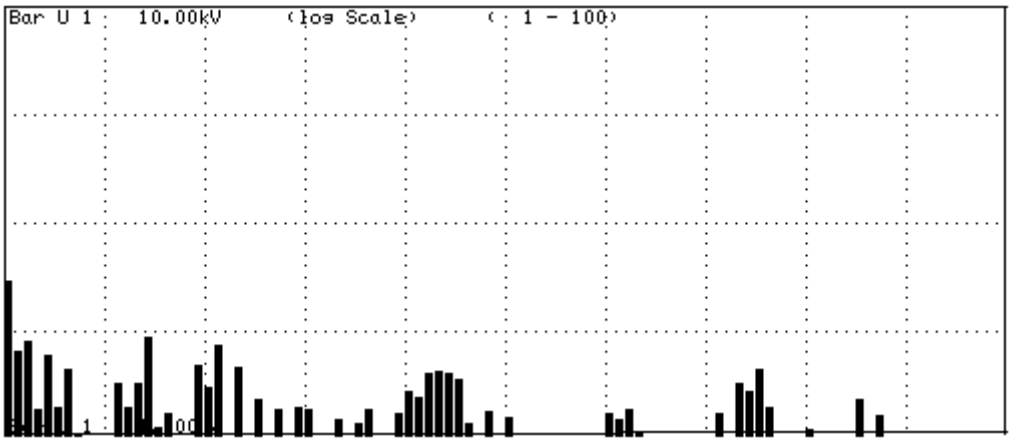

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Figure 10: Figure 4 :

			I[A]	Hdf[%]	Or.	I[A]	Hdf[%]
PLL	U1		0.711	---------	dc	-0.088	-12.42
Freq	19.68 Hz	1	0.593	83.43	2	0.331	46.63
		3	0.055	7.73	4	0.050	7.08
U1	0.0767kV	5	0.097	13.68	6	0.071	9.94
I1	0.711 A	7	0.013	1.80	8	0.024	3.37
P1	0.051kW	9	0.019	2.60	10	0.028	3.91
S1	0.053kVA	11	0.015	2.07	12	0.033	4.68
Q1	0.014kvar	13	0.014	2.01	14	0.018	2.47
λ1	0.9624	15	0.026	3.68	16	0.016	2.22
ϕ1	15.75 °	17	0.014	1.90	18	0.015	2.16
Uthd1	10.46 %	19	0.026	3.63	20	0.033	4.71

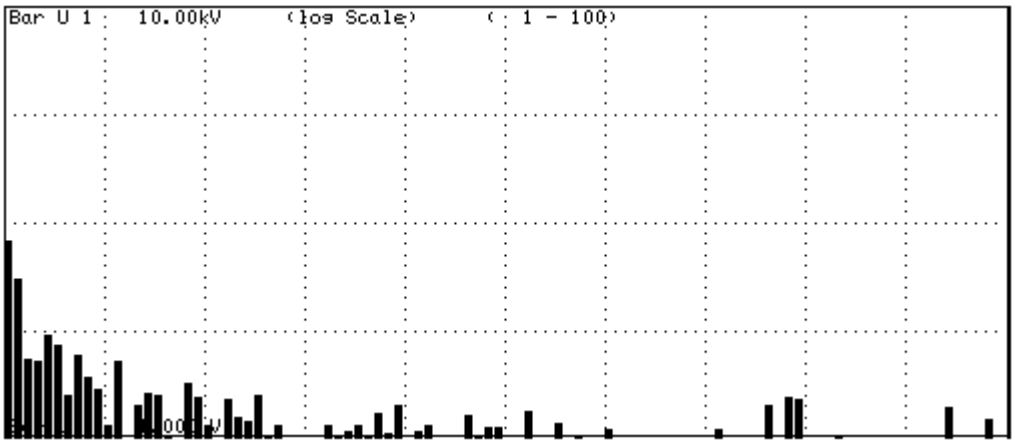

Figure 11:

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Figure 12: Figure 5 :

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Figure 13: Figure 6 :

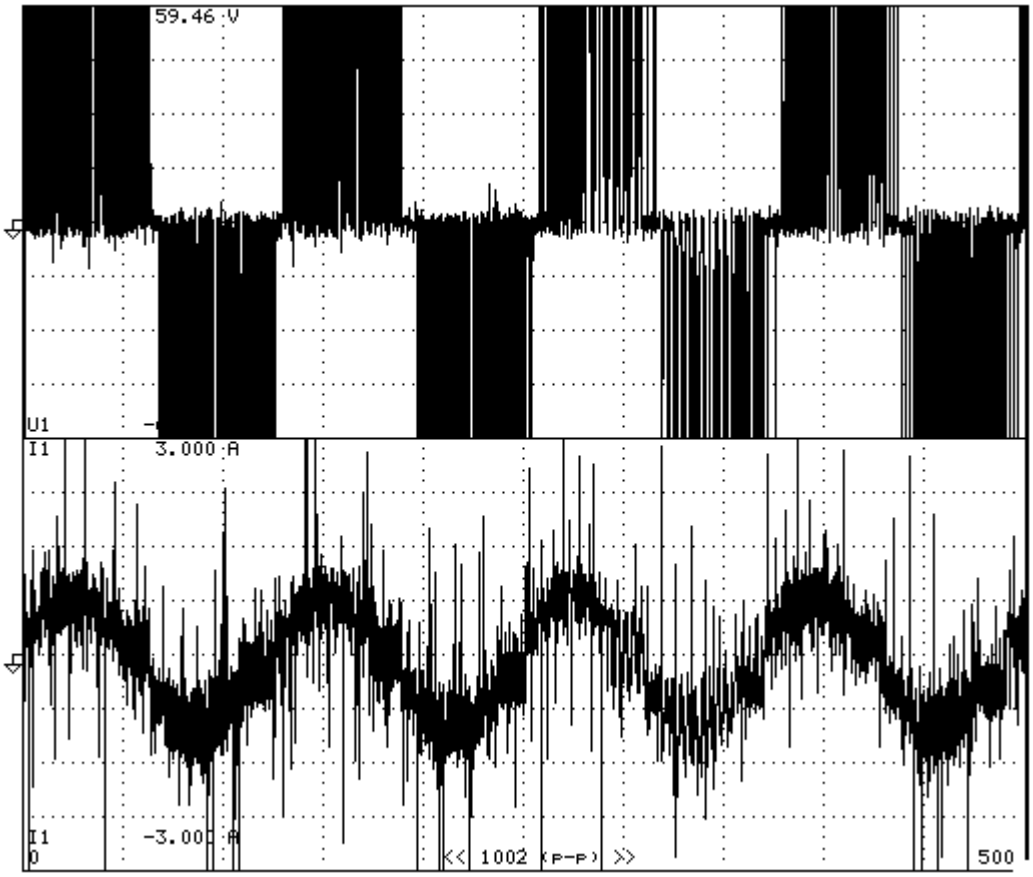

Figure 14:

1

Figure 15: Table 1 :

2

Alpha (degree)	Phase A	Phase B	Phase C
0-30 0	+1	? +1-3 * M*cos(?+) 6	5? +1+ 3 * M*cos(?+) 6

Figure 16: Table 2

3

Figure 17: Table 3 :

4

Figure 18: Table 4 :

5

Alpha (degree)	Phase A	Phase B	Phase C
0-60 0	+1	? +1-3 * M*cos(?+) 6	5? +1+ 3 * M*cos(?+) 6

Figure 19: Table 5 :

.1 v.

index DPWM1 is recommended for use. The viability of the proposed schemes is validated using simulation and experimental result

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