Global Journal of Researches in Engineering: F
Electrical and Electronics Engineering
Volume 14 Issue 7 Version 1.0 Year 2014
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Digital Frequency Synthesis using Multi-Phase NCO for Dielectric Characterization of Materials on Xilinx Zynq FPGA

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Abstract- Precise measurement of dielectric characteristics of materials is becoming necessity in several engineering applications. The dielectric constant measurement over wide frequency range for emerging applications such as PCB manufacturing, agriculture, environmental and food processing industries has several challenges. With the advancement in digital VLSI and Field Programmable Gate Array (FPGA) based processing the digital techniques for estimating the dielectric constant are feasible. In this context the digital based frequency generation techniques over wide frequency are discussed in this paper. The multi phase Numerically Controlled Oscillator (NCO) based technique for generating high frequency signals are experimented in this paper. The efficient implementation of NCO for Xilinx Zynq family FPGA, XC7Z020 device is simulated here. The realized multi phase NCO is observed to be occupying only 15% of resources and operating at 250MHz to result efficient synthesis of sine wave with sampling frequency of 1GHz. The design issues related to digital carrier generation on FPGAs, while driving high frequency Digital to Analog Converters (DACs) are discussed and simulation results are presented here.

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GJRE-F Classification : FOR Code: 290901p, 090609

Strictly as per the compliance and regulations of :

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Abstract- Precise measurement of dielectric characteristics of materials is becoming necessity in several engineering applications. The dielectric constant measurement over wide frequency range for emerging applications such as PCB manufacturing, agriculture, environmental and food processing industries has several challenges. With the advancement in digital VLSI and Field Programmable Gate Array (FPGA) based processing the digital techniques for estimating the dielectric constant are feasible. In this context the digital based frequency generation techniques over wide frequency are discussed in this paper. The multi phase Numerically Controlled Oscillator (NCO) based technique for generating high frequency signals are experimented in this paper. The efficient implementation of NCO for Xilinx Zynq family FPGA, XC7Z020 device is simulated here. The realized multi phase NCO is observed to be occupying only 15% of resources and operating at 250MHz to result efficient synthesis of sine wave with sampling frequency of 1GHz. The design issues related to digital carrier generation on FPGAs, while driving high frequency Digital to Analog Converters (DACs) are discussed and simulation results are presented here.

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I. Introduction

The dielectric properties measurement is necessary because it can provide the electrical or magnetic characteristics of the materials, which proved useful in many research and development fields [1][10]. The present work is aimed to evolve digital multi phase technique for generating high frequency sinusoid signal using FPGAs, which becomes useful in precise dielectric characterization of materials.

The work presented in this paper is part of ongoing research [1] [9] aimed for precise characterization of printed circuit board (PCB) at high frequencies (order of Hundreds of MHz). This paper discusses the multi phase NCO based technique for generating high frequency sine wave, which is required in this context.

Measurement of dielectric properties requires measurements of the complex relative permittivity (ε_r) and complex relative permeability (μ_r) of the materials [1]. The complex dielectric permittivity consists of real and imaginary parts. The real part of the complex permittivity is referred as dielectric constant and it is a measure of the amount of energy from an external electrical field stored in the material. The imaginary part is indicative of the amount of energy that gets dissipated in material when it is subjected to electric field [1]. The imaginary part is zero for lossless materials. The term loss tangent is defined as given in (1) which indicates the dissipative nature of material with respect to the energy storage nature [11].

$$\tan \alpha = \frac{\varepsilon_r''}{\varepsilon_r'} = \frac{1}{Q} \quad (1)$$

The vector diagram for loss tangent is shown in Fig.1. Loss tangent is also referred as quality factor (Q). The circuit equivalent of real and imaginary parts of permittivity can be well derived from capacitor action [1].

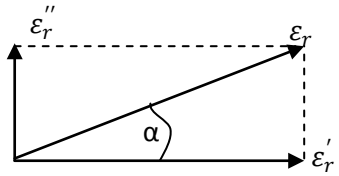

Fig 1 : Capacitor action with dielectric

The equation (2) gives capacitance value of parallel plate capacitor as function of area of the plate, distance between plates and permittivity of the medium.

$$C = \frac{\varepsilon A}{d} \quad (2)$$

Where ε is the total permittivity, which can be represented as $\varepsilon = \varepsilon_o \varepsilon_r$

The C_O can be used to represent the capacitance when only vacuum is present between the capacitor parallel plates. The equation (2) can be rewritten as given in equation (3) in terms of C_O.

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$$C = \varepsilon_r C_0 \quad (3)$$

The Fig. 2. shows simple RC circuit for measuring the dielectric constant.

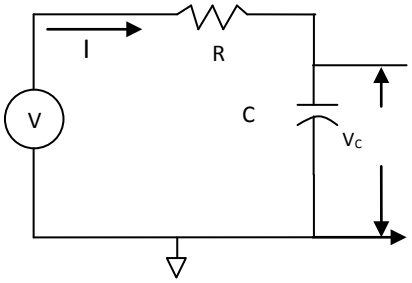

Fig. 2 : Schematic of RC circuit

The voltage across capacitor can be given as equation (4) whose phase term can be computed as in equation (5).

$$V_C = \frac{V}{1+j\omega C_0 \varepsilon_r' R} \quad (4)$$

$$\theta = -\tan^{-1}\left(\frac{1}{\omega C_0 \varepsilon_r' R}\right) \quad (5)$$

The phase shift between V and V_C is a function of dielectric constant for all remaining being constant values. The dielectric constant measurement through digital techniques is possible, if the signal with angular frequency ω can be generated digitally and the phase shift between and V and V_C is measured accurately [2]. The FPGA based techniques for sinusoid generation using NCO is an established area and being widely used in communication applications. However the maximum synthesizable signal with NCO is limited to $F_{clk}/2$, where F_{clk} is the clock at which the NCO runs.

To enable dielectric Constant measurement up to high frequencies it is required that the FPGA based circuit should be able to generate the signal up to the desired frequency. Above in equation (4) $\omega = 2\pi f$ and f=frequency at which dielectric constants are measured. In conventional implementation of NCO the realizable frequency by NCO is given in equation (6). Fig.3. describes the basic NCO architecture.

$$\text{Output sine wave frequency} = \frac{\Delta p \cdot F_{clk}}{2^N} \quad (6)$$

Where F_{clk} = clock frequency at which NCO is running

N= size of bit width phase registered

Δp = input phase increment word

Since F_{clk} and N are fixed for a particular implementation, the input phase increment word (Δp) describes the frequency of the output sine wave. The first register in the Fig.3. latches the frequency controlled word on the clock edge and the accumulator realized by added and register continuously accumulates input frequency word and generates the phase. This phase accumulator generates the digital phase, which is input to sine lookup table. The sine lookup table generates the digital amplitude samples of sine waves [3]. The digital samples of sine wave need to be supplied to DAC chip which generates corresponding analog sine wave. The analog sine wave after passing through low pass filter will be suitable for dielectric constant measurement. The low pass filter removes the spurious harmonic signals which are present in DAC output.

The present day available RF DAC [6][13] enables high frequency sine wave up to 1 GHz provided the digital part is capable of generating suitable samples. With the present day available FPGA technology the max achievable frequency F_{clock} is up to 300 MHz only which means the maximum F_o that can be generated is 150MHz only, Where as the necessity of dielectric constant measurement of PCB materials is up to few Mega Hertz to Giga Hertz frequencies.

This becomes limitation of digital based carrier generation for high frequency dielectric constant characterization of materials. The present paper implementation of multi phase NCO based architecture enables digital generation of sine wave samples [3], which can be used while interfacing with RF DACs[6][13] by which the concept of digital dielectric constant can be extended up to Hundreds of Mega Hertz to Giga Hertz frequency level.

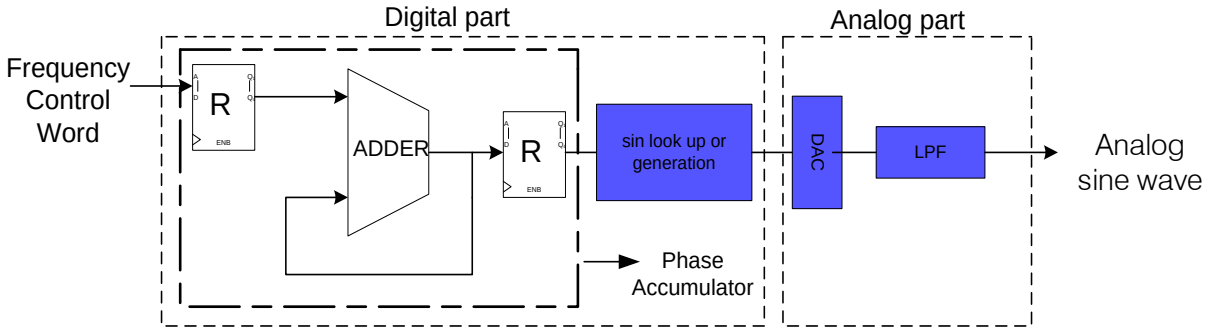

Fig. 3 : High level block diagram of NCO based SIN wave generation

The remaining part of the paper is organized into three sections. Section 2 explains the high level architecture of multiphase digital NCO. Section 3 explains the simulation and synthesis results including the resource utilization summary for ZED board. The last section provides conclusion and future scope of the work.

II. High Level Architecture

This section presents high level architecture of proposed multiphase NCO based sine wave generation [4]. Multiphase NCO technique in principal uses the inverse concept of distributed arithmetic. The distributed arithmetic (DA) principle is an area optimization technique usually implemented in FPGAs and Application Specific Integrated Circuits (ASICs), where certain hardware is made to run at high frequency than the actual throughput required. Utilizing same resource for multiple operations in different clock cycles allows achieving area optimization. For e.g. in a digital logic the requirement is to multiply numbers at 10MHz rate. The FPGA logic employing DA technique runs at 100MHz. The multiplier input is multiplexed and output is de-multiplexed to perform 10 multiplications by using single unit.

In multiphase NCO the concept is reverse implementation of resource sharing. In the present Implementation on the ZED board [12] it is aimed to generate sine wave 400 MHz by achieving sampling frequency of 1GHz.

In this implementation 4 NCO modules are made to run as parallel blocks which shall maintain phase offsets corresponding to their sample position. The sine wave generation [4] is illustrated in fig. 4. Scheme of multiphase NCO for high frequency digital The effective sampling rate achieved is denoted as F_s and is given at (7).

$$F_s = 4 \text{ X } F_{clk} \quad (7)$$

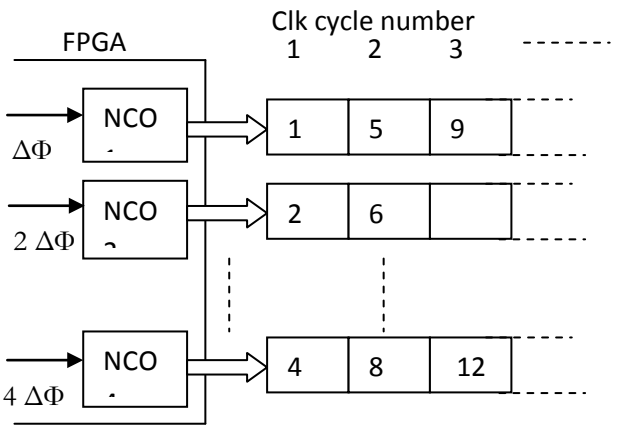

Fig. 5 : Set of 4 NCOs generating samples at F_s

The effective sampling rate achieved is denoted as F_s and is given at (7). The NCOs are fed with phase shifts such that the samples generated by all NCOs form successive samples in sine wave at higher sampling rate F_s. The figure 5 has the illustration of the same.

The initial phase shifts can be computed by a series of adders, where at each stage ΔΦ is added [6].

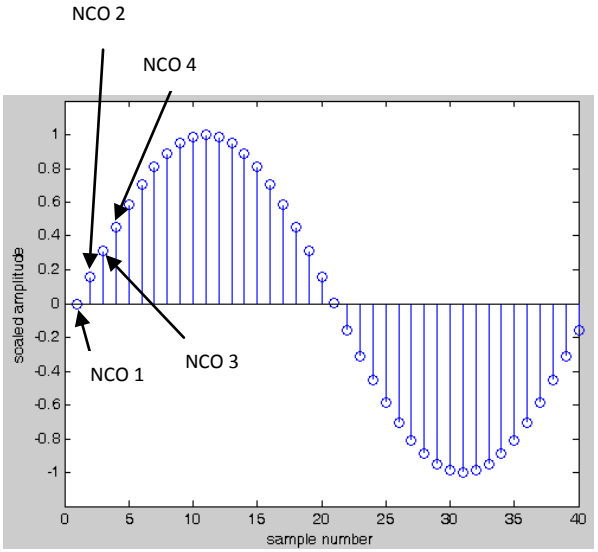

Fig. 5 : Samples generated by each NCO in the sin wave at F_s

As the uniformly sampled phase results in spurious values at the multiples of sampling frequency, the phase dithering is implemented. In the phase dithering a pseudo noise binary signal (PN) is used to produce a random number. This random numbers are added to phase accumulator output, before applying to the address inputs of SIN and COS look up tables.

III. Simulation and Synthesis Results

The simulation results for the implemented logic are given in this section. The figure (6), shows the phase outputs of each NCO. The phase shifts in each channel can be observed due to the different initial values assignment [3].

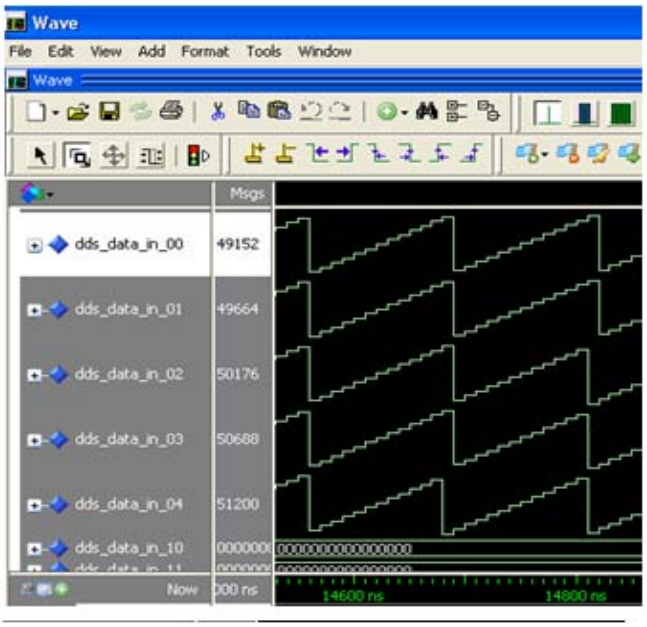

Fig. 6 : Simulation results showing phases of 4 NCOs

The simulation results showing the generated sine waves on all four channels are shown in figure 7. The resultant signal when applied to multi channel DAC is simulated by a mod 4 counter based interleaving logic, placing samples from each channel as illustrated in fig. 5. The last waveform in Fig. 7, RF_DAC_SIG shows the generated sine wave with F_s sampling rate.

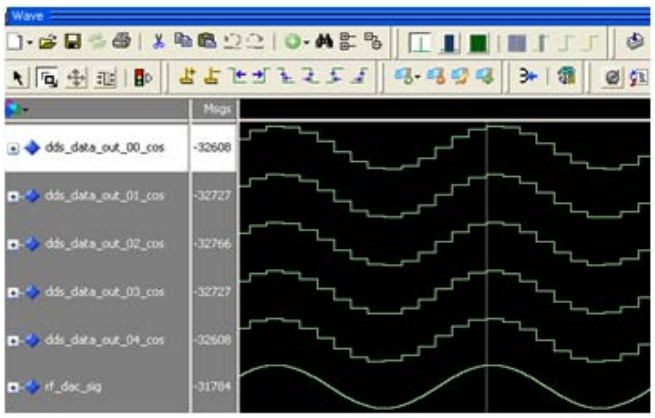

Fig. 7 : Simulation results showing sin wave samples of 4 NCOs and muxed resuling sin wave

The logic is synthesized using Xilinx's ISE 14.6 tool and the area and speed analysis are carried out. The area utilization summary and maximum clock estimate of the implemented digital logic [7] For ZED board (XC7Z020) FPGA [5], are given at fig. 8.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	333	18224	1%
Number of Slice LUTs	459	9112	5%
Number of fully used LUT-FF pairs	270	522	51%
Number of bonded IOBs	35	186	18%
Number of BUFG/BUFGCTRLs	2	16	12%

Fig. 8 : Area utilization summary

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.945ns (Maximum Frequency: 339.587MHz)
   Minimum input arrival time before clock: 3.021ns
   Maximum output required time after clock: 3.819ns
   Maximum combinational path delay: No path found
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Fig. 9 : Maximum clock utilization summary

The maximum speed reports 333 MHz, which is higher than the considered 250 MHz operation for the aimed specifications.

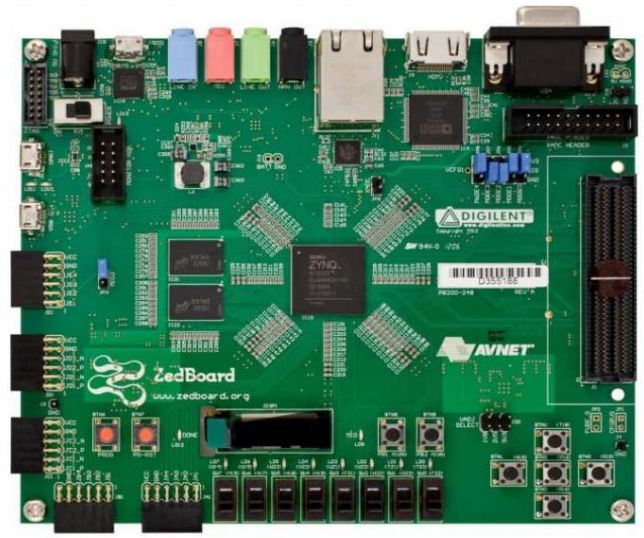

Fig. 10 : Zynq Evaluation and development board

It is aimed to continue this work with hard ware integration of Digital to analog converter from Analog devices AD9122 Tx-DAC IC [13]. Hence the data and control signal generation are ensured to meet the specification of this IC and the same are verified with Xilinx Chipscope Integrated Logic Analyzer (ILA) tool.

The figure 11, has chipscope ILA obtained results for 4 channel with the multiphase technique. Since the the AD9122 is complex DAC, similar logic is implemented for generating the quadrature tones with 90 degree phase shifts.

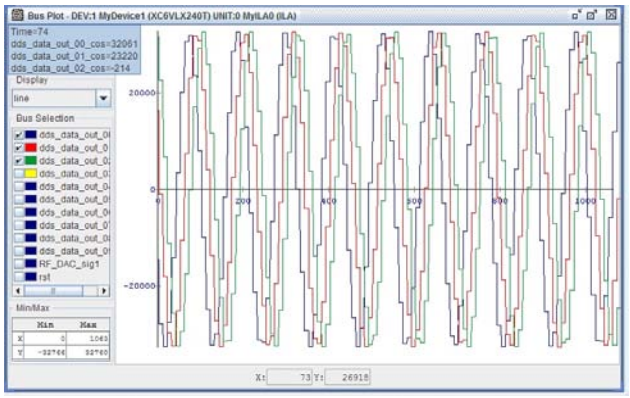

Fig. 11 : On-chip verification results with Chipscope

IV. Conclusion

The dielectric constant measurement technique with capacitance based measurement is discussed. The basic circuit and dielectric constant measurement using RC circuit principle is discussed. The need of high frequency digital signals synthesis for high frequency sin wave generation is elaborated. FPGA based techniques with multi DDS for driving RF DACs presented considering clock frequency of 250 MHz on FPGA. By employing 4 NCOs, sine wave with 1 Giga samples per second is simulated. Using Xilinx ISE tools synthesis is carried out and area utilization summary is observed. The work is aimed to continue in establishing this technique on With Xilinx Zynq FPGA and RF DAC cards for dielectric constant measurement applications.

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