Global Journal of Researches in Engineering: F
Electrical and Electronics Engineering
Volume 14 Issue 6 Version 1.0 Year 2014
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

ASIC Design, Implementation and Exploration on High Speed Parallel Multiplier

By Y. Narasimha Rao, DR. G. Samuel Vara Prasada Raju
& Penmetsa V Krishna Raja
GITAM University, India

Abstract- Designing multiplier is always a challenging and interesting job, in order to satisfy user needs as per demand. Vedic multiplier is prominent system for faster result and optimized circuit design. In any digital system the throughput and power consumption decides the performance. The present work mainly concentrated on Vedic multiplier power consumption and throughput. In much faster computing and parallel processing architectures, pipeline motivates for higher throughput. This is motivated to incorporate pipeline in the present work to enhance the performance of the Vedic multiplier. In the present paper, area and power consumption is also taken into consideration along with throughput. These parameters are compared for different fast adders such as RCA, CSLA, LFA, BKA, KGA in Vedic multiplier. The Vedic multipliers are designed and analysed using Cadense RTL Compiler v08.10.

Keywords: throughput, power consumption, area, pipeline, fast adders, vedic multiplier.

GJRE-F Classification : FOR Code: 100699

Strictly as per the compliance and regulations of :

ASIC Design, Implementation and Exploration on High Speed Parallel Multiplier

Y. Narasimha Rao [α], DR. G. Samuel Vara Prasada Raju [σ] & Penmetsa V Krishna Raja [ρ]

Abstract- Designing multiplier is always a challenging and interesting job, in order to satisfy user needs as per demand. Vedic multiplier is prominent system for faster result and optimized circuit design. In any digital system the throughput and power consumption decides the performance. The present work mainly concentrated on Vedic multiplier power consumption and throughput. In much faster computing and parallel processing architectures, pipeline motivates for higher throughput. This is motivated to incorporate pipeline in the present work to enhance the performance of the Vedic multiplier. In the present paper, area and power consumption is also taken into consideration along with throughput. These parameters are compared for different fast adders such as RCA, CSLA, LFA, BKA, KGA in Vedic multiplier. The Vedic multipliers are designed and analysed using Cadense RTL Compiler v08.10.

Keywords: throughput, power consumption, area, pipeline, fast adders, vedic multiplier.

I. Introduction

Fast adders and multiplications are ever needed in many DSP systems Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit [1].Another important area on which is required to concentrate is the power dissipation and speed. There is always an interrelation between power dissipated and speed of operation ever known to all. Vedic multiplier is famous for fast operation and less power consumption with respect to bit size. Vedic multiplier is adopted from ancient Indian mathematics which is stated in Atharva Veda. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised andgave mathematical explanation while discussingit for various applications. Swamiji constructed 16 formulae and 16 sub formulae after extensive research in Atharva Veda [2] [3].A general block diagram of Vedic Multiplier is shown in figure 1.

Author α: Assistant professor, Dept of IT, GITAM University, Visakhapatnam, AP, India. e-mail: narasimha.yamarthi@gmail.com
Author σ: Professor, Department of Computer Science, Andhra University, Visakhapatnam, AP, India.
Author ρ: AIMS College of Engineering, Mummidivaram, Amalapuram East Godavari, AP, India.

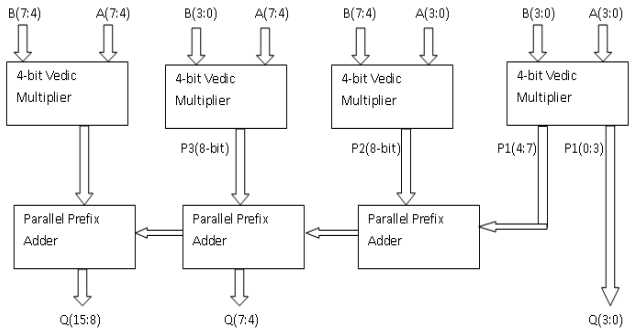


Figure 1 : Block diagram of Vedic Multiplier

There are many adders effectively working in many different types of multipliers. A time, area, and power consumption is studies in previous work [4][5], which are the base work for the present paper. The Carry Look-Ahead Adder (CLA) requires large area and consumes high power with respect to the bit size. So there is a Speed limitation with respect to bit size [6]. Unlike CLA the carry-select adder (CSA) increases its are a requirements to enhance its speed performance. In CSA irrespective of arrival of carry-in, the sum will arrive at output. So it will take less time than other methods to calculate the sum [7][8]. In the proposed work Parallel Prefix Adders (PPA) are selected because addition is done quicker than traditional adders. The large fan-out in PPA can be eliminated by increasing the number of levels of cells and buffers [5]. The Kogg-stone Adder (KSA) is most widely used adder for high performance. It has very low fan-out which makes it performance high [9]. The Brent-Kung adder (BKA) requires less area and minimum interconnecting wires than Kogge-Stone adder [9][10]. The Ladner-Fischer Adder (LFA) adder requires less area when compared with KSA, but has large fan-out [9][10].

II. Motivation

In the previous paper few parameters are measured and compared for Vedic Multiplier with different fast adders. Based on these results it is observed that LFA is selected with less area and less power consumption [5]. Hence the next work is extended with implementation of Pipelined Vedic Multiplier (PVM) with LFA. So In the previous work it is tested and observed that a good throughput is achieved in PVM when compared with Traditional Vedic Multiplier

(TVM) [4]. It is also analysed that as the pipeline is incorporated in traditional circuit, the cell area increased little more when compared with traditional Vedic multiplier. The increase in cell area also leads more power consumption. These analyses done with Ladner Fischer adder (LFA)under Parallel Prefix Adder (PPA) structure [4]. Although the circuit complexity increased in the PVM [4] it is observed that it has relatively less power consumption and better throughput when compared with other existing techniques. This motivates us to measure all the parameters of PVM with all adders. This may lead to a new significant of work. In the present paper the PVM is also tested with various other adders for identifying better results and to find flaws with other adders. This work will be more interesting for future researchers.

III. Proposed Work

In the present work a new architecture is proposed for Vedic Multiplier. Although this method is proposed in my past paper [4], but in the present paper pipeline is applied to all different types of fast adders as case study and makes us flexible to select an adder according to the requirement. It is observed some exciting results with each adder. Each adder is idiosyncratic for a specific application. In the proposed work two 8-bit data A (0:7) and B (0:7) is taken for multiplication.

In the present method pipeline stages are integrated at individual stages of PPA as shown in figure 1[4]. Figure 2 is showing a comprised block diagram of Pipelined Vedic Multiplier (PVM). After adding these pipeline stages the circuit area increases and hence the power consumption also increases when compared with TVM. But this varies from one adder to another adder. So the pipeline technology is applied to all adders and tested to choose best adder with high performance. As each adder is peculiar for a parameter we can consider any adder as per the requirement, and we can simply neglect other adders as they are important in some other area.

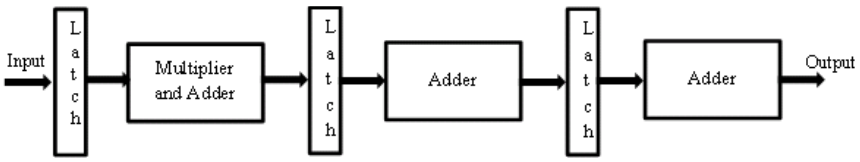


Figure 2 : Block Diagram of Pipelined Vedic Multiplier

In figure 2 latches are place in between input, multiplier and adders. Initially all input are entered into 4-bit Vedic multiplier through first stage of latches. The partial product generated at first stage will enter into next stage latches and the second partial product will be generated and passed through at third stage latches and final product will be produced at last adder circuit. The adder circuit implies all adders such as RCA, CSLA, LFA, BKA, and KGA.

IV. Results

The circuit is designed and analysed using Cadense RTL Compiler v08.10.The circuit is tested on different adders like RCA, CSLA, LFA, BKA, and KGA with and without pipeline technology. Table 1 is showing measured parameters such as Area, Throughput and Power Consumption in TVM and PVM with different adders. The area represented in terms of number of gates, Throughput measured in Nano-seconds (ns) and power consumption indicated in milli-watts (mw). Figure 3 and Figure 4 are showing relative work between TVM and PVM. Figure 5 is showing RTL schematic of a Pipelined Vedic Multiplier. Figure 6.1a to 6.1c is showing simulation results of Brent-Kung adder (BKA) showing cell area, delay and power consumption respectively. Figure 7.1a to 7.1c is showing simulation results of Carry Select adder (CSLA) showing cell area, delay and power consumption respectively. Figure 8.1a to 8.1c is showing simulation results of Kogge-Stone adder (KGA) showing cell area, delay and power consumption respectively. Figure 9.1a to 9.1c is showing simulation results of Ripple Carry adder (RCA) showing cell area, delay and power consumption respectively.

Table 1 : Comparision Table of Vedic Multiplier with different adders

	Regular Vedic Multiplier	RCA	CSLA	PPA		
				LFA	BKA	KGA
Area	348	420	309	415	411	410
Throughput	15	12ns	9ns	10ns	10ns	10ns
Power	10	57.2mW	42.2mW	57.3mW	57.4mW	57.0mW

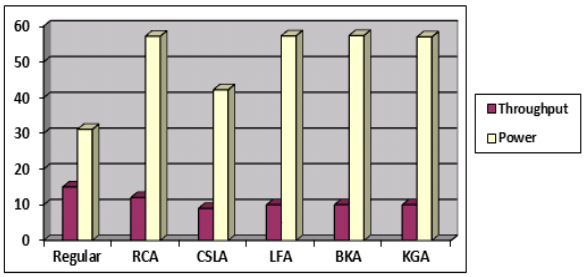


Figure 3 : Comparision of Throughput (ns) and Power Consumption (mW) between TVM and PVM

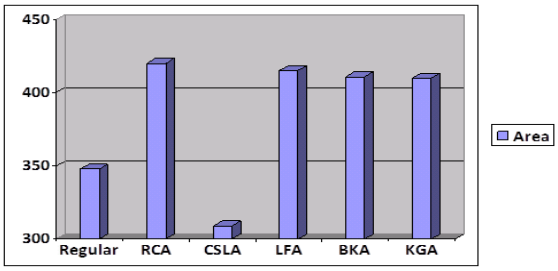


Figure 4 : Comparision of area (no of Gates) between TVM and PVM

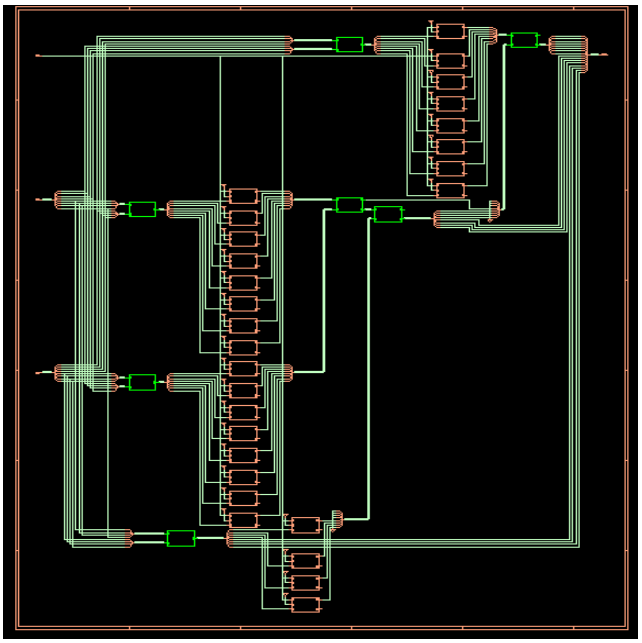
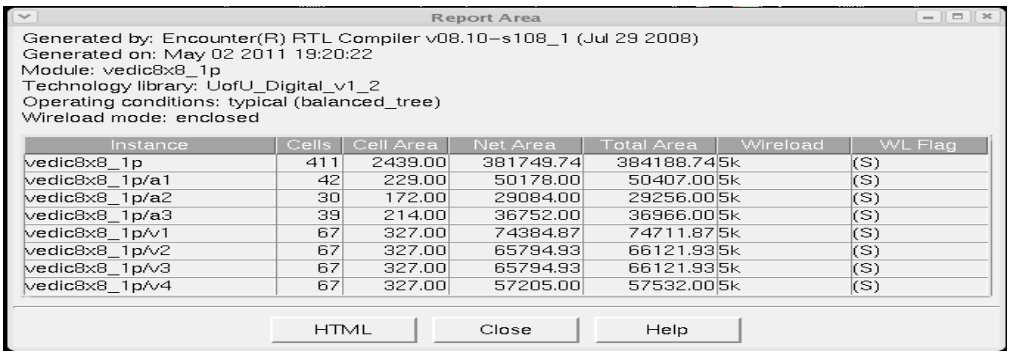
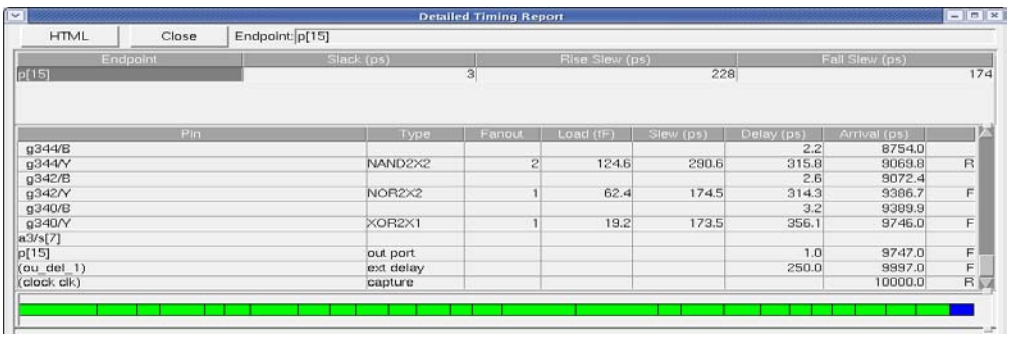


Figure 5 : RTL Schematic of Pipelined Vedic Multiplier



Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
vedic8x8_1p	411	2439.00	381749.74	384188.74	5k	(S)
vedic8x8_1p/a1	42	229.00	50178.00	50407.00	5k	(S)
vedic8x8_1p/a2	30	172.00	29084.00	29256.00	5k	(S)
vedic8x8_1p/a3	39	214.00	36752.00	36966.00	5k	(S)
vedic8x8_1p/v1	67	327.00	74384.87	74711.87	5k	(S)
vedic8x8_1p/v2	67	327.00	65794.93	66121.93	5k	(S)
vedic8x8_1p/v3	67	327.00	65794.93	66121.93	5k	(S)
vedic8x8_1p/v4	67	327.00	57205.00	57532.00	5k	(S)

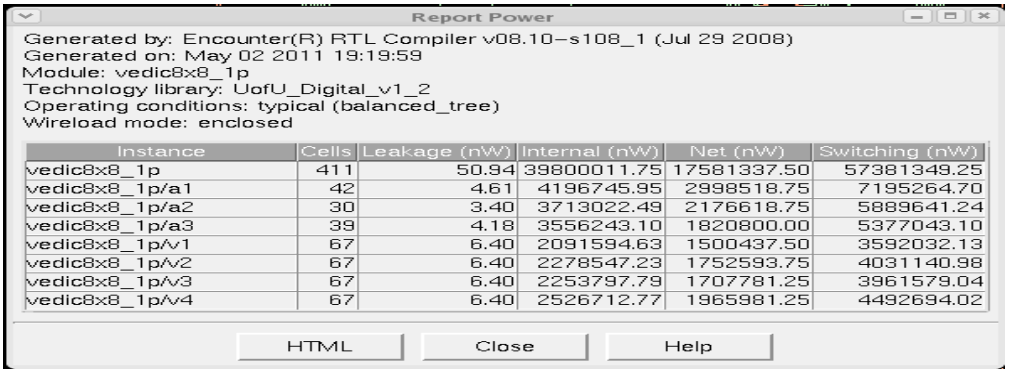
Figure 6.1a : Simulation Results of Cell area in BKA



Endpoint	Slack (ps)	Rise Slew (ps)	Fall Slew (ps)
p[15]	3	228	174

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
g344/B					2.2	8754.0	
g344/Y	NAND2X2	2	124.6	280.6	315.8	9069.8	R
g342/B					2.6	9072.4	
g342/Y	NOR2X2	1	62.4	174.5	314.3	9386.7	F
g340/B					3.2	9389.9	
g340/Y	XOR2X1	1	19.2	173.5	356.1	9746.0	F
a3/s[7]							
p[15]	out port				1.0	9747.0	F
(ou_del_1)	ext delay				250.0	9997.0	F
(clock clk)	capture					10000.0	R

Figure 6.1b : Simulation Results of delay in BKA



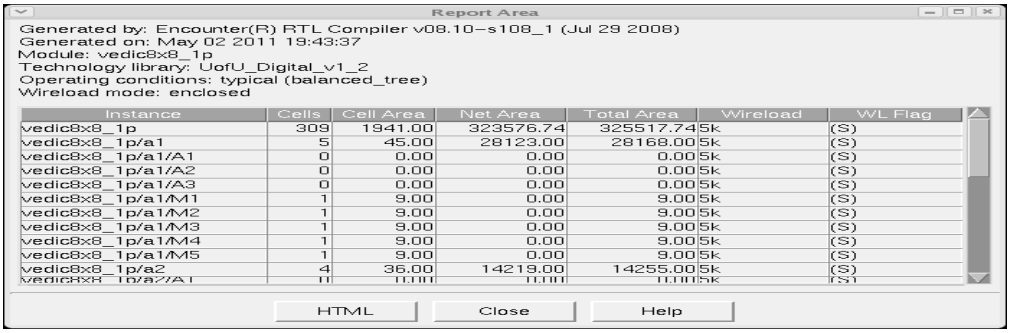
Report Power

Generated by: Encounter(R) RTL Compiler v08.10-s108_1 (Jul 29 2008)
Generated on: May 02 2011 19:19:59
Module: vedic8x8_1p
Technology library: UofU_Digital_v1_2
Operating conditions: typical (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
vedic8x8_1p	411	50.94	39800011.75	17581337.50	57381349.25
vedic8x8_1p/a1	42	4.61	4196745.95	2998518.75	7195264.70
vedic8x8_1p/a2	30	3.40	3713022.49	2176618.75	5889641.24
vedic8x8_1p/a3	39	4.18	3556243.10	1820800.00	5377043.10
vedic8x8_1p/v1	67	6.40	2091594.63	1500437.50	3592032.13
vedic8x8_1p/v2	67	6.40	2278547.23	1752593.75	4031140.98
vedic8x8_1p/v3	67	6.40	2253797.79	1707781.25	3961579.04
vedic8x8_1p/v4	67	6.40	2526712.77	1965981.25	4492694.02

HTML Close Help

Figure 6.1c : Simulation Results of Power Consumption in BKA



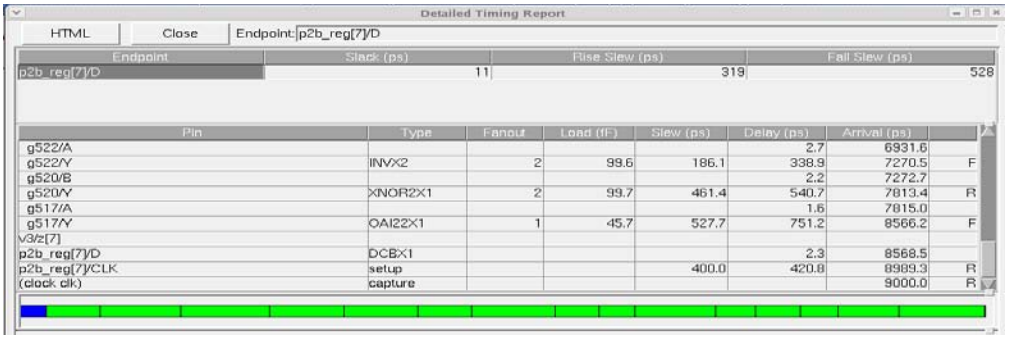
Report Area

Generated by: Encounter(R) RTL Compiler v08.10-s108_1 (Jul 29 2008)
Generated on: May 02 2011 19:43:37
Module: vedic8x8_1p
Technology library: UofU_Digital_v1_2
Operating conditions: typical (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
vedic8x8_1p	309	1941.00	323576.74	325517.74	5k	(S)
vedic8x8_1p/a1	5	45.00	28123.00	28168.00	5k	(S)
vedic8x8_1p/a1/A1	0	0.00	0.00	0.00	5k	(S)
vedic8x8_1p/a1/A2	0	0.00	0.00	0.00	5k	(S)
vedic8x8_1p/a1/A3	0	0.00	0.00	0.00	5k	(S)
vedic8x8_1p/a1/M1	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M2	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M3	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M4	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M5	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a2	4	36.00	14219.00	14255.00	5k	(S)
vedic8x8_1p/a2/A1	1	1.111	1.111	1.111	5k	(S)

HTML Close Help

Figure 7.1a : Simulation Results of Cell area in CSLA



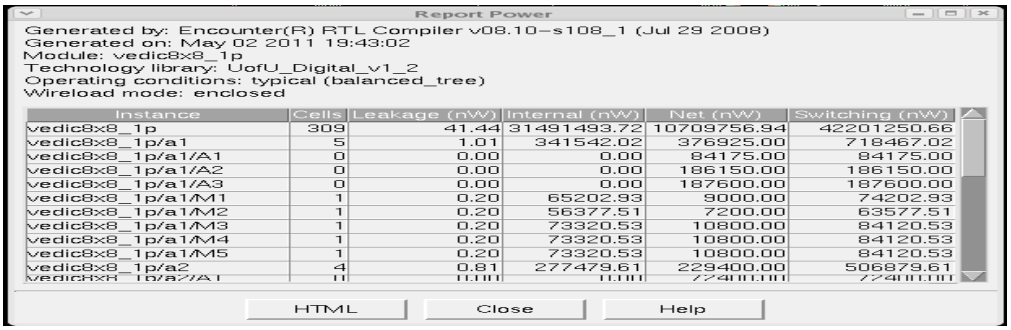
Detailed Timing Report

HTML Close Endpoint: p2b_reg[7]/D

Endpoint	Slack (ps)	Rise Slew (ps)	Fall Slew (ps)
p2b_reg[7]/D	11	319	528

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
g522/A					2.7	6931.6	
g522/Y	INVX2	2	99.6	186.1	338.9	7270.5	F
g520/B					2.2	7272.7	
g520/Y	XNOR2X1	2	99.7	461.4	540.7	7813.4	R
g517/A					1.6	7815.0	
g517/Y	OAI22X1	1	45.7	527.7	751.2	8566.2	F
v3/z[7]							
p2b_reg[7]/D	DCBX1				2.3	8568.5	
p2b_reg[7]/CLK	setup			400.0	420.8	8989.3	R
(clock clk)	capture					9000.0	R

Figure 7.1b: Simulation Results of delay in CSLA



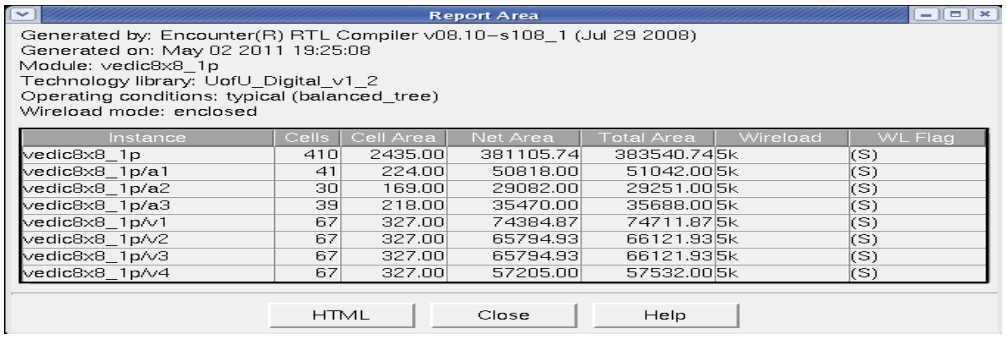
Report Power

Generated by: Encounter(R) RTL Compiler v08.10-s108_1 (Jul 29 2008)
Generated on: May 02 2011 19:43:02
Module: vedic8x8_1p
Technology library: UofU_Digital_v1_2
Operating conditions: typical (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
vedic8x8_1p	309	41.44	31491493.72	10709756.94	42201250.66
vedic8x8_1p/a1	5	1.01	341542.02	376925.00	718467.02
vedic8x8_1p/a1/A1	0	0.00	0.00	84175.00	84175.00
vedic8x8_1p/a1/A2	0	0.00	0.00	186150.00	186150.00
vedic8x8_1p/a1/A3	0	0.00	0.00	187600.00	187600.00
vedic8x8_1p/a1/M1	1	0.20	65202.93	9000.00	74202.93
vedic8x8_1p/a1/M2	1	0.20	56377.51	7200.00	63577.51
vedic8x8_1p/a1/M3	1	0.20	73320.53	10800.00	84120.53
vedic8x8_1p/a1/M4	1	0.20	73320.53	10800.00	84120.53
vedic8x8_1p/a1/M5	1	0.20	73320.53	10800.00	84120.53
vedic8x8_1p/a2	4	0.81	277479.61	229400.00	506879.61
vedic8x8_1p/a2/A1	1	1.111	1.111	1.111	1.111

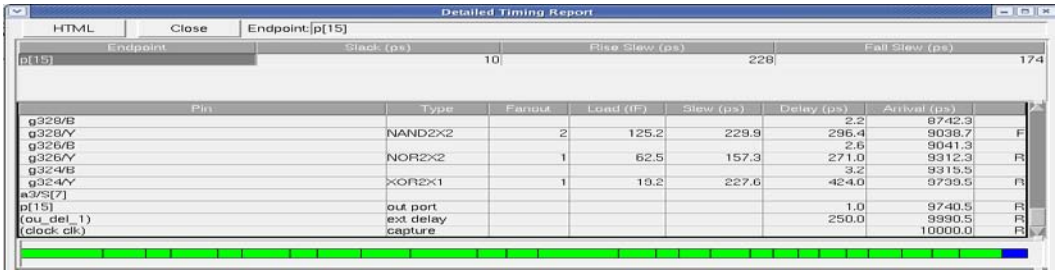
HTML Close Help

Figure 7.1c : Simulation Results of Power Consumption in CSLA



Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
vedic8x8_1p	410	2435.00	381105.74	383540.74	5k	(S)
vedic8x8_1p/a1	41	224.00	50818.00	51042.00	5k	(S)
vedic8x8_1p/a2	30	169.00	29082.00	29251.00	5k	(S)
vedic8x8_1p/a3	39	218.00	35470.00	35688.00	5k	(S)
vedic8x8_1p/v1	67	327.00	74384.87	74711.87	5k	(S)
vedic8x8_1p/v2	67	327.00	65794.93	66121.93	5k	(S)
vedic8x8_1p/v3	67	327.00	65794.93	66121.93	5k	(S)
vedic8x8_1p/v4	67	327.00	57205.00	57532.00	5k	(S)

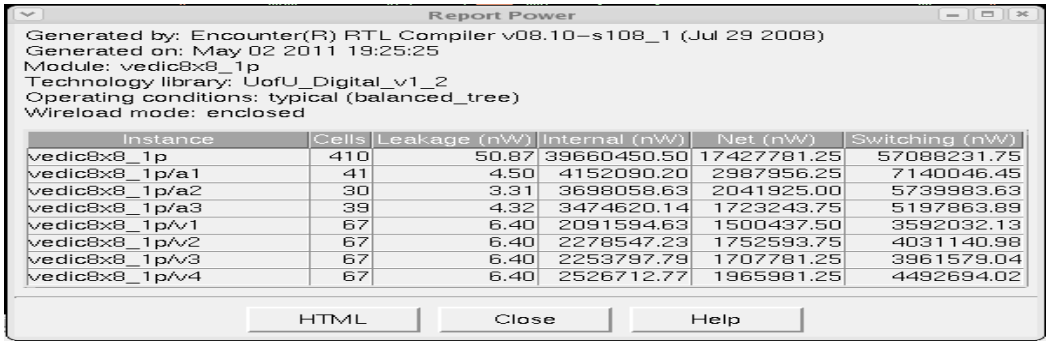
Figure 8.1a : Simulation Results of Cell area in KGA



Endpoint	Slack (ps)	Rise Slew (ps)	Fall Slew (ps)
p[15]	10	228	174

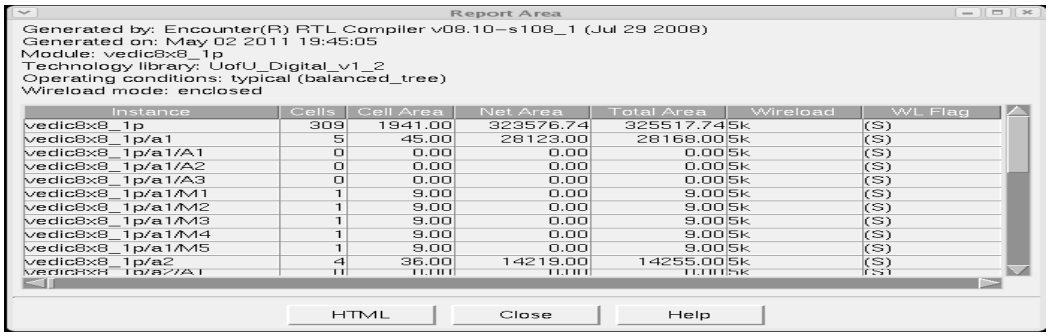
Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
g328/B					2.2	8742.3	
g328/Y	NAND2X2	2	125.2	229.9	296.4	9038.7	F
g326/B					2.6	9041.3	
g326/Y	NOR2X2	1	62.5	157.3	271.0	9312.3	R
g324/B					3.2	9315.5	
g324/Y	XOR2X1	1	19.2	227.6	424.0	9739.5	R
a3/S[7]							
p[15]	out port				1.0	9740.5	R
(ou_del_1)	ext delay				250.0	9990.5	R
(clock clk)	capture					10000.0	R

Figure 8.1b : Simulation Results of delay in KGA



Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
vedic8x8_1p	410	50.87	39660450.50	17427781.25	57088231.75
vedic8x8_1p/a1	41	4.50	4152090.20	2987956.25	7140046.45
vedic8x8_1p/a2	30	3.31	3698058.63	2041925.00	5739983.63
vedic8x8_1p/a3	39	4.32	3474620.14	1723243.75	5197863.89
vedic8x8_1p/v1	67	6.40	2091594.63	1500437.50	3592032.13
vedic8x8_1p/v2	67	6.40	2278547.23	1752593.75	4031140.98
vedic8x8_1p/v3	67	6.40	2253797.79	1707781.25	3961579.04
vedic8x8_1p/v4	67	6.40	2526712.77	1965981.25	4492694.02

Figure 8.1c : Simulation results of Power Consumption in KGA



Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
vedic8x8_1p	309	1941.00	323576.74	325517.74	5k	(S)
vedic8x8_1p/a1	5	45.00	28123.00	28168.00	5k	(S)
vedic8x8_1p/a1/A1	0	0.00	0.00	0.00	5k	(S)
vedic8x8_1p/a1/A2	0	0.00	0.00	0.00	5k	(S)
vedic8x8_1p/a1/A3	0	0.00	0.00	0.00	5k	(S)
vedic8x8_1p/a1/M1	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M2	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M3	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M4	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a1/M5	1	9.00	0.00	9.00	5k	(S)
vedic8x8_1p/a2	4	36.00	14219.00	14255.00	5k	(S)
vedic8x8_1p/a2/A1	0	0.00	0.00	0.00	5k	(S)

Figure 9.1a : Simulation Results of Cell area in RCA

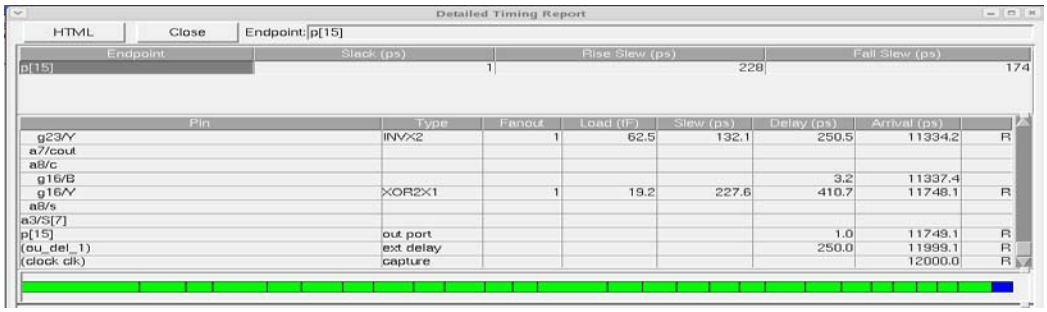


Figure 9.1b : Simulation Results of delay in RCA

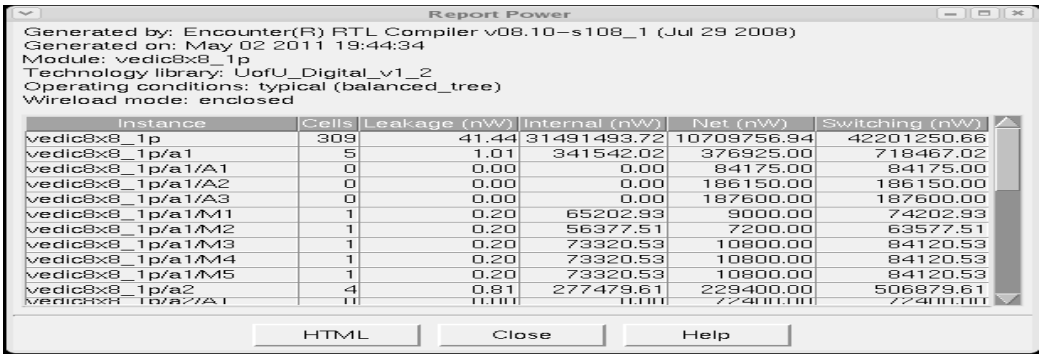


Figure 9.1c : Simulation Results of Power Consumption in RCA

V. Conclusion

The Traditional Vedic Multiplier consumes less power as it circuit complexity is simple. But the data speed is slow in TVM. In pipeline Vedic Multiplier while first partial product is generating the second input (next 8-bit data) can be fetched into the multiplier. A High throughput is observed in Pipelined Vedic multiplier when compared with Traditional Vedic Multiplier. In parallel prefix adders a constant throughput is achieved. But KGA could be best adder as it has less number of gates and consuming less power than other parallel prefix adders. Overall the performance of the pipelined Vedic Multiplier is high when compared with Regular Vedic Multiplier.

References Références Referencias

1. Rakshith Saligram et al., "Optimized Reversible Vedic Multipliers for High Speed Low Power Operations", Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT 2013), pp809-814.
2. Jagadguru Swami Sri Bharath, Krsna Tirathji, "Vedic Mathematics or Sixteen Simple Sutras From The Vedas", Motilal Banarsidas, Varanasi (India), 1986.
3. G. Ganesh Kumar et al., "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques", International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012, pp1-5.
4. Y. Narasimharao et al., "Design of high speed vedic multiplier with pipeline technology", JATIT, VOL 67 Issue no 3, 2014.
5. Y. Narasimharao et al., "Studies and Performance Evaluation of Vedic Multiplier using Fast Adders", IJCET, Vol 4 no3, Jun 2014, pp1908-1912.
6. Hoe, D.H.K. et al.,"Design and characterization of parallel prefix adders using FPGAs" , IEEE, 43rd Southeastern Symposium on System, 2011.
7. Desiree JV, "Fast and Area Efficient RSA Cryptosystem Design Using Modified Montgomery Multiplication for FPGA Applications", IJSER, vol4 no7, July 2013.
8. Lecture Notes, Parallel Adder - Concordia University, http://users.encs.concordia.ca/~asim/COEN_6501/Lecture_Notes /~WRL2849.tmp
9. G.Jyoshna et al.,"Parallel-Prefix Adder Architecture With Efficient Timing-Area Characteristic",UACEE International journal of Advances in Electronics Engineering Vol:1 Issue:1, 2011.
10. Sreenath K, "Reconfigurable VLSI architecture for FFT computation", IJSER, vol 3 no6, june 2012.

Biography

Mr. Y. Narasimha Rao, working as Assistant professor, in the department of Information technology, GITAM University, Visakhapatnam, has more than 10 years academic experience. He has completed his Masters degree from Acharya Nagarjuna University. He has published couple of research papers in reputed international journals and conferences. Presently he is

doing his research work in Andhra University. His research of interest is Parallel processing, Advanced computer architecture, Cryptography algorithms and Network security.

Dr. G. Samuel Vara Prasada Raju received the M.Tech degree in CS&SE from Andhra University in 1993. He received PhD degree from Andhra University in 1996. From 1994 to 2003 worked as Asst. Professor in the Dept. of CS&SE in Andhra University College of Engineering. From 2003 onwards worked as Associate Professor and Director of the CS&SE Department for School of Distance Education of Andhra University College of Engineering. His research interest includes ecommerce, Network Security, Cryptography, Data Mining and parallel processing. He has more than 30 years of experience in Academics and Research.

Prof. Penmetsa V Krishna Raja has more than 15 years of academic experience. Presently he is working as Principal, AIMS college of Engineering, Amalapuram. He has Completed his Masters from Andhra University and Ph.d from JNTUK. He has published more than 20 research paper in reputed National and International Journals. His Research of interest includes Data Mining, Cryptography and Network Security, Bio Informatics, Image processing and Parallel processing.