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Low Power Conditional Sum Adder using Modified Ripple Carry Adder

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Abstract

Carry select adder (CSeLA) is mainly used to alleviate the propagation delay caused by carry bit and upon which sum bit is generated. It produces n+1 sum from n bits. In this Paper, a simple Gate level implementation of regular Carry Select Adder is compared with our proposed work. Based on the comparison made in terms of power, delay and area, it is found that there is considerable reduction in area and power with delay overhead. Both regular and proposed methods are modeled using 180nm CMOS technology. From the results obtained, it is clear that proposed CSeLA is better than regular CSeLA.

Index terms— CMOS, delay efficient, CSeLA, low power, Propagation delay.

1 INTRODUCTION

esigning power efficient, high performance adder is one of the major concerns as far as VLSI Sub system is considered. Speed is usually limited due carry propagation bit of an adder. The sum of final bit is generated by the carry propagation from the previous bit to next stage. The CSeLA consists of two multiplexed ripple carry adder and performs operation in parallel with carry Cin=0 and Cin=1, then final sum is selected through multiplexer (mux). Due to multiplexed RCA, there is considerable increase in area, which reveals that there is scope for reduction in area [2].

The main idea behind this work is to compare regular carry select adder with modified carry select adder. The modified carry select adder uses Boolean function based RCA along with modified XOR gate. The main advantage of this modified RCA comes with reduced gate count than the n-bit Full adder circuit.

This paper is organized as follows. Section II deals with the delay and area measurement of conventional full adder. Section III explains the Boolean function based RCA design. Section IV shows the comparison between proposed methods with regular CSeLA. Section V shows the power and delay evaluation of regular CSeLA and modified CSeLA. The implementation method and results obtained are analyzed in Section VI. The work is finally concluded in Section VII.

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2 DELAY AND AREA EVALUATION OF CONVENTIONAL ADDER

The XOR gate is implemented using conventional AOI logic. The delay and area is found from this AOI logic, with the assumption that each gate having delay equal to one and the gate with the longest path contribute critical path delay. The total number of gate in AOI logic contributes to total area of logic block. Based on this method, 2:1 Mux, full adder, half adder, XOR are evaluated. The main idea is to use modified RCA instead of RCA with Cin=0 to reduce area and power consumption of regular CSeLA. The AOI implementation of full adder requires 14 gates, while the modified full adder CSeLA has two ripple carry adder with Cin=0 and Cin=1

and multiplexer to choose data one among them. One of two RCA is replaced with Boolean function (BF), which has reduced number of gate count. From the truth table of full adder its evident that sum is obtained from D ? The group 2 has two bit RCA, which comprises 1 FA and 1 HA with Cin=0 and other RCA with Cin=1 is replaced with modified BEC -1.

3 Delay and area evaluation of CSeLA

? Based on the delay and area analysis listed in Table **??**, the total number of gate count for group 2 is ? Propagation delay of proposed carry select adder is given as, T Proposed = T s + (N-1) T mux + T sum = 3ns ? Area and delay is computed in same way as that of group 2 and listed in Table 1.

V.

4 Experimental Results

The proposed work is designed using DSCH simulator and synthesized using 180nm technology. The synthesized verilognetlist is imported to Microwind and automatic layout is generated. From Microwind, power, area and delay is found by choosing different technology.

Table 2 shows the simulation results of both regular and modified CSeLA in terms of delay, power and area. Each individual cell in the design contributes the total cell area. Total power consumption is the sum of leakage power, switching power and static power. Area, power, delay, power delay product (PDP) is shown in fig. in terms of percentage reduction. The total power reduction for 8-b, 16-b, 32-b are 9.3 %, 23.1%, 9.7% respectively. Similarly Percentage reduction in area is shown in fig. There is delay overhead of 14.9%, 12.1%, 6.18% respectively.

5 Conclusion

A modified approach for carry select adder is proposed in this paper to reduce power and delay compared to conventional CSLA. The modified structure of RCA and BEC provides the scope for further area reduction and power for 90nm technology. From the experimental results it is clear that there is 9.3 %, 23.1%, 9.7% reduction in power and 10.5 %, 24.9%, 18.3% reduction in area with 14.9%, 12.1%, 6.18% delay overhead. The modified Carry Save Adder is thus area and power efficient. [1] [2]

1 

Figure 1: Figure 1 :

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[2] © 2014 Global Journals Inc. (US) Low Power Conditional Sum Adder Using Modified Ripple Carry Adder

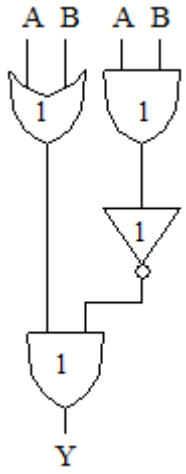

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Figure 2: Figure 3 :

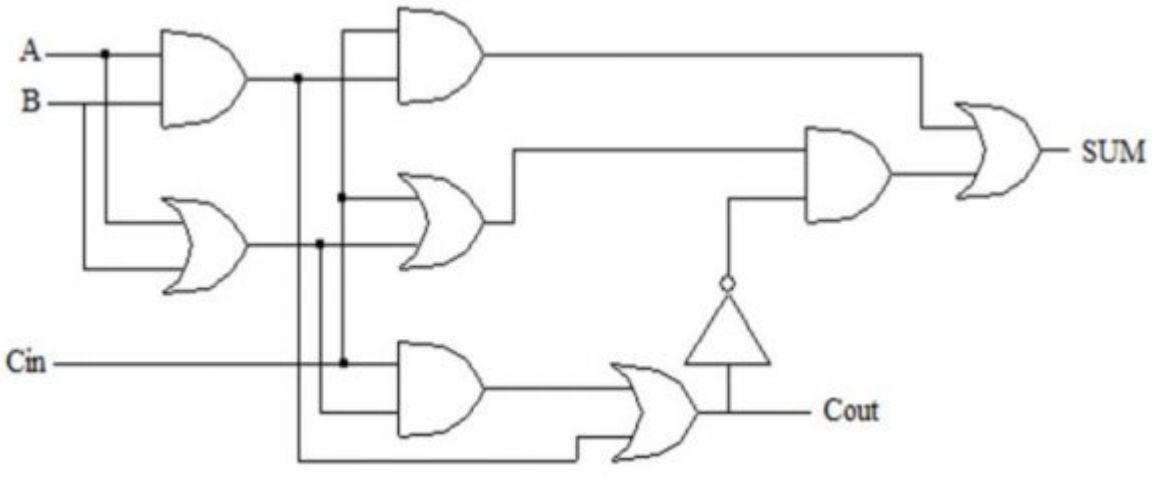

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Figure 3: Figure 4 :Figure 5 :Figure 6 :

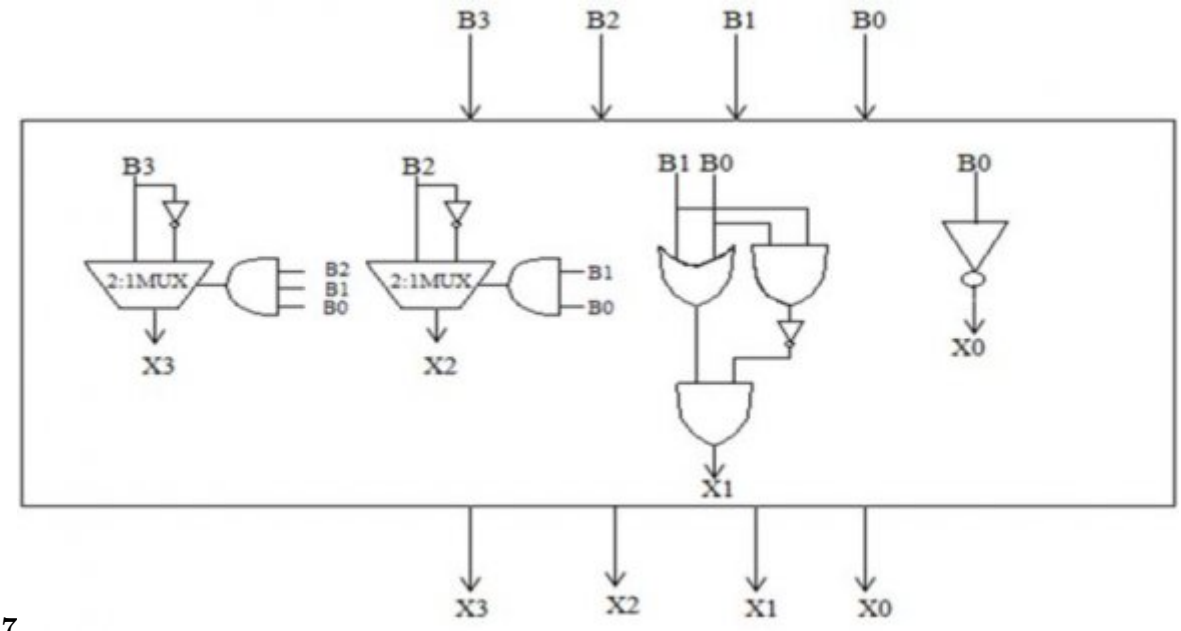

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Figure 4: Figure 7 :

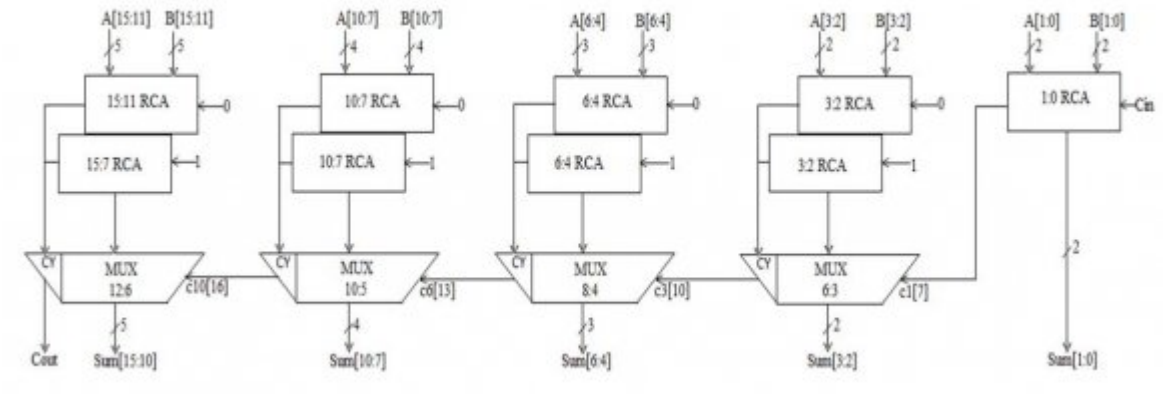

Figure 5:

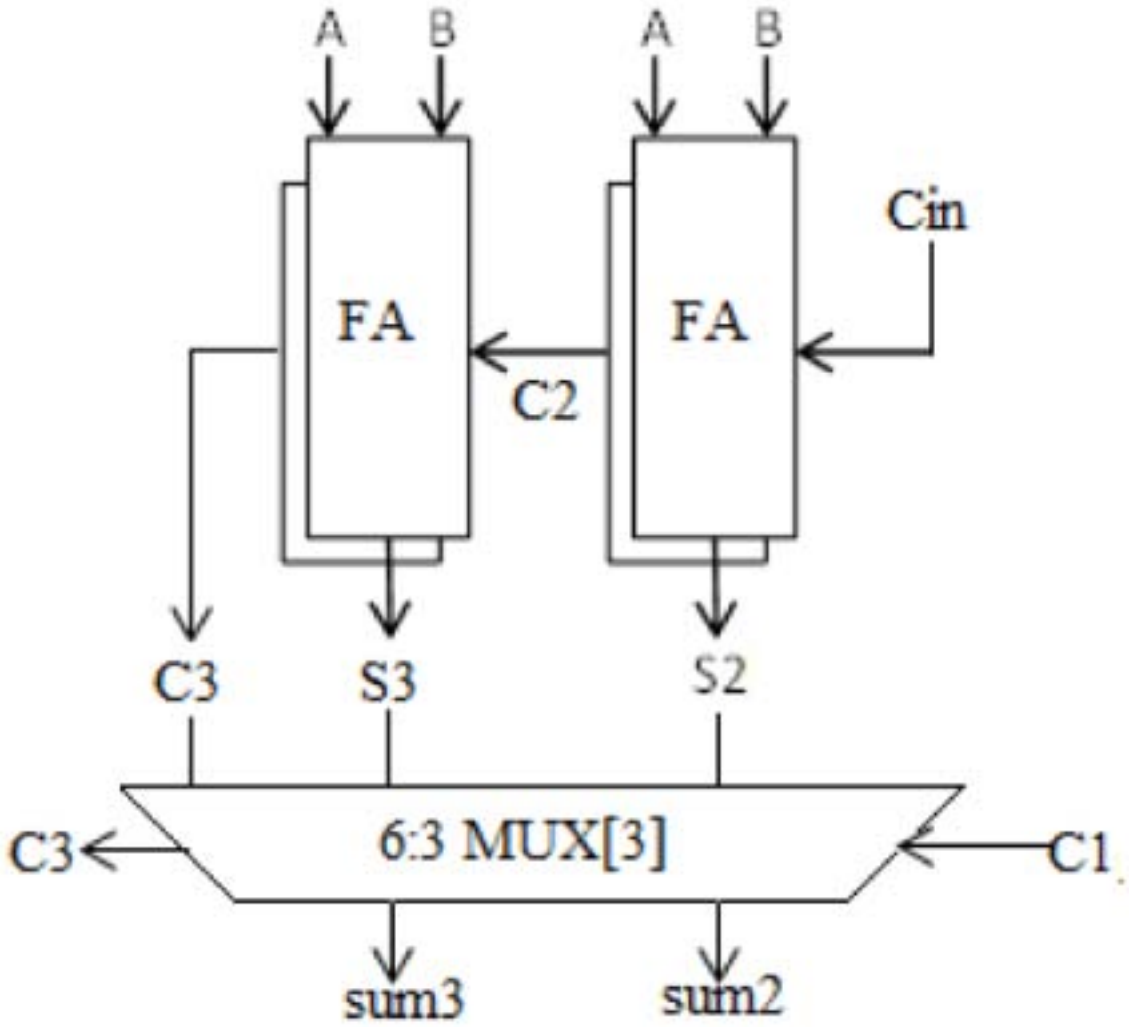

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Figure 6: Figure 11 :

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1-Bit Adder	Delay	Area	Issue V Version I
Full adder Half adder 2:1	6 3 3 3	13 6 4 5	( ) F Volume XIV
MUX XOR AND	1	1	
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Figure 7: Table 1 :

2

Word Size	Adder	Power (mW)	Area(um 2)	Delay(ns)	PDP(pW)
8-Bit	Conventional CSLA	0.32	941	1.61	0.515
	Modified CSLA	0.29	842	1.85	0.3885
16-Bit	Conventional CSLA	0.69	2435	2.62	1.80
	Modified CSLA	0.53	1829	2.94	1.55
32-Bit	Conventional CSLA	0.92	4683	4.93	4.53
	Modified CSLA	0.83	3826	5.13	4.25

VI.

Figure 8: Table 2 :

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