AC Characteristics of a Dual Gate Large Area Graphene MOSFET

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Abstract

This paper presents a detailed study of RF characteristics together with the high frequency performance of dual gate large area graphene MOSFET. A quasi analytical modeling approach is presented here. To know the RF characteristics of a graphene MOSFET, the transconductance is simulated using small signal equivalent model. Finally the intrinsic top and back gate gain of graphene MOSFET are also shown which are very important figure of merit for RF applications.

Index terms— graphene MOSFET, GFET, large area graphene, top and back gate gain, transconductance.

1 Introduction

raphene is a flat monolayer of sp^2 carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice including a linear energy dispersion relation [1]. Graphene offers many of the advantages such as high carrier mobilities up to 10×2 5 cm 2 V -1 s -1 in substrate supported devices and high saturation velocity [2] [6]. The novel electronic properties of graphene lead to intense research into possible applications of this material in nano scale devices such as dual gate graphene MOSFETs.

There have been studies on designing and fabrication of dual gate graphene MOSFETs. However, the progress in designing and fabricating of G-MOSFETs is at initial stage. In order to fabricate high performance G-MOSFETs, understanding of detailed device modeling and performance evaluations is urgently required. The recent works have been concentrated mostly on the DC characteristics of large area graphene MOSFETs using different approaches. However, there have no significant works on AC characteristics although graphene is predicted to highly attracted material for nano-scale devices.

2 II.

3 Device Model

A dual gated graphene MOSFET is considered for our work shown in Fig. 1. Graphene grown on metal and transferred to a SiO_2 covered Si wafer is used as the channel of the MOSFET. The length and width of the graphene channel are 5 µm and 1 m respectively. Here, HfO_2 (k=9) is used as top-gate oxide and SiO_2 (k=3.9) is used as back-gate oxide [5], [7]. The goal of this work is to model the highfrequency characteristics of these devices. This will be done by calculating the elements of the small-signal equivalent circuit. Before we can deal with these elements we need to know how to calculate the channel charge, since this is essential in order to determine the gate-source and gate-drain capacitances. In general the channel charge Q_{ch} can he calculated by subtracting the amount of electrons from the amount of holes and multiplying the result by the elementary charge. This can be written as **??**09].

(01)

To obtain Q_{ch} , a simple numerical integration is performed using a trapezoidal approximation. The x dependence of the local hole and electron sheet densities can be translated into a dependence on the local voltage V(x). By using this equation It is important to distinguish between p, n and in the formula above. If we neglect the minority charge carriers, p(V(x))-n(V(x)) is equal to can be expressed as:? ? ? L ch dx x n x p qW Q)) (( ) (x V v I x V qW x dV

(05)

The integral to determine Qch is solved numerically. We have used the MATLAB simulation. Note that to calculate channel charge as well as small signal parameters the internal voltages have to be used The high-frequency behavior of the transistor can be modeled with a small-signal equivalent circuit [10] as shown in Figure2. The intrinsic transistor is described by the transconductance g m , the drain conductance gds, the gate-source capacitance C gs , and the gate-drain capacitance C gd . Thereby the whole behavior of the device is described by these four elements: g m , g ds C gs and C gd . The reason why this is possible is the following. The high-frequency AC signal is thought to be superimposed onto a DC signal, which defines the DC operating point. If the amplitude of the AC signal is small, the nonlinear transistor characteristics can be linearized around the DC operating point. Thus all elements of Fig. 2 The intrinsic transconductance, gm, is related to the internal small-signal gate source and drain-source voltages, VGSi and VDSi, whereas the terminal transconductance, gmt, is related to the applied gatesource and drain-source voltages, VGS and VDS [10].

4 III. Transconductance Calculation

The transconductance calculation is very important to know the radio-frequency characteristics of a graphene MOSFET. The transconductance is defined as the variation in the drain current caused by a small variation in the drain current caused by a small variation in the gate voltage. They are two types: intrinsic transconductance and drain-conductance. ? ? ? ? int 0) ( ) ( ))] (( )) (([ds V ch x dV x dV dx x V n x V p qW Q) ( ))) (( )) ((( )] ( )) (([int 0 x dV x V v I x V qW x nV x V Q sat d V ch real ds ? ? ? ? ? ? ? ? ? real ? real ? q top ox top ox q back ox top gs top gs q top ox top ox q top ox top gs top gs C C C C C V x V V C C C C C V x V V x V n x V p 2 1 2 1)) ((2 1 2 1)) (( )) (( )) ((0 , 0 , ? const V

5 Intrinsic Capacitance Calculation

The intrinsic capacitance is very necessary to calculate the cut-off frequency and other radiofrequency behaviour of a graphene MOSFET. The mobile channel charge depends on the top-gate voltage V gs-top-int , the back-gate voltage V gs-back-int and drain-source voltage V ds- The gate-drain conductance C gd is defined as the variation in the channel charge Q ch caused by a small variation in the drain-source voltage V ds-int with a fixed value of top-gate voltage V gs-top-int .

(12) (13)

The gate-drain capacitance due to the fixed value of top-gate voltage (C gd-top) and the gate-drain capacitance due to the fixed value of back-gate voltage (C gd-back) can be evaluated using Eqn.12 and Eqn.13 also.

V.

6 Intrinsic Gain Calculation

Finally, we show an example of projection of the intrinsic gain as a figure of merit commonly used in RF/analog applications. In small signal amplifiers, for instance, the transistor is operated in the ON-state and small RF signals that are to be amplified are superimposed onto the DC gate-source voltage **??**41]. Instead, what is needed to push the limits of many analog/RF figures of merit, for instance the cut-off frequency or the intrinsic gain, is an operation region where high trans conductance together with a small output conductance is accomplished. Next, we will give an example on how to use our current-voltage DC model to project an important figure-of-merit (FOM) used in RF/analog applications, namely the intrinsic gain (G).

as the ratio of the transconductance to the drainconductance expressed as: Intrinsic top-gate gain, (14)

The top-gate gain (

) is very important in RF/analog applications as well as cut-off frequency.

7 b) Intrinsic Back-Gate Gain, Gback

The intrinsic back-gate gain , which is defined as the ratio of the trans conductance ( ) to the drain-conductance ( ) expressed as: Intrinsic back-gate gain, (15) VI. VII.

8 Results and Discussion

9 Conclusion

In this paper, the AC characteristics of a dual gated Graphene MOSFET are studied using analytical approach. The drain transconductance of the device is computed. We have simulated the top and back gate gain as a function of drain to source voltage. The resulting high intrinsic top ate ain 73 which is promising. [1] [2]

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Figure 1: Figure 1 :

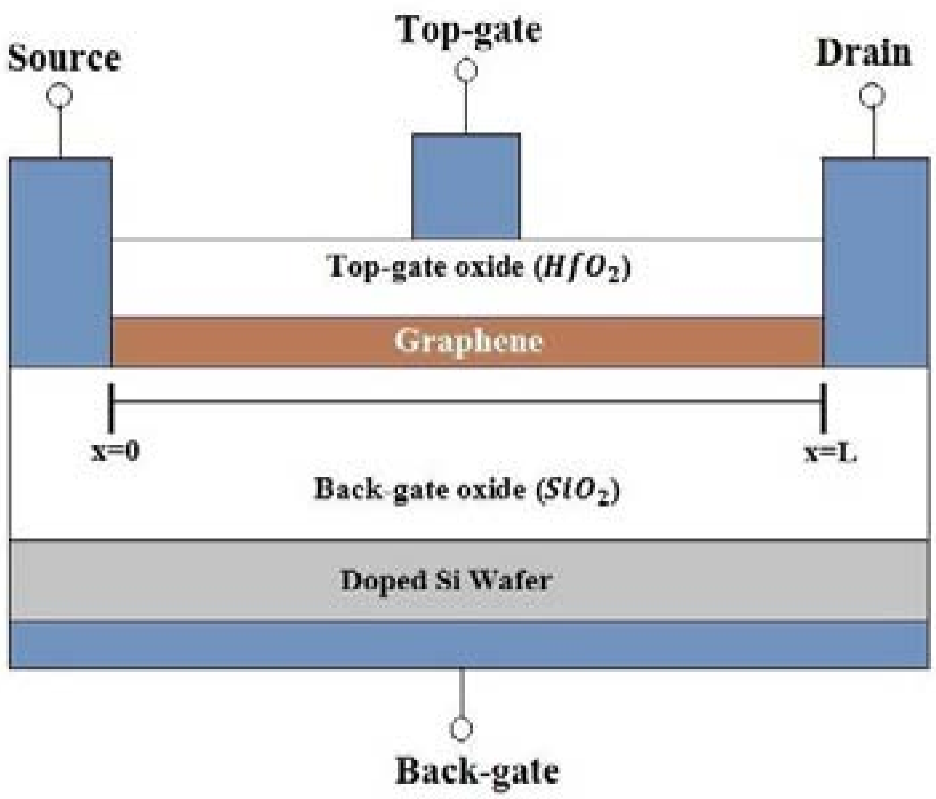

Figure 2:

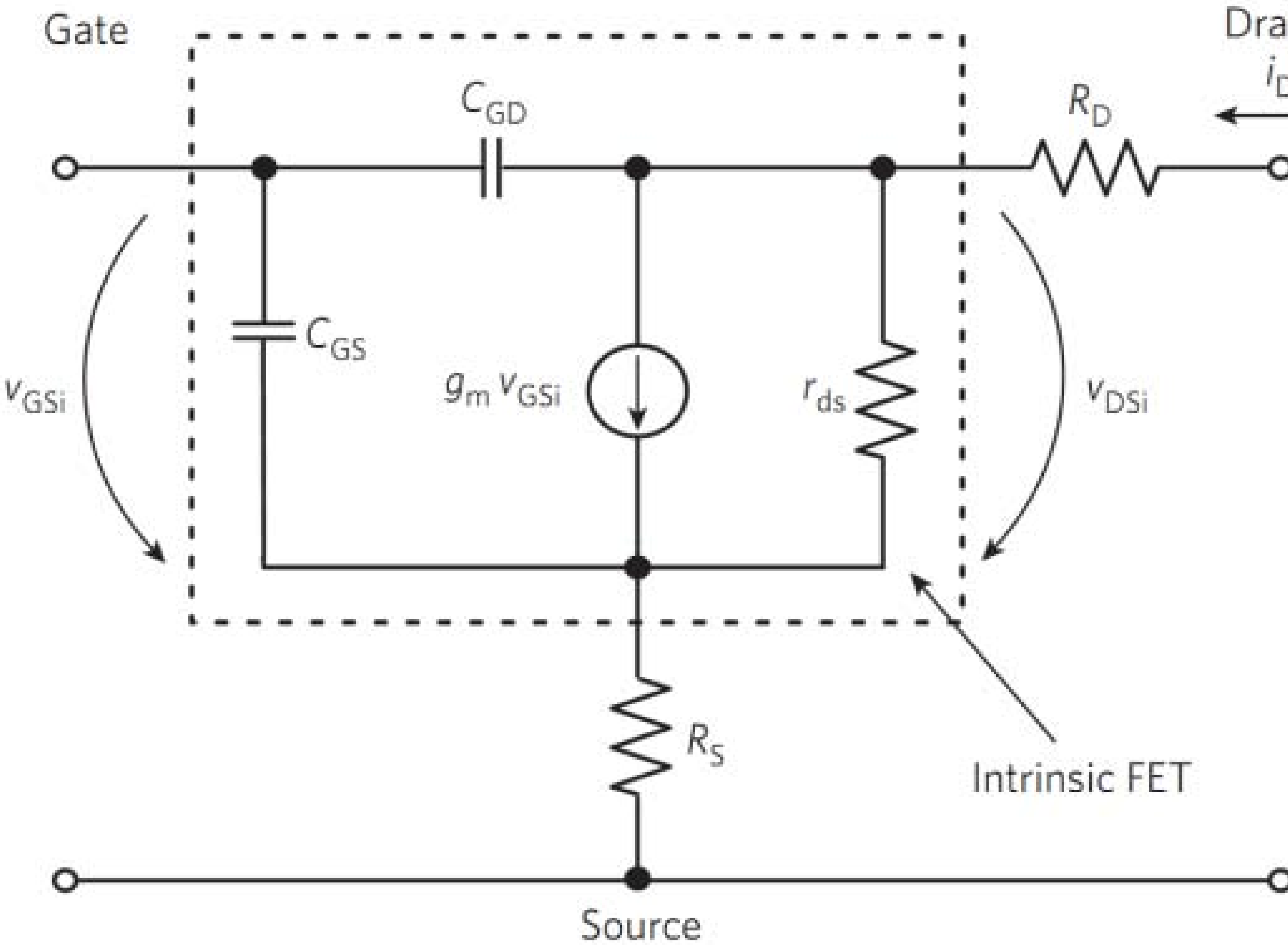

Figure 3:

Figure 4:

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