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Investigation the Impact of Silicon Film Thickness on FDSOI and PDSOI MOSFET Characteristics

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Abstract

The performance of chip is degraded because of the short-channel effect (SCE) as the metal oxide semiconductor field effect transistor (MOSFET) size scales down. Silicon on insulator (SOI) technology helps to reduce the short channel effects and permits a good solution to the miniaturization. The electrical characteristics of fully depleted SOI (FDSOI) and partially depleted SOI (PDSOI) n-channel MOSFET (N-MOSFET) are investigated as silicon film thickness is varied in this paper. Both transistors are compared in terms of electrical parameters which are the threshold voltage, subthreshold slope, on-state current, leakage current and drain induced barrier lowering (DIBL). Silvaco TCAD tools are used for simulating both PDSOI and FDSOI MOSFETs. FDSOI MOSFET is superior to PDSOI MOSFET based on found simulation results.

Index terms— silicon on insulator, subthreshold slope, leakage current, threshold voltage, drain induced barrier lowering.

1 I. Introduction

oday devices of minimized area, reduction in power and increased performance have a great demand in the industry of microelectronics. The feasible technique of semiconductor industry to enhance productivity and performances is scaling of device [1]. The size of MOSFET has continually been scaled down [2]. The submicron technologies have created electrical operational challenges such as threshold voltage (Vth), sub threshold slope and leakage current due to the shrinking of the devices dimensions in MOSFET. The industry is facing difficulty to fulfill the Moore's Law using bulk devices which cause threshold voltage to decrease and leakage current to increase as length of channel decreases because of short channel effect (SCE). Silicon on Insulator (SOI) is considered as a potential alternative over conventional bulk MOSFET due to decreased silicon geometries and simple fabrication process. Radiation hardness, improved switching speeds, reduced leakage currents, better isolation, eliminization of latch up and decrease in the short channel effects are some of the advantages of the SOI devices [3]. It has the intrinsic benefit of reduced source and drain areas and reduction of junction capacitance which makes these devices a potential candidate for low power and voltage applications [4][5][6]. SOI has several benefits over other technological solution such as no latch up, lower threshold voltage and better sub threshold slope [7][8]. There are two types of SOI, which are partially depleted (PD) and fully depleted (FD) depending on the thickness of the silicon film on the insulator. Usually, the thickness of silicon film is between 100nm to 500 nm for PD SOI device. For fully-depleted SOI devices, the thickness of silicon film is about less than 100nm. Due to removal of the floating body effect, FDSOI provides better short channel behaviour compared to the PDSOI. Hui et al. investigated impact of silicon film thickness on leakage current and threshold voltage in PDSOI and FDSOI [9]. This paper presents investigation between partially depleted and fully depleted SOI devices in terms of electrical parameters which are threshold voltage, subthreshold slope, on-state current, leakage current and drain induced barrier lowering. TCAD Silvaco software was used for simulation study of SOI devices. Simulation results revealed that the electrical characteristics such as threshold voltage, subthreshold slope and leakage current of fully depleted SOI outperformed than that of partially depleted SOI devices. There is difference in turn on voltage in fully depleted SOI (FDSOI) MOSFET. The threshold voltage is stable in partially depleted SOI (PDSOI) device due to thicker silicon film layer.

2 II. Methodology

To study the electrical parameters on SOI MOSFET a schematic cross-sectional view of the SOI MOSFET, shown in figure 1, is simulated using Silvaco TCAD device simulator. The channel doping concentration is kept at 1×10 17 cm -3 . The source/drain region doping concentration is kept at 1×10 20 cm -3 . Gate length of the device is 1 ?m. Gate oxide (SiO 2) thickness and buried oxide thickness are 18 nm and 0.4 ?m respectively. The total device length including drain, channel and source is 3 ?m. Shockley-Read-Hall recombination, field-dependent mobility model and T impact ionization model from Selberherr [10] was used for the simulation. Newton methods is used as numeric methods for simulation.

3 III. Results and Discussion

The n-channel PDSOI and FDSOI MOSFET has been investigated in terms of electrical parameters by simulation results obtained using Silvaco TCAD simulation software. Atlas syntax is used to create SOI structures and TonyPlot is used to display simulation results.

The impact of silicon film thickness on SOI MOSFET's electrical parameters are shown in table 1. FDSOI MOSFET has thickness of silicon film below 0.1 ?m while for PDSOI it is greater than 0.15 ?m for the simulated structure [11]. The gate to source voltage needed to turn on the MOSFET is defined as threshold voltage, V th [8]. Smaller threshold voltage satisfies high performance of device with technology scaling [12]. The threshold voltage for PDSOI is above 0.68 V and for FDSOI below 0.47 V as extracted from simulation results and also shown in figure 2. So the turn on voltage of PDSOI is larger than FDSOI from the results. This is the reason for FDSOI devices consuming less power and gaining higher speed. A high on-state current(I on) is needed to increase the driving force of the device. From figure 5, it can be said that the on-state current is greater when thickness of silicon film is reduced. As threshold voltage is increased, the leakage current(I off) is decreased [14]. It can be decided that in PDSOI the leakage current is lesser but the variation is insignificant as shown in figure 6. Static power dissipation is created by leakage current when the device is not powered [15]. Static power dissipation will be small if leakage current is smaller. Thus, from the simulation results the static power dissipation of PDSOI will be smaller compared to FDSOI. It is concluded that with increase of thickness of silicon film, the threshold voltage and subthreshold slope increased on SOI MOSFET which allows a smaller operating voltages and a higher switching speed for FDSOI. PDSOI can ensure a low static power dissipation as leakage current is small. But the leakage currents are in pA (10 -12) range for both SOIs. The DIBL parameter value shows that FDSOI is less sensitive to short channel effects. Based on the results obtained, FDSOI MOSFET displays superior performance compared to PDSOI MOSFET because of its lesser threshold voltage, steeper subthreshold slope, high on-state current and improved DIBL value in the device.

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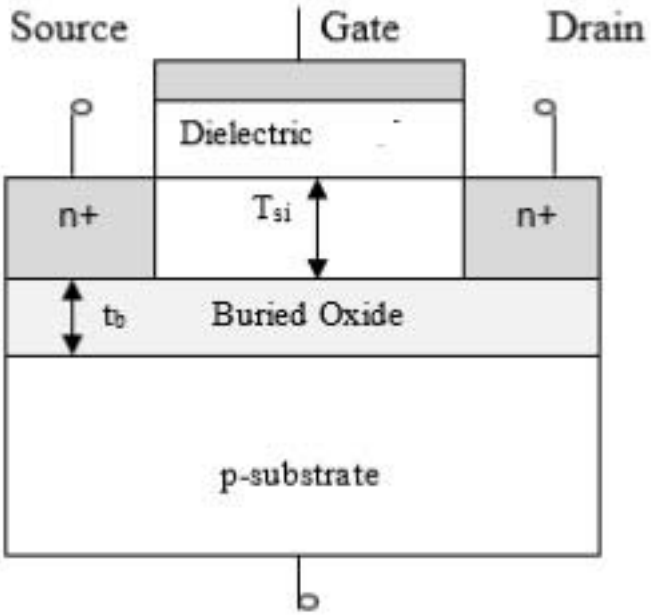

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Figure 1: Figure 1 :

SiO_2

Figure 2:

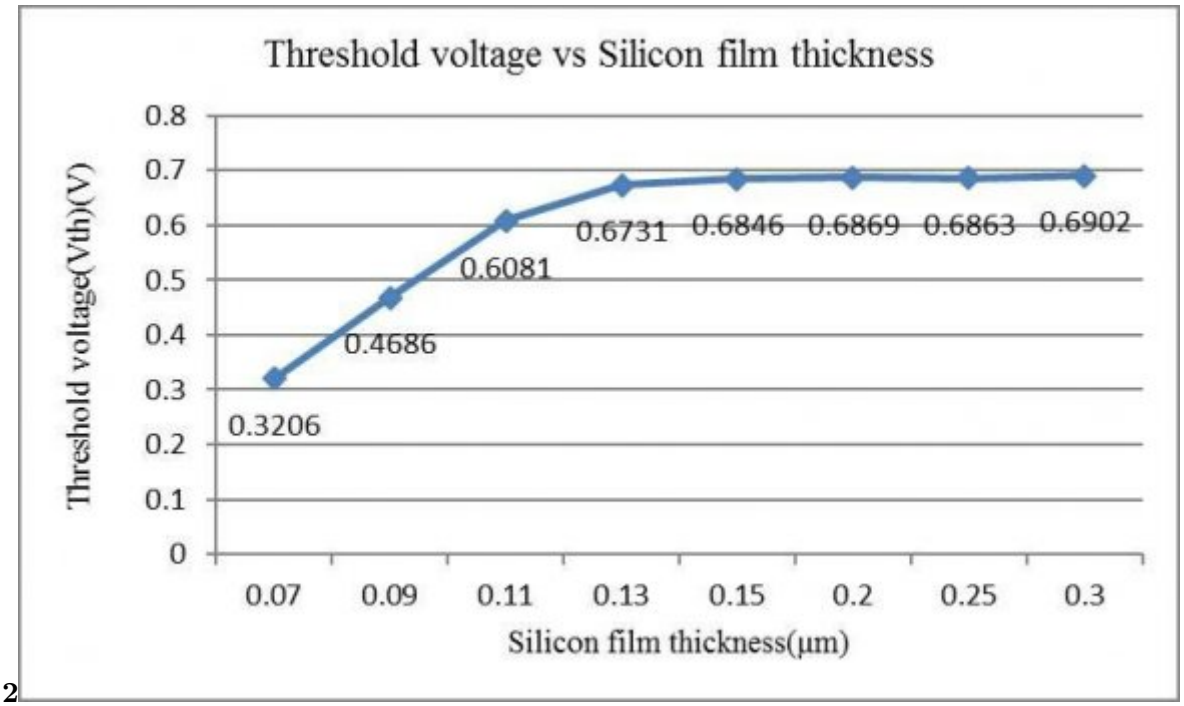

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Figure 3: Figure 2 :

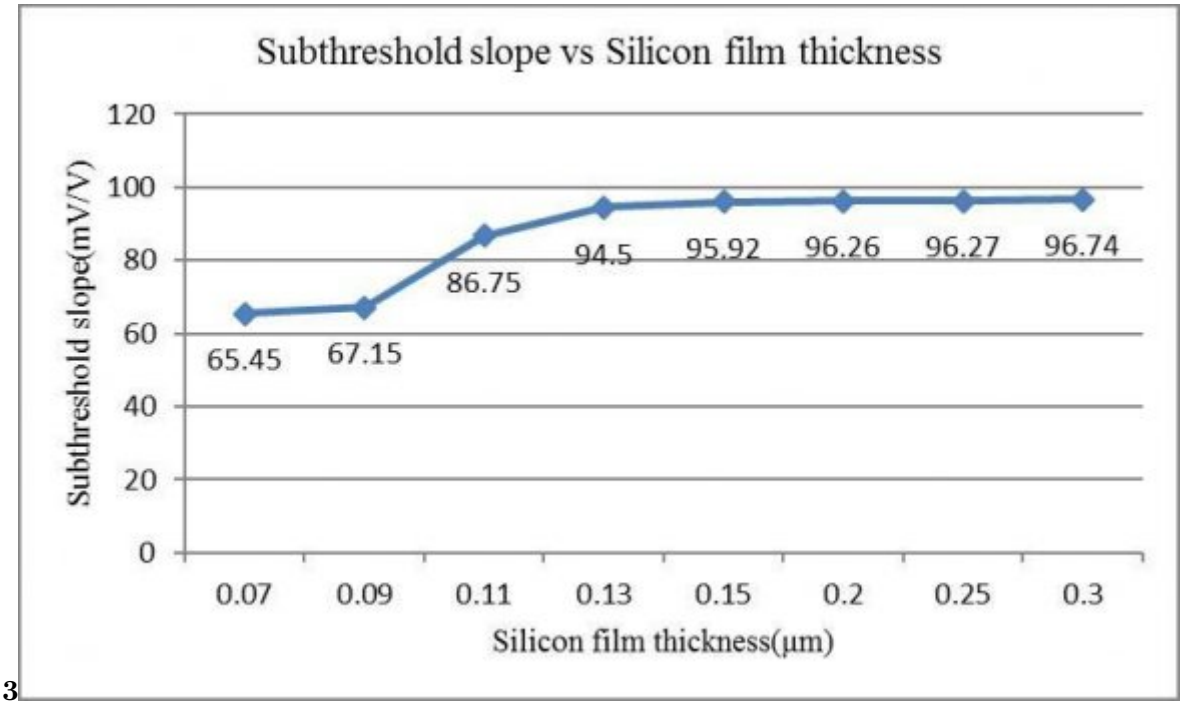

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Figure 4: Figure 3 :

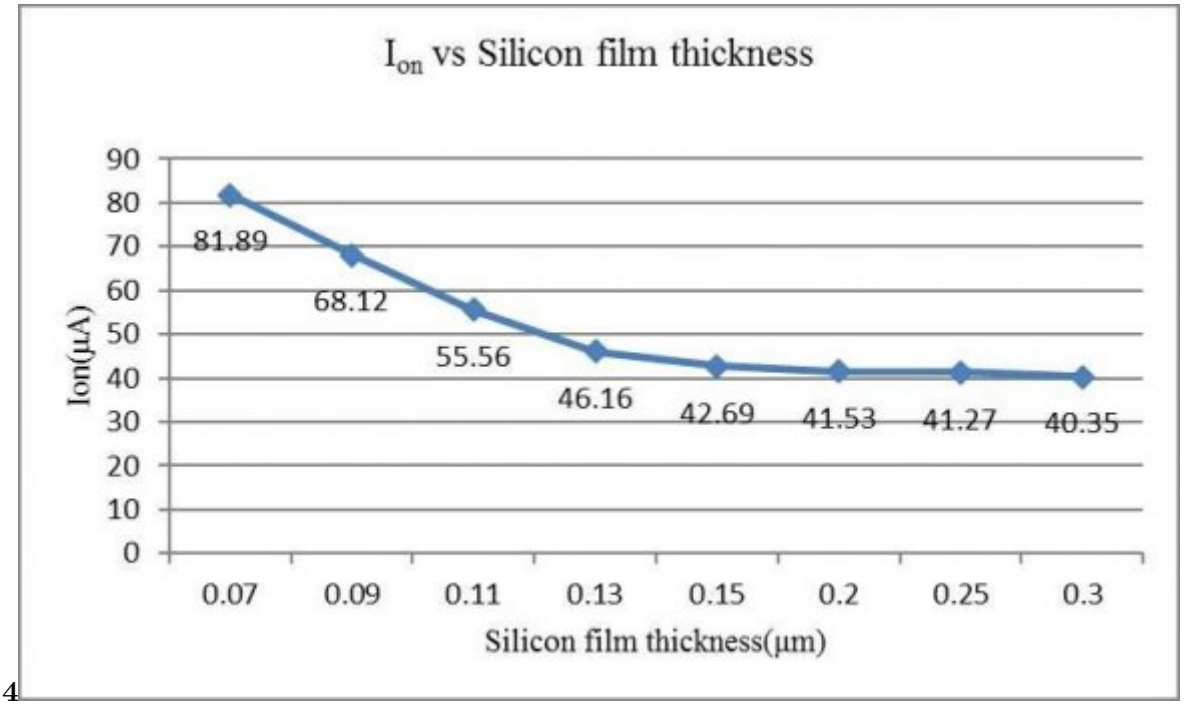

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Figure 5: Figure 4 :

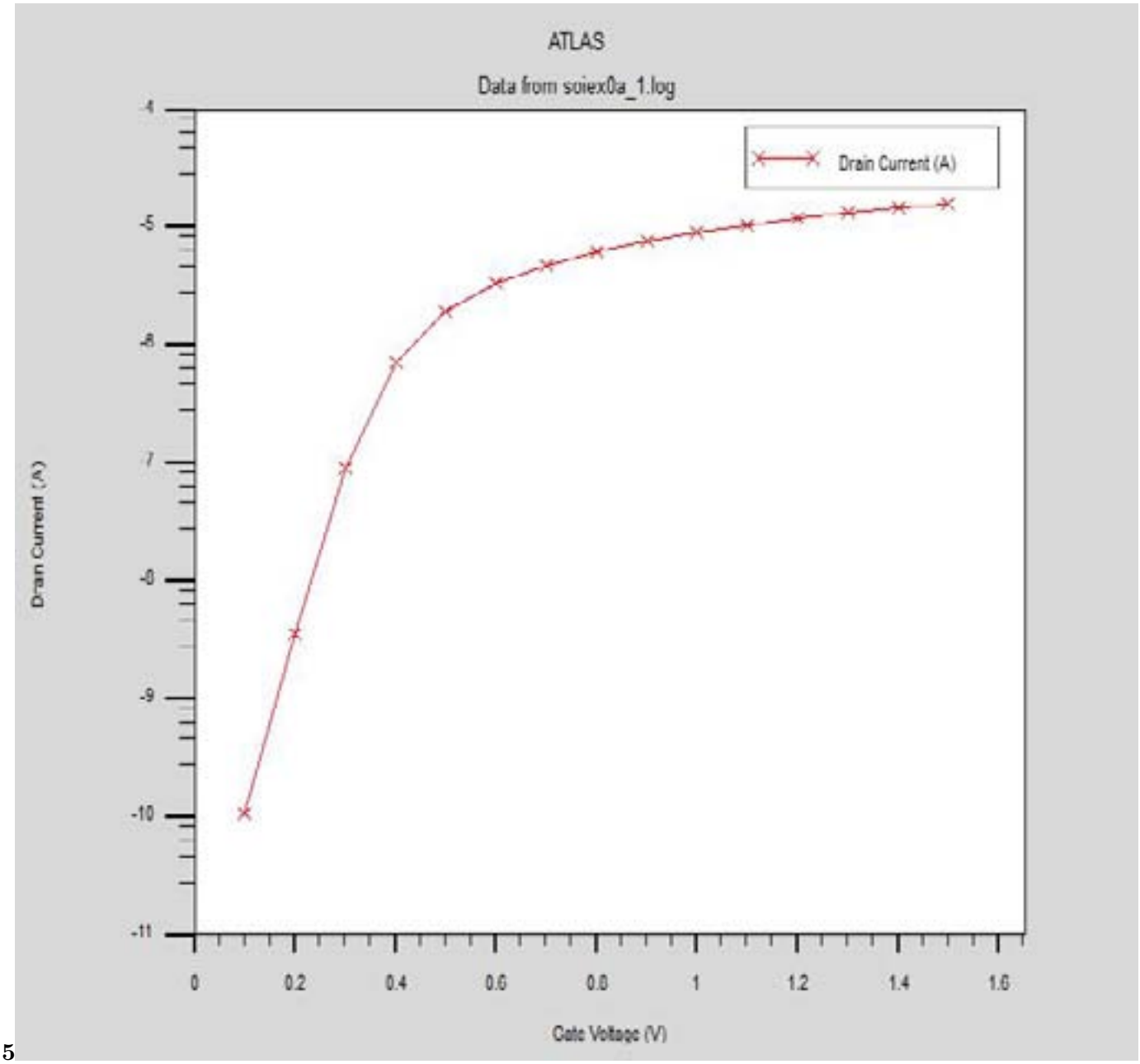

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Figure 6: Figure 5 :FD

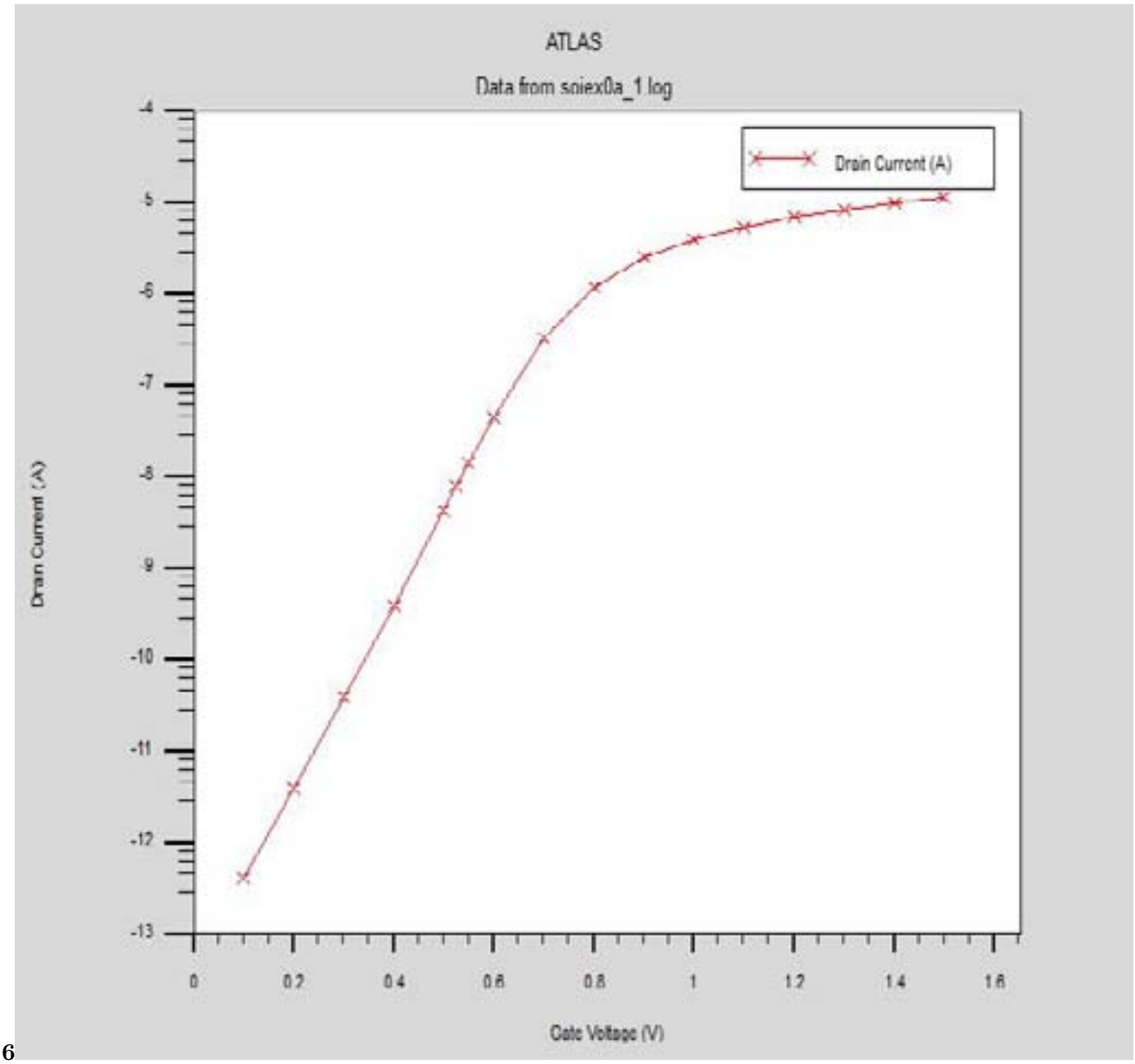

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Figure 7: Figure 6 :

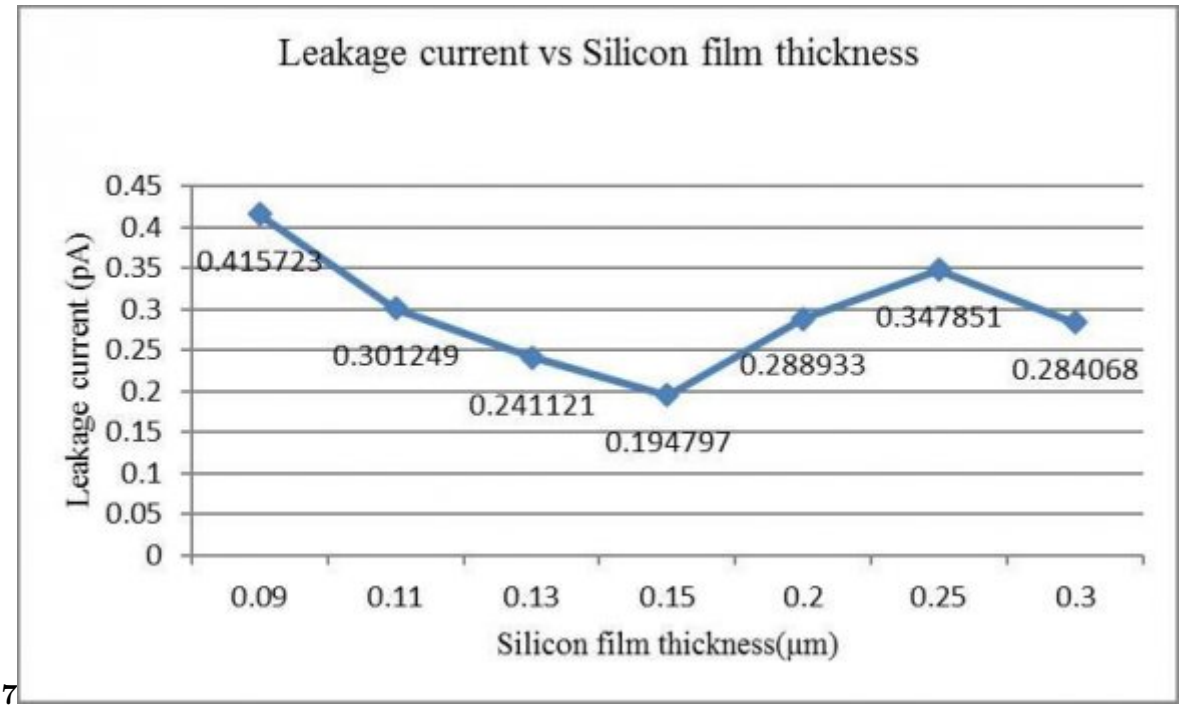

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Figure 8: Figure 7 :

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Silicon Film Thick-ness(?m)	Threshold Volt-age,Vth(V)	Subthreshold slope(mV/dec)	On-state current,I on (?A)	Leakage current,I off (pA)	DIBL(mV/V)
0.07	0.3206	65.45	81.89	12.42	74.84
0.09	0.4686	67.15	68.12	0.415723	113.34
0.11	0.6081	86.75	55.56	0.301249	166.66
0.13	0.6731	94.5	46.16	0.241121	178.18
0.15	0.6846	95.92	42.69	0.194797	180.73
0.20	0.6869	96.26	41.53	0.288933	179.56
0.25	0.6863	96.27	41.27	0.347851	177.83
0.30	0.6902	96.74	40.35	0.284068	175.69

Figure 9: Table 1 :

.1 Conflict of Interest

The author declares that there is no conflict of interest.

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