FPGA-Based Multi-Channel A/D Converter by Optimal Duty-Cycle Modulation Technique

Tchitnga Robert

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Abstract

In this article, we present the multichannel architecture of the analog-to-digital converter based on the duty cycle modulation technique with prototyping on FPGA hardware targets. This diagram is the continuation of the work presented in [1],[2] proving the feasibility of the single-channel version of this converter on the one hand and its characterization on the other. This conversion approach is based on the use of parallel duty cycle modulation cells, each used as an independent 1-bit interfacing circuit per analog channel. In addition, all of the modulated output bits associated with all of the analog inputs are simultaneously sampled and processed. The principle already demonstrated [11] and the important properties revealed by this A / D conversion scheme studied in depth in the review articles are presented, then, an experiment with a 4-channel virtual oscilloscope is presented, in order to show the potential results of the prototype of the multi-channel version of the FPGA-based converter. The design and implementation are carried out by software and hardware co-simulation using platforms such as the Simulink / Xilinx based system generators in which the ODCM-ADC is implemented, and the programming tool Vivado 2019.2 from Xilinx. The hardware platform consists of the Zynq 7000 FPGA kit (25 MHz sample clock), equipped with an integrated FPGA-based IIR (infinite impulse response) digital decimation filter and a JTAG communication cable / connectors on PC. The co-simulation systems are built and successfully tested for a modulating bandwidth of 3 KHz. These performance levels, obtained under virtual and hardware co-simulation conditions, show a relevant challenge of an oversampling multichannel ADC, compared to most ADC oversampling techniques. As a merit, the proposed FPGA-based ADC technique is a novel and relevant ADC architecture for on-board instrumentation systems and industrial electronics.

Index terms— analog-to-digital converster, optimal dutycycle modulation, iir decimation filter, FPGA, JTAG communication.

1 INTRODUCTION

ultichannel analog-to-digital converters (ADCs) are necessary in a context of digital processing of signals coming from several sensors or sources given that nature is essentially analog through its manifestations which can be images, sound, vibrations. The great power of digital computers has revolutionized the fields of industrial instrumentation and systems engineering through analog-to-digital converters which combine the role of interface between the analog world and the computer. Many applications require the digitization of signals from current output sensors, such as photo sensors and photodiodes, and in multichannel conversion systems lower power per channel is important so that as the number of channels increases, the power does not increase. not increase drastically [3], [4]. Thus, the possibility of directly digitizing the currents without current-to-voltage conversion saves the energy, the surface area and the design time necessary for the implementation of the converters. The main objective of this article is to study and implement on FPGA and test an optimal multichannel cyclic

cycle modulation ADC. This circuit provides an interface to analog sensors and minimizes the dynamic range dependence of the conventional oversampling ADC on the supply voltage. The following sections explain the history, background, of the duty cycle modulation technique.

Fig. **??**: Oversampling ADC principle [1] In Section II, the knowledge on the DCM-based ADC topology is outlined. Then, a case study and prototyping multi-channel A/D converter is presented in Section III, followed in Section IV by the hadware cosimulation results. Then, the conclusion of the paper is presented in Section V. The block diagram of our multi-channel ODCM-ADC is inspired by the single-channel converter taken from [2], and is shown in Fig. **??**. It consists of two main parts, connected in tandem, that is to say an optimal upstream DCM circuit (see Fig. 2 (a)) with modulating input x and DCM output xm (t), and an optimal downstream digital filter IIR (Infinite Impulse Response) (see Fig. 2 (b)). The optimal DCM demodulator circuit is modeled by a set of nonlinear parameters which form a constrained optimization problem, while the optimal IIR filter is synthesized according to the specifications of the weighted pth standard. The optimal parameters of multichannel ADC system prototyping based on optimal duty cycle modulation considered in this section are taken from previous work [] namely: fs = 25MHz (sampling period or Ts = 1 / fs = 40 ns so equivalent), fs = 3KHz (modulating bandwidth), fm (0) = 172 KHz (DCM base oversampling frequency), E = 9 volts (power), * = 0.012366816265686 where ? * = R1 / (R1 + R2) and RC = 0.000115510618677 s. It should be remembered from [1] that the DCM circuit shown in Fig. 2 is modeled by equation (1), which is quite easy to implement in the Matlab / Simulink framework. In addition, the transfer function z of the second-order optimal digital IIR decimation filter is given by (2).

2 II. RECALL OF ODCM-ADC ARCHITECTURE

( ) ? + + = ? < ? = + ? ? ? ? ? = ? = ? + ? ? ? ? ?**(1)**

F 0 (z) = b2 z 2 + b1 z + b0 z 2 +a1 z + a0 wit h b2=8.263545624646787 e ?08 b1=1.652709124929357 e?07 b0=8.263545624646787 e?08 a1= ?1.999777875893610 a0=0.9997782064354348

(2)

3 III. FPGA-BASED OF MULTI-CHANNEL ODCM-ADC DESIGN

The FPGA-Based multichannel ODCM-ADC design is conducted under Simulink workspace, according to the schematic diagram presented in Fig. **??**. The upstream subsystem shown in Fig. 3(c). As in the case of single input ODCM or sigma-delta A/D converters ([1], [2]), an important problem to take into account when sampling a discrete sequence given by "Eq. 3", is the over sampling phenomenon [10] It is due to the fact that theanalog original version of "Eq. 3" is a time varying square wave, with a wider bandwidth compared tothat of the modulating wavex(t) encapsulated in R m (x(t)). (2R m (x, ?) ? 1)E + 4E ? ? sin ? n ? R m (x,?) n ? cos 2? n t T m (x) ? n=1

Thus, the sampling theorem used in digital signal processing [1],is applicable in this case to the target modulated wave x m (t) to be sampled. Let fosc (x j t))(being the fundamental frequency of the oscillator associated with the jth channel, its maximum value fosc max which occurs for xj(t) =0, is assumed tobe an identical constant for all channels, in which case the bandwidth f max related to the periodic square wave is large enough compared to f max [9]. Thus, assuming that the admissible bandwidth of the jth analog signal xj(t) is a constant fBj, then the following constraint should be satisfied when choosing the simultaneous sampling frequency fs ,? ? ? ? ? ð ??"ð ??" ?????? (0, ?) = 1 2.??.ln ? ?? +1 1??? 1 ? ð ??"ð ??" ?????? (x max , ?) = 1 ??.ln (?((1???)x max) 2 ?((?? +1)??) 2 ? ?((1???)x max) 2 ?((?? ?1)??) 2 ? (4)

Fig. 3(a) is a Simulink-based model of the DCM circuit given by (1), with analog modulating input Xs ? x as in Fig. 2(a), and with a sampled modulation output xm. Then, the downstream subsystem presented in Fig. 2(b) is modelled as a digital IIR filter given by (2), which is implemented using visual building resources and configuration panels available in Xilinx System generator frame work. The IIR filter is implemented according to the direct form approach. The implemented only required 5multipliers, 5 registers and an added tree, although the full resolution is maintained across the multipliers and the tree. In addition, the data width cannot grow indefinitely, and thus a quantization block is placed at the output of the adder to reduce the width of the data. At this step, it is worth noting that the whole schematic diagrams presented in Fig 2, is tested over the modulating band width followed by the creation and the configuration of an additional hwcosimblock for further hardware co-simulation requirements. In addition, the DSP code for the target FPGA is generated as an input module for XilinxISE framework. As an implication the related high level RTL diagram shown in Fig. **??**, is organized into 9 digital processing modules.

4 a) Virtual Simulation of the multichannel ODCM-Based

ADC System Following (2), the ODCM-based ADC system, designed in depth in this section, has been implemented in Simulink framework as shown in the virtual model (see Fig. **??**). It consists of a visual model of the optimal DCM block as shown in Fig. **??** (a), corresponding to the first order dynamic model(2), and a discrete transfer function F(z) of the optimal second order digital IIR filter.

The simulation required for performance evaluation of the overall prototyping ODCM-based ADC, is conducted over a sufficiently wide range of frequency including the modulating bandwidth of 3 KHz. In addition, a sample of detailed result related to a sine modulating input (1 KHz, 100Hz, 1.5kHz, 2kHz, 1 Vpp) is presented in Fig. **??**, whereas all results of hardware cosimulation obtained under variable modulating frequencies are summarized in Fig. **??** [5].

5 b) Design chart of a multichannel ODCM-ADC based on FPGA

The design workflow for an FPGA application is usually done in several stages. First of all, algorithmic specifications make it possible to define the architecture by an algorithm-architecture fit approach. This architecture is then described with the HDL language. You can then simulate the system and modify it if necessary [2]. Then come the phases of synthesis and routing placement, which consist in determining which elements will actually be used in the FPGA and how they will be connected to each other, where in the component they will be placed, etc. Each phase requires verification of the correct timing and, if necessary, modifications.

The hardware description language such as VHDL or Verilog, usually used for the development of FPGAs, are of a concurrent nature. Programming in VHDL implies a good knowledge not only of the algorithm but also of the FPGA and the compiler used [2]. To better exploit the intrinsic parallelism of the algorithm, it is necessary to perform the processing tasks in parallel (non-sequential) to satisfy the time constraints. For most control or signal processing specialists who are very often software researchers and engineers, these hardware languages are unfamiliar and sometimes difficult to use. This is probably one of the reasons holding back the democratization of FPGA technology. In an attempt to provide an appropriate solution to this problem, co-design platforms by association of several development environments have been proposed. The general System Generator/Silulink chart is schown in figure 3.

6 HARDWARE CO-SIMULATION OF MULTICHANNEL ODCM-ADC

Co-design is the design technique of the day for its many advantages so one can co-use MATLAB / Simulink software and System Generator building blocks to implement SISO downlink chip systems. or to propose a design of QPSK modulator on FPGA which consumes little power and using the hardware cosimulation, to obtain a reduction in the cost of the hardware requirements.

As part of this work, the development of the converter prototype is carried out with the XSG software. This is a toolkit developed by Xilinx to be integrated into the Matlab/Simulink environment and which lets the user create highly parallel systems for FPGAs. The created models are displayed as blocks, and can be linked to other blocks and to other Matlab-Simulink toolkits such as SPS. Once the system is complete, the VHDL code generated by the XSG tool exactly reproduces the behavior observed in Matlab. For rapid prototyping, the choice of this tool is easily explained. As the conversion system needs to be checked and simulated often and quickly throughout development, it is much easier to analyze the results with Matlab than with the tools usually associated with VHDL, such as Modelsim [6], [7]. When the prototype is up and running, the switch to the hardware platform for field testing is rapid, making validation of the prototype a feasible project in the short term. The PC and the FPGA board are connected via a suitable communication cable/connectors (USB, Ethernet or JTAG). Thus, in a hardware co-simulation context, the digital signals involved in a DSP/FPGA chip are automatically uploaded to the PC-based virtual platform for real-time visualization. During a cosimulation session, the virtual simulator and the hardware DSP are simultaneously started and driven under the same operating conditions (input and parameters), while the real-time behavior of the hardware DSP is brought to the virtual simulation environment for rapid design, visualization and performance evaluation [8]. The co-simulation environment created in this research work for the rapid computation and evaluation of the predicted and experimental characteristics of multi-channel ODCM-ADC prototyping based on FPGA, is presented in Fig. **??** Figure **??**: FPGA-Based ODCM-ADC design architecture [2] Figure **??**: Hardware Co-Simulation environment Finally, a summary of simulation results obtained are presented in Fig. 7.

The results presented here show that, the proposed multichannel ODCM-based ADC offers high performance within 3 KHz of modulating bandwidth. The high level of predicted performance obtained from virtual simulation of a prototyping system, is a great challenge an oversampling ADC topology, consisting of a piece of ODCM circuit with impressive properties, and a single stage of optimal 2 nd order digital decimation filter. The figure above shows the converter model produced in Matlab's Simulink environment. The modulator is realized in Simulink while the second order RII filter is realized together in simulink for virtual simulation. For the software co-simulation, the blocks of the Xilinx System Generator toolbox were used. A successful simulation in the System Generator environment generates the hardware co-design block that allows the Matlab/Simulinx environment to interact with the Zynq 7000 board. The filter will be implemented using the 4x4Filter block from Xilinx . The 4x4Filter block is a 4x4 mask that scans four lines of the input signal at a time to apply the chosen filter. Therefore, the system requires a buffer that accepts four lines of inputs at a time to be fed into the filter. Figure **??** is the model which shows how to design for the assembly.

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8 CONCLUSION

This research was carried out in phases. First, the use of a filtering block with an input multiplexer and an output demultiplexer was studied, then 4x4 filtering blocks were studied. A unique way has been identified to incorporate these design techniques into the existing analog-to-digital converter so that the advantages of this mode of circuit design can be used to overcome some existing problems in the multi-channel architecture. The applications of this architecture are then defined. The sub-blocks of the architecture have been defined and designed according to the required specifications. The design and co-simulation have been successfully implemented on the Xilinx ZYNQ 7000 FPGA hardware target. It should be noted that the analog-to-digital converter thus produced based owes its low cost of implementation and its high quality (stability, precision and robustness) both to the material simplicity and to the topological relevance of its DCM circuit. interfacing. As a major discovery, the FPGA-based multichannel ODCM-ADC presented in this article, could be used as a potential new architectural solution for on-board instrumentation systems. [1] [2] [3]

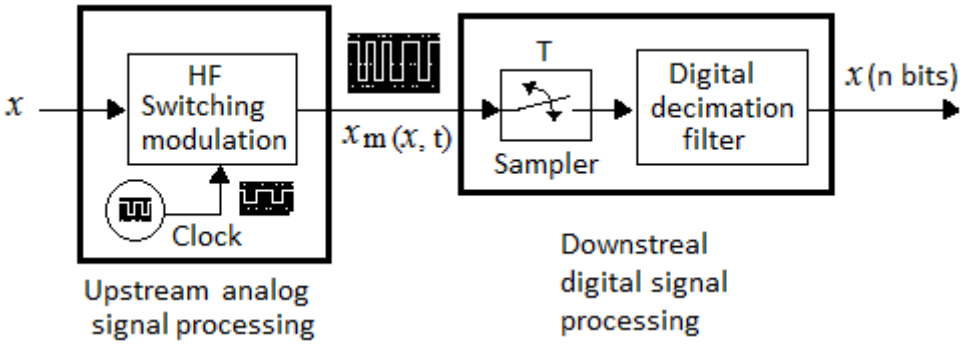

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Figure 1: Fig. 2 :

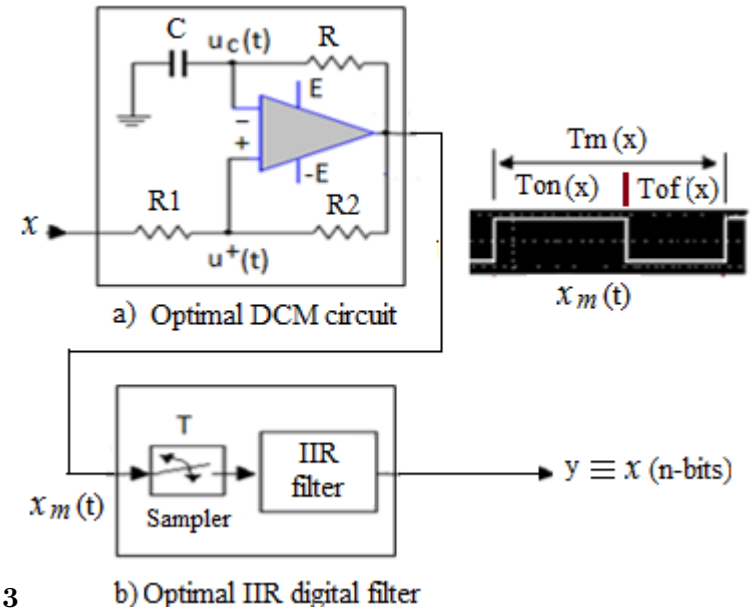

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Figure 2: Figure 3 :

[1] FPGA-Based Multi-Channel A/D Converter by Optimal Duty-Cycle Modulation Technique (3) © 2022 Global Journals

[2] FPGA-Based Multi-Channel A/D Converter by Optimal Duty-Cycle Modulation Technique

[3] © 2022 Global Journals

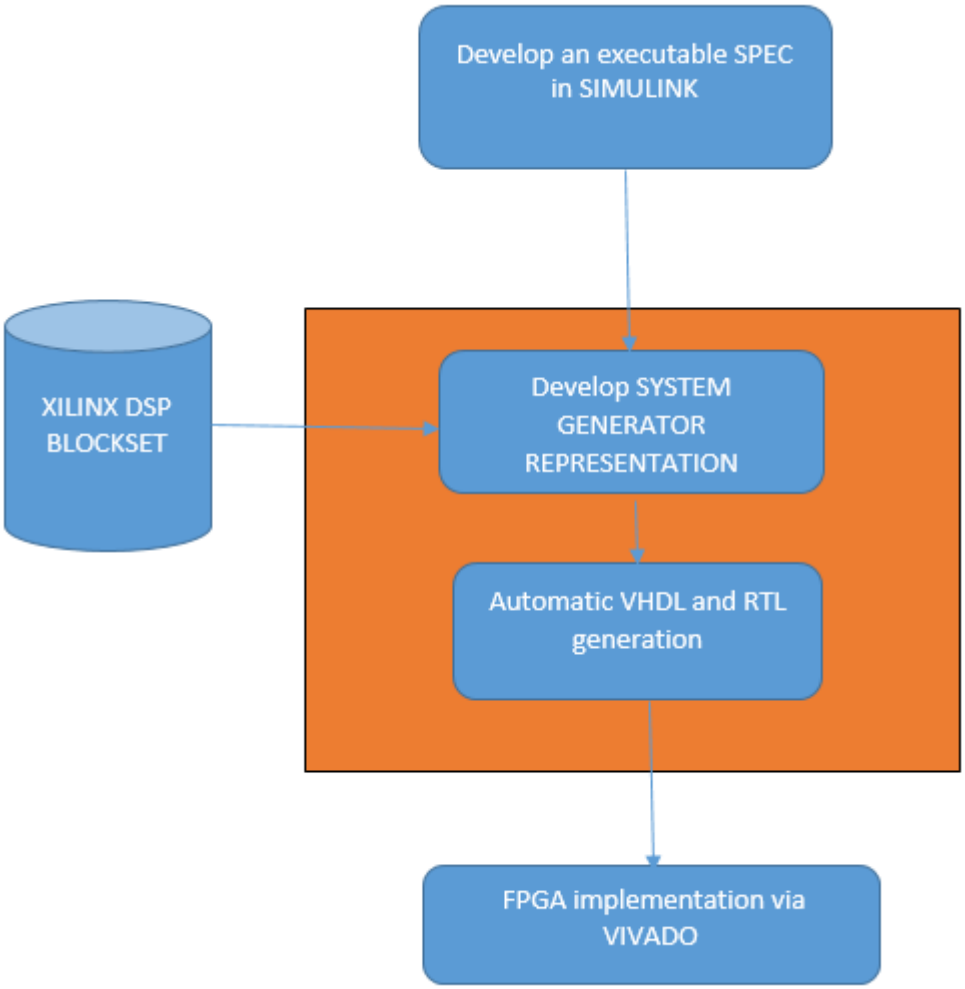
Develop an executable SPEC in SIMULINK
XILINX DSP BLOCKSET
Develop SYSTEM GENERATOR REPRESENTATION
Automatic VHDL and RTL generation
FPGA implementation via VIVADO

Figure 3:

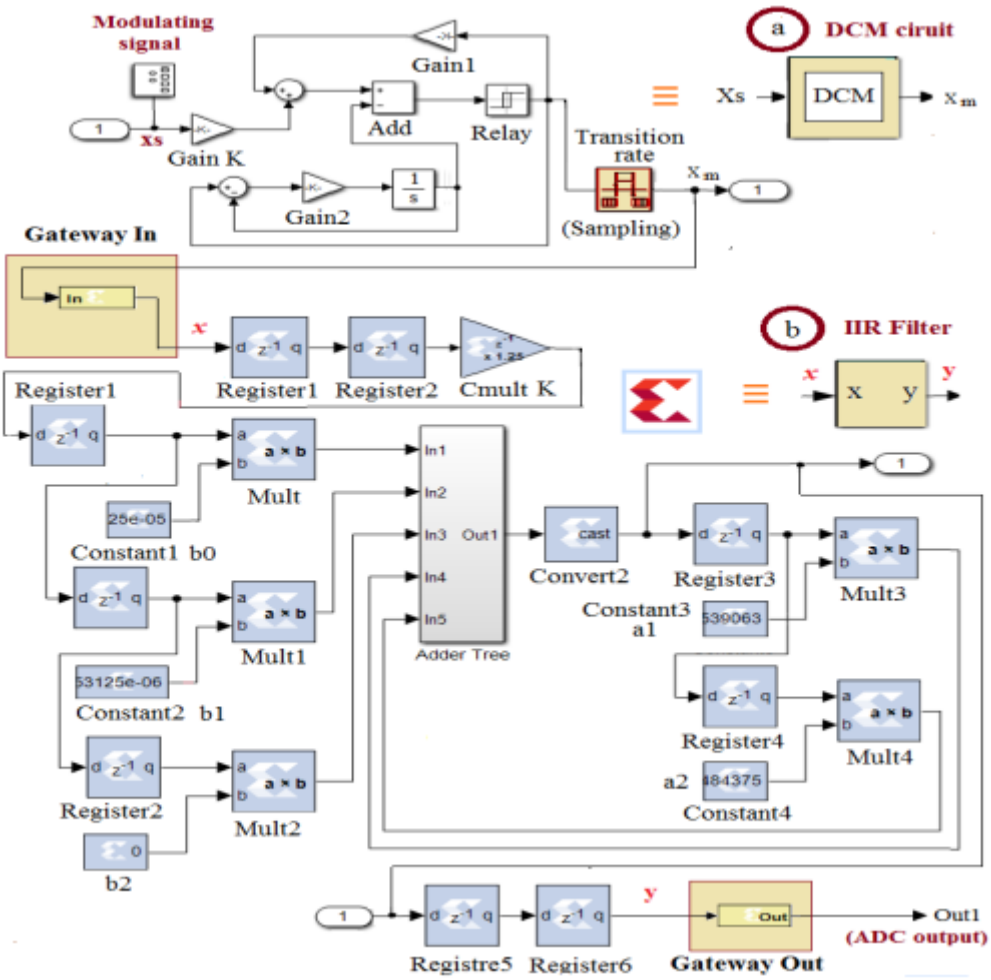

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Figure 4: Figure 6 :

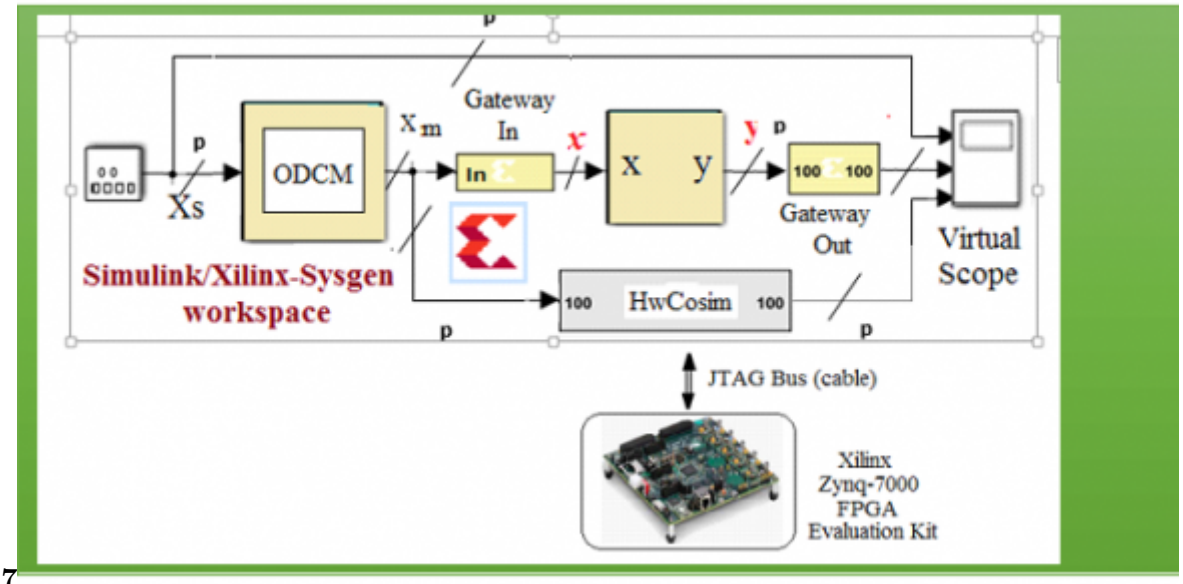

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Figure 5: Figure 7 :

[Mbihi et al. ()] 'A novel analog-to-digital conversion technique using nonlinear duty-cycle modulation'. J Mbihi , F Ndjali Beng , M Kom , Nneme Nneme , L . *International Journal of electronics and computer science engineering* 2012. 1 (3) p. .

[Lonla et al. ()] 'A Novel Digital-to-Analog Conversion Technique using Duty-Cycle Modulation'. Moffo Lonla , B Mbihi , J Nneme Nneme , L Kom , M . *International Journal of Circuits* 2013. 7 (1) p. . (Systems and Signal processing)

[Inose et al. (1962)] 'A telemetering system by code modulation, deltasigma modulation'. H Inose , Y Yasuda , J Marakami . *IRE Trans. on Space, Electronics and Telemetry* Sept 1962. (8) p. .

[Doley and Kornfeld ()] 'Comparison of Sigma-Delta converter circuit architectures in digital CMOS technology'. N Doley , A Kornfeld . © *World scientific publishing company* 2005. 14 (3) p. . (systems ans computers)

[Sonfack and Mbihi ()] 'FPGA-Based Analog-to-Digital Conversion via Optimal Duty-Cycle Modulation'. G B Sonfack , J Mbihi . *Journal of Electrical and Electronic Engineering* 2018. 8 (2) p. . (JEEE)

[Lonla and Mbihi ()] 'Low Cost and High Quality Duty-Cycle Modulation Scheme and Applications'. Moffo Lonla , B , Jean Mbihi . *Computer, Energetic, Electronic and communication Engineering* 2014. 8 (3) p. . (International Journal of Electrical)

[Nneme and Mbihi ()] 'Modeling and Simulation of a New Duty-Cycle Modulation Scheme for Signal Transmission System'. Nneme Nneme , L Mbihi , J . *American Journal of Electrical and Electronic Engineering (AJEEE)* 2014. 2 (3) p. 82.

[Mbihi et al. ()] 'Modelling and simulations of a class of duty cycle modulators for industrial instrumentation'. J Mbihi , B Ndjali , M Mbouenda . *Iranian J.Electr. Comput. Eng* 2005. 4 (2) p. .

[Lonla and Mbihi (2016)] *Nouvelle technique de coversion N/A des signaux par modulation numérique en rapport cyclique et applications en instrumentation virtuelle*, Moffo Lonla , B Mbihi , J . July 2016. ENSET, University of Douala (Ph/D thesis)

[Moffolonla and Mbihi ()] 'Novel Digital Duty-Cycle Modulation Scheme for FPGA-Based Digital-to-Analog Conversion'. B Moffolonla , J A Mbihi . *IEEE Transaction on circuits and system II* 2015. 62 (6) p. .

[Sonfack et al. ()] 'Optimal Duty-Cycle Modulation Scheme for Analog-To-Digital Conversion Systems'. G Sonfack , J Mbihi , L B Moffo . *World Academy of Science, Engineering and Technology* 2017. 11 (3) .