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Myths, Misconceptions and Mistakes in the Electrostatic Protection of Field-Sensitive Items -Why it's Time to Re-Visit Device Protection

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Abstract

The measures currently being taken to prevent electrostatic damage in semiconductor manufacturing environments are not sufficient to guarantee the complete protection of items that are highly sensitive to electric field. Mistakes that have been made in the interpretation of electrostatic damage phenomena in manufacturing and errors that have been made in attempting to provide protection against them are described. It is shown that some of the ESD countermeasures in widespread use today can actually increase the electrostatic risk for fieldsensitive items. The static dissipative materials that are commonly used to make pods and transport boxes are shown to expose field-sensitive items to a significant risk that can result in cumulative and permanent damage. It is concluded that more research into semiconductor device electrostatic damage mechanisms other than ESD is urgently needed, as has previously been called for by researchers studying the problem. It is also recommended that the electrostatic countermeasures being used in device manufacturing and handling should be reviewed and revised where necessary, to improve the protection of all extremely-electrostaticsensitive (EES) items.

Index terms—

1 Introduction

f one asks any electrostatics expert working in the semiconductor industry about what must be done to eliminate electrostatic risk, the response will probably center on ESD and how to prevent it. This leads to discussion about the causes of ESD, which are primarily; a) the generation and accumulation of electric charge, and b) the bringing together of objects having a different charge balance during handling or processing. It follows logically that ESD prevention involves avoiding a) and b). First one must identify where such risk exists, then one must find a way to either counter or remove it.

Charge accumulation is most easily indicated by measuring the voltage of an object, and this is usually done with a high impedance voltmeter for conductive objects, or a hand-held field meter to measure the electric field emanating from insulating objects. In more detailed electrostatic investigations and factory audits, the level of excess charge held on an object may be measured directly with a coulomb meter or Faraday cup, the purpose of which is to estimate the current that is likely to flow in any discharge event and hence assess the risk of serious damage being caused by a discharge. This approach to risk assessment is embodied in SEMI Standard E78, "Guide to assess and control electrostatic discharge (ESD) and electrostatic attraction (ESA) for equipment" [1] and SEMI Standard E129 "Guide to assess and control electrostatic charge in a semiconductor manufacturing facility" [2] which are just two of many such guides that have been published.

It is necessary to have such standardized approaches to assessing electrostatic risk to ensure that different manufacturing sites can be assessed for electrostatic safety in a comparable way by different personnel, thus ensuring consistency throughout the supply chain. Electrostatic compatibility assessments are also carried out to qualify the production equipment that is to be used for making different generations of semiconductor devices,

and each year the voltages and level of charge that are permitted within the manufacturing environment are reduced in line with the shrinking feature sizes of each production "node". Users expect that the certification of a piece of manufacturing equipment to the levels defined in an industry standard gives them assurance of the electrostatic safety of that equipment.

For a manufacturing site manager, receiving a pass result in an electrostatics audit is probably more important than understanding the nature of the electrostatic risks present in the facility. What the site manager needs is confirmation from an expert authority that it is safe to carry on production, which is why audits carried out by electrostatics consultants are extensively relied upon. The rationale behind this is that the person conducting the audit fully understands all the risks, and that those risks are being properly assessed in the tests being carried out.

Unfortunately, that is not always true [3] and the use of standardized approaches to risk assessment for certification purposes, whereby auditors focus on taking prescribed measurements and filling in forms to generate a pass or fail result, can risk them overlooking the diversity of electrostatic risks that may be present. Errors made in understanding the risks that are identified can also lead to ineffective or incorrect treatment, with the consequence that further unidentified risks can still be present.

The following sections identify some of the risks that can be missed in conventional electrostatic audits, some of the mistakes that have been made in defining 'safe' handling practices for electrostatic sensitive objects, and some of the errors present in equipment designs and installations. Illustrations are given using reticles as a primary example (or with data from sensor devices developed specifically to study reticle handling risk) because reticles are extremely field-sensitive, they have been studied extensively and they provide clear illustrations of the risk created by electric field, which is invisible and can be difficult to measure electronically. The use of reticles and reticle-related data for these examples does not mean that the characteristics being discussed are restricted to reticles -these are simply presented as examples of how electric fields can behave -so for "reticle" read "any field-sensitive object". Electrostatics operate in the same way with everything.

2 II.

3 Limitations of some Electrostatic

Risk Assessment Methods a) Charge accumulation Methods for evaluating the electrostatic safety of a piece of production equipment are described in SEMI Standard E78. One of the tests involves measuring the amount of static charge present on a wafer or reticle as it leaves the equipment's load port. This risk assessment method assumes that the amount of charge found on the wafer or reticle when presented at the load port would indicate the likelihood of electrostatic damage being caused to it by the equipment, or by its subsequent handling. This is not necessarily true, however. If a wafer or reticle's insulating surface becomes charged within a piece of equipment, subsequent grounding of the reticle's conductive film or the wafer substrate during handling can result in the attraction of a balancing charge onto it from ground.

A hypothetical scenario is illustrated schematically in Fig **??**, wherein a vacuum gripper contacts the upper surface of a reticle to move it. In accordance with the established practice in the semiconductor industry, the reticle support points at the hand-off position are made from grounded static dissipative material. A balancing charge would be drawn onto the conductive part of the reticle from ground through the support points, attracted by the static charge on the upper surface created by the vacuum gripper. An electric field would then be present between the two opposite charges on the reticle and this could induce damage in the reticle's pattern area.

However, if a reticle in this condition were removed from the equipment and the amount of charge it carries at the load port measured using a Faraday cup, the result would be close to zero because the static charge had been balanced by grounding the reticle inside the equipment. The equipment would pass the E78 safety assessment and hence be considered "safe" -despite the fact that reticles could be damaged while inside it.

Fig. **??**: Charging of a reticle within a piece of equipment (or an insulating layer on a wafer, which could also result from a processing operation) followed by the addition of a balancing charge to a conductive part by a grounded handling tool. On removal from the equipment a measurement of the charge held on the tested item, as defined in SEMI Standard E78, would measure little or no net charge, incorrectly indicating the 'safety' of the equipment.

A similar situation could arise in wafer handling, if a processing operation charged an insulating layer on the upper surface of the wafer and the substrate was grounded through an equipotential bonding scheme being used on the material handling system.

Other risks than those caused by the charging of a sensitive item with static electricity can occur inside equipment. Electrostatic damage to reticles has been shown to occur through field induction even when there is no charge transfer to or from the reticle. A reticle can suffer ESD damage through exposure to an electric field while remaining electrically neutral -the reticle does not even have to be touched for damage to occur. This is the predominant electrostatic risk for reticles during normal use. It is described and guidance for avoiding it is given in SEMI Standard E163 [4]. The risk to a reticle from field induction cannot be assessed by measuring the charge the reticle holds at a load port, it is better assessed by using a specially configured sensor device [5] that can go where a reticle goes inside the tool and can record the electric field conditions that a normal reticle would experience. Examples of this will be shown.

4 b) Tribo-charging of carriers

Technical errors have been made in attempting to reduce the electrostatic risk to reticles caused by the tribo-charging of reticle pods and storage boxes during manual handling. When the first single-reticle boxes were made they were molded from insulating plastic such as polycarbonate, which has the advantage of being crystal clear so the reticle inside can be identified without opening the box. It was subsequently found that handling of the boxes could tribo-charge them to a very high voltage (up to 50kV) and when they were opened on a piece of equipment to remove the reticle, the electric field became concentrated between the charged box and the grounded load port, passing directly through the reticle and causing ESD damage. Alternative materials were sought that would not tribocharge to the same extent, and modifications were attempted to try and improve the performance of existing pods (which will be described later).

Investigations into the suitability of alternative materials for making reticle pods measured how much they would be charged by handling, which was done by performing a "wipe test". In this test, a sample of the material under investigation is rubbed vigorously with either a cloth or a cleanroom glove, and the degree of tribocharging is then determined by measuring the electric field the material generates, as described in SEMI Standard E43 [6]. Static dissipative plastic materials were found not to exhibit persistent electric fields when tested in this way, so it was decided to make reticle pods from static dissipative rather than insulating plastic. resulted in a significant decrease in the rate of reticle ESD damage. However, changing the pod material only addressed the specific risk being caused by the pod itself first being charged by handling, then being placed onto a grounded load port or other surface. Other risks remained, and these new materials actually introduced some new risk, as will be described later.

It became a common belief, as a result of using "wipe tests" to evaluate materials for electrostatic risk in this way, that static dissipative plastics do not tribocharge. This is a dangerous misconception, since all materials can be tribocharged. What was actually being measured in a wipe test was the ability of the tested material to retain the static charge on its surface for a long time. Static charge is generated on the surface of dissipative material by friction, but the charge then spreads out across the surface, reducing the strength of the electric field it produces. If the material is grounded the excess charge is drained away within a few seconds leaving no electric field to be detected.

Typically, it would take several seconds for a field reading to be taken in a wipe test, so any field generated on a dissipative test material by tribocharging would have diminished or even disappeared by the time the readings were taken. Since a reticle can be damaged by an electric field within nanoseconds, this assessment method is not temporally sensitive enough to detect the risk that static dissipative material actually presents to a reticle. Just as with the "retained charge" test in SEMI Standard E78 giving a false impression of safety as illustrated in Fig **??**, passing a wipe test falsely indicated the electrostatic safety of static dissipative material, and incorrectly indicated its suitability for the construction of reticle pods and storage boxes. Experimental confirmation of this will be described later.

5 c) Inductive charging of ESDS items

Small but important errors are sometimes made in the assessment of electrostatic risk in manufacturing processes. One commonly made mistake is in the description of discharges that can occur when using pick-and-place equipment to remove individual die from diced wafers, to place devices into circuit boards or to insert devices and circuit boards into testing stations. It is sometimes described that when an object is handled in the presence of an electric field it becomes charged by field induction, and that if it is subsequently brought close to a grounded conductor (e.g. when placing a packaged device into a circuit board or tester) it can be discharged. An example describing CDM risk in this way is mentioned in in Chapter 3 of the Industry Council on ESD Target Levels' White Paper 2 [7], which says: This change, when introduced alongside other static-reduction measures in reticle handling areas, This is a physically incorrect description of the phenomenon. What is actually happening in such a scenario is similar to the example shown in **??**ig 1, except that in this case the charge is present on the plastic pins used to hold the board in the tester, rather than being present on the board itself. The board cannot be charged by induction as described in the white paper because it is an insulating substrate and the charged plastic pins that hold down the board are also insulating, so no charge can be transferred between the two. Rather, the electric field from the charge on the plastic pins attracts a balancing charge from ground, so that when the tester contacts the circuit board connectors through the pogo-pins, it is the transfer of this balancing charge into the circuitry -not the discharging of the inductively charged board -that causes the CDM event."A typical

This may seem like undue pedanticism to some, but correctly understanding such events and describing them accurately is essential for controlling the associated risks. The white paper makes the following observation after giving this example:

The conclusion that the board would not be charged after this process is incorrect. Only after the "discharge" has taken place through the pogo pins is it correct to say that the board has been charged by field induction. If the electrical connection to ground through the pogo pins is broken before the circuit board is removed from the electric field being generated by the charged plastic clamping pins, which is highly probable, the circuitry will retain the balancing charge that was added to it from ground. Moving the circuit board away from the charged plastic pins on the tester would leave it in a charged state, so the board could suffer another CDM (or more correctly, a "charged board") event when next connected to ground at another processing station.

It is essential when defining how to deal with the risk created by such processes to correctly identify where the excess charge is located. In the example of Fig **??** the charge on the object is on an insulating surface, so it cannot be removed by grounding the object. In this example of the inductive charging of a circuit board at a test station, the excess charge is present within the circuitry itself, so it can be removed by grounding the contact pins.

If grounding is used inappropriately as a universal way of trying to prevent objects from carrying excess charge, as it often is within the semiconductor industry, there will probably be many situations like the one shown in Fig **??**, and it is not guaranteed that all objects being treated in such a way would be undamaged by it.

The white paper includes another incorrectly assessed example, this time describing the risk from the charging of an ESD sensitive component by a vacuum cup used in a pick-and-place tool. Fig **??** The description of this risk is not completely correct. If the suction cup is an insulator, it cannot transfer a significant amount of any charge it holds to the ESDS item, because any charge it holds will be trapped on its insulating surface. It can charge the ESDS item by field induction if the ESDS item contacts a grounded conductor while it is exposed to the electric field from the charged suction cup. As in the previous example of the charging of a circuit board by a circuit tester, the ESDS item would become charged by induction when it is grounded by being inserted into the board, it would not be discharged by this step.

The most critical factor in the use of suction cups for pick-and-place operations is the ability of the suction cup to tribo-charge the object being handled, as shown in the example of Fig 1 **??** The degree of charging is dominated by the separation within the tribo-electric series of the different materials of the object and the suction cup that come into contact under pressure; it is not affected by the conductivity of the suction cup. Even metals can be tribo-charged and can tribo-charge other materials. The conductivity of the cup material only affects the time for which any excess charge that is created on its surface by tribo-charging will remain in place.

Since any tribo-charging of the ESDS item becomes permanent the moment the suction cup releases it (assuming that the part of the ESDS item "Very critical during such "closed" process steps is the fact that the problem can be overlooked very easily since the PCB is not charged before and after the process but can nevertheless be damaged during the process".

contacted by the suction cup is insulating or electrically isolated, for example the encapsulation) then the fact that the charge on the suction cup could subsequently drain away to ground after separation would not change the risk to the ESDS item created by its tribo-charging during the handling process. A field meter measurement of a conductive or static dissipative suction cup after the ESDS item has been separated from it would show no remaining electric field, but it would not indicate that no tribo-charging of the ESDS item had taken place and therefore it would not be correct to conclude that the ESDS item was safe.

The confusing effect of using grounded handling tools is difficult to appreciate in such scenarios if one is relying on field meter measurements to assess the risk. This can be appreciated by considering the following description of the use of a static dissipative suction cup to place a device into a tester socket.

The suction cup tribo-charges the upper surface of the device encapsulation due to friction between the cup and the encapsulation as the vacuum is applied and released. At the moment of separation there will be an electric field present between the two separated charges. As the suction cup retracts from the device that it has just placed in the tester, the charge on the encapsulation would attract a balancing charge into the device circuitry through the connections to the tester. On completion of the test, the device would again be picked up by the static dissipative vacuum cup, which by now would be electrically neutral. The device in the tester would contain balanced charge, so there would be little external field present to attract a balancing charge towards the device through the suction cup. The device would then be disconnected from the tester and moved to its next destination, still holding the static charge on its surface and the balancing charge within the circuitry. This second handling step would create more tribocharging of the device due to the friction between the cup and the encapsulation, so on next grounding the device a further amount of balancing charge would be drawn into it. Hence, the repeated pick-and-place steps would effectively be equivalent to the repeated rubbing that is used to generate as much static charge as possible in a "wipe test". Each handling step between equipotentialbonded stations would build up more charge, increasing the internal electric field strength between the charged encapsulation and the balancing charge drawn into the circuitry from ground. Yet because of the grounding of the device, which draws into it a balancing charge, any field measurement of a device experiencing such a handling sequence would register little or no external electric field, thereby conveying a false impression that the device was not being charged by the procedure.

6 III. Limitations of some ESD Prevention Methods

The primary focus of most electrostatics advisors working in the semiconductor industry is on ESD and its prevention. (There is also parallel activity focused on controlling electromagnetic interference, which is in part related to ESD suppression). A fundamental component of virtually all ESD and EMI reduction programs is electrical grounding, with appropriate standards being defined for the inherent conductivity and resistance to ground of all things used in the factory, from the flooring materials to equipment panels, conveyors and the clothing worn by operators. Electrostatic control has become an industry of its own within the semiconductor industry, because of its importance.

The standard approach taken to control ESD in the semiconductor industry is quite simple and easy to understand:

? Eliminate all non-essential insulators because they can accumulate static electricity ? Neutralize all essential insulators using methods such as air ionization ? Connect all conductive objects to a common electrical potential, normally ground (which is a procedure known as "equipotential bonding"). ? Personnel working within a factory are required to wear conductive clothing and to be connected to ground, either through conductive footwear or by a special grounding strap worn at a workstation. ? Workstations are required to be grounded, to have static dissipative work surfaces and to have supplementary methods of charge neutralization, such as ionized air showers. While these methods do successfully control many electrostatic-related problems in manufacturing, they are targeted specifically at ESD prevention rather than device damage prevention. An assumption behind this approach to the problem is that if you eliminate ESD by managing the conditions that cause it, devices and other electrostatic-sensitive items being handled in the controlled environment will be adequately protected. Unfortunately, that is a slightly over-simplistic view to take. Eliminating damage due to ESD achieves only partial protection.

7 a) Equipotential bonding

A brief indication of the confusion that can be caused by using equipotential bonding has already been given in the previous section. Additionally, equipotential bonding can be positively harmful if applied inappropriately, so it is essential to correctly understand the effect it is having and to only use it in an appropriate way. Using it routinely for the handling of ESDS items is not always appropriate. When reticle electrostatic damage reached epidemic proportions in the late 1990s, the described principles of ESD control were applied to reticle handling in an effort to prevent the losses. The initiative succeeded in bringing down damage rates significantly, but reticle electrostatic damage did not cease completely; some semiconductor facilities were still experiencing extremely serious reticle damage problems.

In one example reported privately to the author, damage to a particularly sensitive production reticle had caused a loss of over $1 million in scrapped inventory and reticle replacements, despite the facility being equipped with the most advanced ESD countermeasures available and having frequent electrostatic audits. Every time a damaged reticle was replaced and the production line was purged of the defective wafers that had been printed with it, within a few weeks the same damage was experienced with the replacement reticle and more inventory had to be removed from the production line and scrapped.

Research at International Sematech had already demonstrated that field induction causes electrostatic damage in reticles without any conductive ESD taking place. Through computer simulation, it had been shown that grounding a reticle to protect it against conductive ESD during handling makes it more sensitive to electric field-induced damage [7], [9]. So this indicated that the adoption of equipotential bonding for reticle handling as part of the countermeasures defined above [10] was having the opposite effect to that which had been intended. Rather than helping to protect reticles, it was making the risk of field-induced electrostatic damage worse.

In the facility described above, wherein ESD was being effectively managed but electrostatic risk had not been completely removed, the damage being caused to the reticles was impossible to associate with any particular process or handling procedure; the risk was distributed everywhere, but it was either below the level considered to be hazardous or was not detectable by the methods being used in the electrostatic audits. risk of reticle damage worse and it increases the severity indicates that field induction is a complex subject that can confound even highly experienced ESD practitioners.

It also shows that the reduction in reticle ESD damage rates had actually been achieved through a variety of other electrostatic countermeasures being taken at the same time, which had succeeded in reducing the overall electrostatic risk to a level where the effect of the error in using equipotential bonding was not observed. However, as was proven by the $1 million loss event, the remaining risk (which is made worse by the inappropriate use of equipotential bonding) can have much more serious consequences than the ESD risk that was being focused on in the electrostatic audits.

One other negative consequence of using equipotential bonding for the handling of electrostatic sensitive items is that it reduces the effectiveness of air ionization systems. Ionizers offer the only practical way of neutralizing a charged insulator in a semiconductor manufacturing environment. An ionizer injects a balanced flow of positive and negative ions into the air, then the electric field from any charged object close by will attract ions of the required polarity to achieve neutralization, while ions of the opposite polarity will be repelled. It is necessary for the electric field from a charged object to attract the required airborne ions and repel the others in order to achieve charge neutralization, but if the object is grounded through an equipotential bonding scheme as illustrated in Fig **??**, the charge it contains becomes balanced and it produces no significant electric field (other than the short-range internal field between the balanced charges it holds). Hence, by eliminating the external electric field from charged objects, equipotential bonding reduces the ability of ionizers to neutralize them. Year 2021 of any field-induced damage that does occur. This Initially, the conclusion drawn from the computer simulation study indicating the harmful effect of equipotential bonding was challenged by several electrostatics consultants who were working in the semiconductor industry, as their practical experience indicated to them that grounding is protective. This opinion seemed logical because reticle damage rates had fallen significantly after equipotential

bonding was recommended for reticle handling, and the use of equipotential bonding had been known for a long time to improve semiconductor device yields.

Nevertheless, independent experimentation carried out by several research groups confirmed the indications of the computer simulation [11], [12], demonstrating conclusively that grounding makes the . It is often said in defense of equipotential bonding that it is the only practical way of removing static charge from items being manufactured in a production environment, where speed of material handling is essential for productivity. Grounding achieves charge balance relatively quickly (orders of magnitude faster than air ionization can achieve charge neutralization) which is why it is valued so highly by equipment makers and semiconductor manufacturers alike. But, since any static charge on a typical electrostatic-sensitive object being handled in a semiconductor factory is likely to be located on an insulating part of the object, such as the encapsulation of a packaged semiconductor device, the substrate of a circuit board or an insulating layer on a wafer, it cannot be removed by grounding. Connecting any conductive part of the object to ground can only introduce a balancing charge. This results in the object holding no net charge, so there will be no ESD if it contacts another grounded conductive object, but the object is not electrically neutralized by grounding it -it is put into an energized state rather like a charged capacitor, with energy stored in the internal electric field between the separated charges. If the object contains field-sensitive structures, this internally concentrated electric field can potentially cause damage, as it certainly does to reticles.

It is important to recognize that electric fields are vectorially additive, so even if the internal electric field produced by grounding a charged device during handling is not itself sufficient to cause damage to the device, its presence during testing or when power is applied during normal use could raise the total electric field within the device to a dangerous level -so this issue should not be ignored.

The desire for speed in material handling may need to become a secondary consideration in order to prevent extremely electrostatic-sensitive items from being damaged. An example of unavoidable charging by a process, which limits the speed with which the item can be handled when using equipotential bonding, is the cleaning of a reticle. Washing with deionized water and spin drying produces a large static charge on the surface, as shown by the measurement in Fig **??**. This is a recording of electric field taken by the specially designed sensor device [5] mentioned in section 2, which has the same form factor as a normal production reticle and can pass through many of the processes that a standard production reticle would experience.

Internal field-measuring electronics continually record the electric field that the device is exposed to, then the stored data are downloaded to a computer for processing after the measurement is complete. Fig. **??**: Electric field recorded during reticle washing with deionized water followed by spin drying. Ionization to neutralize the reticle is essential after such a process, preventing the reticle from being moved until the static charge has been eliminated.

The static charge generated on the reticle by the process cannot be safely removed by equipotential bonding, as will be illustrated in the following subsection, which means that the cleaning procedure has to incorporate a throughput-limiting charge neutralization step, which requires five minutes in this example. Other production processes involving devices and semiconductor wafers, if subjected to equally stringent analysis of the electrostatic risks inherent in the process, may also be found to have a similar requirement for the safe removal of static charge by air ionization before further handling, rather than relying on equipotential bonding.

The conclusions drawn from this analysis are somewhat alarming, considering the trust that is placed in using equipotential bonding as a protective practice within the semiconductor industry:

? Grounding a charged object is unlikely to neutralize it unless it is homogeneous and conductive ? Grounding a charged object is likely to create an internal electric field between balanced opposite charges ? Grounding a field-sensitive electrically neutral object makes it more susceptible to field-induced damage

? Grounding reduces the effectiveness of air ionization, the only practical way of neutralizing an insulator Equipotential bonding definitely reduces conductive ESD during material handling, by ensuring that objects always carry balanced charge, but it is neither inherently safe nor protective to use it with any field-sensitive object. ESD suppression through equipotential bonding does not necessarily achieve complete device protection and it can have the opposite effect to the one intended, by enhancing any risk arising from field induction.

8 b) Air ionization

Air ionization is the most practical way of removing static charge from insulators in a semiconductor factory, but it has been explained why it is not a guaranteed way of neutralizing static charge if used in combination with an equipotential bonding scheme. Air ionization also has some potentially negative attributes. Year 2021 Most types of air ionizer used in semiconductor factories generate ions by applying a high voltage to a sharp electrode. This creates a high field strength at the tip of the electrode and this ionizes air molecules, which are subsequently repelled from the electrode by the electric field. It is evident from this description that many air ionizers generate intense electric fields in order to work. It is essential that the electric field generated by otherwise the object could be damaged by the very device that is installed to protect it. This potential damage scenario is regrettably not rare.

In the measurement shown in Fig **??**, the sensor device [5] was loaded into a piece of reticle handling equipment fitted with an air ionizer in the load port area to neutralize any charged incoming reticles. Unfortunately, this ionizer had been installed much too close to the reticle handling path and the pulsed field from the ionizer tips

could reach the reticle as it passed underneath. Every pulse of electric field from this ionizer recorded by the sensor reticle was capable of causing irreversible and cumulative damage to a production reticle.

Fig. **??**: Electric field recorded by a sensor reticle introduced to a piece of handling equipment fitted with an ionizer that is too close to the reticle handling path. As the reticle passes by the ionizer it experiences a rapidly oscillating field, each transient of which is capable of causing EFM degradation of the reticle [7], [14], [15], [21], [22], [23]} Furthermore, as is shown by the offset in the reading after the reticle had passed beneath the ionizer, the ionizer had actually charged the surface of the reticle, leaving it susceptible to further damage as a consequence of subsequent handling with grounded robot arms. A similar observation was reported by Turley in an evaluation of the static control measures being used in a reticle manufacturing facility [13].

For correct operation it is essential that the ionizer is maintained to keep its output in a balanced condition, since contaminants in the cleanroom air can build up deposits on the ionizer tips that affect the ion production efficiency, leading to unbalanced ion emission. As mentioned by Turley [13], correct positioning of an ionizer is also essential to ensure that balanced ion streams can reach the target. If ionizer imbalance happens or an ionizer is badly positioned, it can add static charge to any object that passes nearby, which is demonstrated by the measurement shown in Fig 5. Subsequent handling of the reticle by a grounded robot arm, which is probably intended to safely remove any charge through static dissipative contact pads, results in rapid field reversals within the reticle. It can be seen that after each of the two handling steps the reticle has not been discharged.

The use of a grounded handling tool in this instance has created a significant risk of damage, by causing rapid transient field changes within the reticle. Every time the field conditions experienced by a reticle change, irreversible and cumulative damage can be caused, with transient field reversals of this kind being particularly hazardous [14], [15].

If the reticle cleaning station illustrated in While ionizers may indeed be the only practical way of dealing with static charge on insulators in a semiconductor manufacturing environment, they are certainly not fail-safe when being relied upon for the protection of field-sensitive items. When combined with an equipotential bonding scheme they can be rendered ineffective, and when used under conditions similar to those illustrated here they can be extremely hazardous.

9 c) Static dissipative and ”conductive” plastic boxes

industry the incorrect impression that the pods were working as intended and were adequately protecting their reticles, so they have subsequently been adopted the world over.

Reticle pods that were claimed to be electrostatically protective by providing a conductive path from the reticle to ground were developed by several makers wishing to capitalize on the standardization of reticle handling through the SEMI Standards, and pod designs based on this concept have become widely adopted. Fig **??** shows an extract from a reticle pod patent [17] that includes claims of the protective quality of the design, based on the belief that equipotential bonding safely removes static charge from charged objects such as reticles. The patent describes the prior art as requiring static dissipative contacts with the reticle to provide grounding through the pod door, but identifying that the static dissipative additives available at that time when added to the plastic of the box shell made the material cloudy, so the reticle could not be viewed. In this patent the grounding is provided via the support structure rather than through the pod shell, so the shell is made from transparent nondissipative (i.e. insulating) material to provide improved visibility of the reticle inside the pod.

Grounding a reticle in this way increases the risk of electrostatic damage, and increases the severity of any damage that may be caused to a reticle carried inside such a pod [7], [11], [12]. Making the pod shell from field-transmitting material and grounding the reticle is a significant technical error, which is also made in another reticle box patent that claims to be protective [18], so this is not an isolated case of the misunderstanding.

Cheng et al [19] describe a modified reticle pod with embedded and/or externally applied metallic panels that are intended to shield the reticle from electric field, such as that arising from static charge generated on the pod handle by manual handling. However, these ”shields”, and the metal plates added to the top of single reticle pods for automated handling in reticle stockers, actually increase the field-induced reticle damage problem as shown by the computer simulation of It was mentioned in section II that static dissipative boxes (also known as pods or FOUPS) have been found to be less protective than they were originally believed to be. Very soon after static dissipative single reticle pods were developed, testing showed that they are incapable of effectively shielding reticles from externally generated electric fields [16]. Because it had already been shown through experimentation at International Sematech that reticles can be damaged by field induction, this revelation should have resulted in the adoption of alternative reticle handling solutions that offered reticles adequate protection from electric field. However, the reduction in reticle ESD damage rates after the introduction of these new static dissipative reticle pods (alongside the complementary electrostatic countermeasures as already described in IIIa) gave the semiconductor Fig. **??**: An example of a reticle pod patent that claims to be electrostatically protective but which will actually have the opposite effect to that claimed. Grounding of a reticle in this way will increase its susceptibility to field-induced damage and cannot remove static charge from the reticle in the way claimed in the patent (refer to **??**ig 1). Fig. **??**: Computer simulation of a reticle pod with a grounded static dissipative door and reticle supports, that has a metal panel inserted between the handle and the top casing of the pod in an attempt to shield the reticle from static charge generated on the handle, as described in [19]. The metal

panel increases the electric field strength experienced by the reticle by perturbing the electric field, which is the opposite effect to that intended.

Metallic shielding in the form of a Faraday cage needs to be continuous and to completely enclose the protected item, as is well known from studies of EMI prevention. Modifications of reticle pods in the way illustrated in Fig **??** were carried out in an attempt to simultaneously overcome the ESD damage problem caused by reticle pod charging while avoiding the cost of replacing existing reticle pod inventories with much more expensive static dissipative alternatives. Such "inhouse" modifications and pod redesigns were ineffective for the reason illustrated in Fig 7 **??** Consequently, in the belief that the claims of reticle protection made by their manufacturers (as described in the cited patents) are true, most single reticle pod users have adopted static dissipative pods and boxes, which production. All these attempts to provide electrostatic protection fail because of fundamental errors in the understanding of the risk.

The significance of making such errors in reticle pod design becomes apparent when one considers the extent of tribocharging of a reticle pod during normal handling and use. It was believed on the basis of the wipe-tests carried out to simulate the tribo-charging of a pod during manual handling that static dissipative materials do not tribocharge, hence their use for the construction of reticle pods should eliminate the pod charging problem and the ESD damage that it causes.

However, it has been shown that this is a misconception, as static dissipative plastics actually do tribo-charge quite efficiently. Year 2021 have now become a de facto standard in semiconductor If one uses a field sensor with sufficient sensitivity and temporal response, one finds that static dissipative pods generate and transmit to the interior a great number of intense electric field transients, even when they are being carefully handled in staticcontrolled semiconductor production environments. An example of this is shown in Fig 8. Transients and high frequency fields are potentially highly damaging to reticles, as is explained in [15]. Static dissipative materials generate transient electric field pulses through normal handling, as demonstrated by the recording in Fig 8 **??** They also convert constant external electric fields into internal field transients, doubling the damage risk; and they act as high-pass filters, selectively allowing rapidly changing external electric fields to penetrate -which means that they are definitely not ideal materials to use for the construction of reticle pods and boxes.

Being aware that reticle electrostatic damage was still happening inside static dissipative reticle pods, despite the adoption of all the recommended protective measures, Helmholz and Lering [12] conducted experiments to measure how much the protection provided by a reticle pod could be improved by increasing the conductivity of the plastic, from static dissipative to "conductive". By this time the desire to have a transparent case for the reticle so that it could be visually identified, as mentioned in the reticle pod patent [17], had been replaced by the urgent need to eliminate costly reticle electrostatic damage.

Helmholz and Lering showed that as the conductivity of the plastic pod shell was increased, the tested a pod constructed from the most conductive plastic material available (carbon nanotube loaded PEEK) a test reticle stressed inside it by exposure to an externally generated electric field suffered ESD damage.

Pernicious electrostatic damage mechanisms other than ESD take place at an electrostatic stress level orders of magnitude weaker than that which causes ESD in a reticle [20], [21], [22], [23], but their study did not evaluate the ability of the pods to suppress these. If a "conductive" plastic reticle pod was found to be incapable of preventing ESD damage to a reticle stored inside it, it certainly would not be capable of protecting a reticle against these other damage mechanisms.

Helmholz and Lering also confirmed that the damage sustained by the reticles in their test pods was increased by grounding them, as is confirmed by the results from their paper which are reproduced in Fig 9 **??** lobal Journal of Researches in Engineering ( ) Volume Xx XI Is sue III Version I J Year 2021 field-shielding effect was improved. But when they Fig. **??**: Reticle pod test results reproduced from [12] showing that the test reticles suffered ESD damage inside conductive plastic reticle pods when stressed by an externally generated electric field, and that the damage was made much worse by the reticle being grounded inside the pod.

An important observation relating to the results presented by Helmholz and Lering is that even though their field measuring apparatus was some of the most sensitive and temporally responsive equipment available (a picocoulomb meter connected to a fast storage oscilloscope) it did not detect the rapid field transients that the "conductive" plastic pods allowed to penetrate, and which had caused the ESD damage in their test reticles. The sensor reticle [5] used to present the field measurements previously shown also cannot accurately measure field transients with shorter duration than ~50ms, owing to the integrating electronics that the device uses.

Since a reticle can respond to (and potentially be damaged by) field changes up to GHz frequencies and beyond, such electronic sensors cannot detect all electrostatic threats that can cause damage in a reticle.

10 IV. Implications for the Electrostatic Security of Devices

The previous sections have dealt almost exclusively with the electrostatic risk to reticles, because they are the most extensively studied subjects in investigations of field induction effects in semiconductor manufacturing and they have been the primary focus of this author's work. Through the reticle studies it has been found that there are inherent weaknesses in the methods being adopted to mitigate electrostatic risk, with some ESD prevention practices creating or exacerbating other electrostatic risks that can cause damage to very sensitive items.

Technical errors have also been made in developing material handling "best practice" which, while intended to be protective, instead results in fieldsensitive items such as reticles being put at an elevated risk of damage

through field induction. It follows that if this undesirable situation is true for reticles, which has now been proven beyond any doubt, then it must also be true when handling other field-sensitive items in the same way. This would be especially true considering the errors that have been made in the interpretation of the risks, and the procedures that have been adopted to address them, as described earlier.

It is known that semiconductor devices are generally not as sensitive to external electric field as reticles, although some devices do exhibit sensitivity to example, Wallash et al [24] report that GMR recording heads exhibit sensitivity to transient fields if one terminal of the device is connected to a short conductor that functions as an antenna. This means that components that may not be field sensitive when they are being manufactured may develop field sensitivity when they are being installed into electronic assemblies. They observe:

"the susceptibility of Class 0 devices to current transients caused by transient, high frequency fields has not been well studied. It is concluded that it is important to measure the field sensitivity of assemblies with Class 0 devices" Not detecting an electrostatic threat -and even the total absence of ESD damage -does not mean that electrostatic risk is being adequately controlled, and patented "protective" solutions don't necessarily do what is claimed of them. field-induced damage under certain circumstances. For Sonnenfeld et al [25] in their review of failure modes in semiconductor devices also comment:

11 "?it is not widely known how degradation mechanisms propagate as a function of environmental conditions and various stressors. The attainment of such knowledge is critical for advancements in the field of power electronics health management and prognostics. The ability to perform large scale experiments and characterize the degradation signatures of such semiconductor devices under various scenarios is of great interest?

The assumption of new functionality will also increase the number of electronics faults with perhaps unanticipated fault modes. In addition, the move toward lead-free electronics and microelectromechanical devices (MEMS) will further result in unknown behaviors."

Both of these articles highlight the lack of knowledge about damage mechanisms and the susceptibility of advanced devices to them. They also express the view that further research into semiconductor and hybrid device damage mechanisms should be carried out. In consideration of the identified errors and misunderstandings that have been made during the development of supposedly protective handling methods used throughout the semiconductor industry, it seems prudent that field sensitivity -and the effect of exposure to electric fields during the manufacture of electrostatic-sensitive devices -should be a prominent part of such research.

It would not be wise to assume that current handling methods are safe, given the errors in them that have been identified, and especially if no research has been conducted to find out whether hitherto-undetected field-induced damage might be happening in electrostatic-sensitive electronic devices.

A flat panel display is an example of a recentlydeveloped electronic device that exhibits extreme electrostatic sensitivity during its manufacture. The initial approach taken to try and avoid electrostatic damage was to implement the standard principles described in This did not prevent damage, which was happening as a consequence of the unavoidable charging of the panel by the manufacturing processes. It was therefore considered necessary to adopt an alternative approach, so the principles of field management rather than control of electrical potential -as described in SEMI Standard E163 -were applied.

Special coatings were developed and applied to surfaces that contact the panels so that tribocharging would be reduced; ionizers were installed to neutralize charge generated on the panels when rolling conveyors were being used; and insulating support pins rather than grounded conductive ones were employed at processing stations to prevent the concentration of any remaining electric field at the points of contact with the substrates as they were being lifted [26]. It was found that significant improvements could be made by abandoning long-established principles and taking this alternative approach to their electrostatic protection.

Re-evaluating a problem from a different perspective sometimes reveals that evidence has been misinterpreted in the past, as was found after retrospective analysis of data from the reticle damage studies that had been conducted at International Sematech [20]. This led to debate among some electrostatics practitioners about the presumed protective quality of equipotential bonding. During an online discussion initiated by this author about the possible negative consequences for device safety as a result of using equipotential bonding during handling, most contributing ESD practitioners in the discussion group stated that devices are not field-sensitive and believed that they could not be damaged in this way. Smallwood expressed doubt that concern about the use of equipotential bonding was justified, because the rationale for using it during manufacturing was sound and the results achieved by doing so were significant and positive.

However, M K Radhakrishnan, an IEEE EDS distinguished lecturer [27] commented:

11 ”?IT IS NOT WIDELY KNOWN HOW DEGRADATION MECHANISMS PROPAGATE AS A FUNCTION OF ENVIRONMENTAL CONDITIONS AND VARIOUS STRESSORS. THE ATTAINMENT OF SUCH KNOWLEDGE IS CRITICAL FOR ADVANCEMENTS IN THE FIELD OF POWER ELECTRONICS HEALTH MANAGEMENT AND PROGNOSTICS. THE ABILITY TO PERFORM LARGE SCALE EXPERIMENTS AND CHARACTERIZE THE DEGRADATION SIGNATURES OF SUCH SEMICONDUCTOR DEVICES UNDER VARIOUS SCENARIOS IS OF GREAT INTEREST?

”The assumption of internal damage in the semiconductor devices is correct. We have seen it in our experimental analysis studies of thin gate dielectric devices some time back. Also, we have observed that the internal electric field can cause damages not only to gate dielectric, but in many cases to other interfaces and junctions as well.”

Examples of the kinds of damage that can be caused in and around electrically-overstressed device junctions can be found in Radhakrishnan’s published papers, for example [28]. In this paper the authors present failure analysis results from a variety of semiconductor devices that have been damaged by ESD or by EOS, identifying through high resolution microscopy some distinguishing characteristics of the two different damage mechanisms. The paper includes TEM images of suspected ESD-induced damage to tungsten via plugs, as reproduced in Fig 10, showing progressive damage that ultimately results either in the via contact being broken (their fig. **??**b) or penetrating into the silicon substrate (their figs. **??**a and 9d). These images are particularly interesting because they indicate a directional quality of the damage mechanism that is similar to that seen in field-induced damage in reticles.

When chrome migration was first observed in reticles it was initially attributed to melting and reflow of the metal by the discharge current from low power ESD events [29]. This was subsequently shown to be a diagnostic error, however, after the movement of the metal was identified as field-induced migration [20], [21], [22], [23]. The directional quality of the damage mechanism in reticles and measurements of the current flowing during the damage process unambiguously Electric field is known to enhance atomic mobility, being applied during epitaxial deposition processes to enhance the growth of crystal films [30], [31]. Sengupta and Pavlidis [30] further explain how bonding in a material can be altered by the application of an electric field.

The images reproduced in Fig 10 show a directional damage characteristic, and the region around the damage sites does not appear to have been stressed by localized heating -certainly not to a temperature sufficient to melt tungsten (>3400°C). Their images 4a and 9d show movement of the tungsten plug material into the silicon substrate, whereas their figs 4b and 9c show separation at the contact junction and no movement of the tungsten into the substrate. In their images 4a and 4b there are also discernable changes at the top of the tungsten via plugs; when the tungsten has moved towards the substrate there is a small depression visible at the top via contact, but where the tungsten has broken contact with and moved away from the substrate, there is no depression seen at the top. The contact zone within the substrate itself is also sharply defined and appears undamaged when the tungsten has moved away from the substrate (their fig **??**b).

If these examples of damage had all been due to thermal overload at the interface, leading to melting of the tungsten, it is unlikely that this directional behavior would be observed, that areas in close proximity would be undamaged and that the junction would have survived to be studied by TEM. This suggests that the material movement observed in these damaged structures is possibly due to a high local electric field. Although it was observed after ESD stress testing, such damage would not necessarily be dependent on an ESD event injecting a surge of current to cause it.

Further evidence of the damaging effect of electric field within a semiconductor device is shown in Fig **??**1, which is reproduced from another of Radhakrishnan’s papers [32]. The authors had identified that breakdown of gate oxides in FETs was often accompanied by the epitaxial growth of silicon protrusions at the site of the breakdown, a newlyidentified phenomenon that they called dielectric breakdown induced epitaxy (DBIE). They attributed this epitaxial growth to the effect of a strong ”electron wind” at the site of the dielectric breakdown, pushing silicon atoms either from the silicon substrate or the polysilicon gate electrode into an epitaxial hillock at the breakdown site.

Fig. **??**1: TEM image of an FET that had suffered DBIE but was still working, reproduced from [32] However, in Fig 11 the gate oxide had not yet been ruptured by the applied stress and the transistor was still working, but DBIE was present beneath the gate oxide layer, which had bowed upwards. There is no evidence of localized breakdown of the dielectric and the DBIE is evenly distributed across the gate. On close inspection it is also possible to see faint lines beneath the distorted dielectric layer, suggesting the progressive movement of the interface through a number of discrete steps.

Rather than the epitaxial growth of the hillock being due to dielectric breakdown, a more plausible explanation for it is the field-enhanced diffusion of the oxygen atoms, followed by the re-incorporation of the silicon atoms that were left behind into a continuation of the substrate’s crystal structure. It is evident from this that field-enhanced diffusion is a probable precursor to dielectric breakdown, an explanation that would be consistent with the established ”percolation” models of dielectric breakdown. If this interpretation of the evidence is correct, this example indicates that the stoichiometric changes produced by electric fields within solid state devices can be somewhat more significant than previously thought -the macroscopic structure can actually move!

The online debate among ESD experts about the hypothetical enhancement of field-induced damage in semiconductor devices through the use of equipotential bonding resulted in no agreement being reached. It nevertheless generated some fresh curiosity, with Smallwood recently conducting a simple experiment to determine whether or not semiconductor devices can be damaged by field induction [33]. His experiment proved that under certain circumstances they can be damaged, without an ESD event taking place. Until this experiment was carried out to test the hypothesis, the prevailing view of ESD consultants working in the semiconductor industry has been that devices are not susceptible to field-induced damage and that grounding them is therefore both safe and protective.

That view is now shown to be open to doubt, so further investigation of field induction effects in devices and of any potential negative consequences arising from the use of equipotential bonding during their manufacture and handling would therefore be prudent.

V.

12 Discussion

The Industry Council on ESD Target Levels white paper 2 [7] fully describes the subject and recommends a reduction in the specification for device protection. This is not, however, an indication that devices are becoming less sensitive to electrostatic damage over time, which is a conclusion that could be drawn from this recommendation. It is a response to the changing nature of CDM discharges as devices become larger and pin counts increase into the thousands. The simulated discharge current increases with package size and the smaller contacts needed to make so many connections to the device are unable to withstand the current generated by the CDM testers at the specification of 500V. It is not that the risk itself has reduced, it is that the established way of determining the susceptibility to the risk has become unsuitable. The nature of reticle electrostatic damage has also changed with shrinking feature dimensions and spacing. Retrospective interpretation of previously published data on device damage has now indicated that some of the available evidence may have been misinterpreted in the past.

Clearly, the assessment of electrostatic damage risk is something that demands constant review and revision.

Many papers have been published that have reported on the durability and performance of the various dielectrics being used for gate insulation. This is not only of interest with regard to the potential for gate oxide damage as a result of an ESD strike, but also because time dependent dielectric breakdown (TDDB) is a major cause of devices failing during use. The ability of dielectrics to work efficiently and remain durable when only nanometers thick is crucial for device scaling, which is why better performing materials are always being sought.

These studies have consistently reported that one of the main causes of dielectric failure regardless of the specific chemical composition of the dielectric is stress from an excessive electric field, which causes cumulative stoichiometric damage to the material, ultimately leading to breakdown. The evidence from TEM analysis of highly stressed FET gates indicates that field-induced structural damage may precede dielectric breakdown and device failure.

It follows from this review that there is a potential risk to all advanced devices arising from uncontrolled exposure to electric field, and even from the stresses created during normal device operation, yet this aspect of risk has not been extensively investigated, perhaps because the prevailing view among those advising the industry on electrostatic protection is that devices are not sensitive to damage by electric field.

”there is increasing anecdotal evidence that the presence of static charge on wafer surfaces is becoming an ESD hazard as gate oxide thicknesses become thinner. In the future, there may need to be further limits on allowable static charge on wafer surfaces to prevent ESD-related gate oxide damage during front-end semiconductor manufacturing. Further research is needed in this area.”

Despite this anecdotal evidence being known about and advice for further research to be carried out being included in the SEMI Standard for two decades, little fundamental research appears to have been done in this regard, as no publications on the study of fieldinduced defects in devices have been identified through an online literature search. This may be due to the focus in the SEMI Standards and other static-related advisory documents being almost exclusively on ESD prevention, as the text above demonstrates by using the term ”ESDrelated gate oxide damage”. The prevailing belief is that ESD control is already well understood and is being efficiently implemented. So unfortunately, any concern that might have arisen about this ”anecdotal” dielectric damage problem would, in all probability, have resulted in ESD consultants being more stringent in the application of the standard ESD countermeasures, including the use of equipotential bonding, which probably would not have improved understanding of the situation. Dielectrics can be damaged by electric field without any ESD taking place.

As with the new reticle damage mechanisms first identified in 2003, which had incorrectly been thought to be a form of ESD damage since the cause of them is the same (exposure to electric field) [11], [29], hybrid devices would be a cumulative process, giving no immediate indication that anything untoward had happened. Any dielectrics affected during manufacture would be unlikely to fail catastrophically when a device was tested but they could cause parametric variations in performance, and any such dielectric degradation would almost certainly contribute to early device failures through TDDB. The gate distortion seen in Unfortunately, if a damaged dielectric breaks down when a device is powered it is likely to result in thermal runaway that will destroy the defect site and make diagnosis of the root cause of the failure impossible. Thus, it is conceivable that a number of device failures in the field that are currently being classified as due to electrical overstress (EOS) may be caused by latent defects in the devices, resulting from dielectric damage that occurred during manufacture. It will be impossible to know whether or not this is happening without conducting more fundamental research of the kind carried out by Radhakrishnan et al to identify the precursor states and the factors causing them that eventually result in

industry can have some negative consequences for the protection of electrostatic sensitive items. Focusing on ESD prevention alone does not guarantee adequate protection of electrostatic sensitive objects. Remaining risks have been identified that are the result of incomplete and sometimes incorrect understanding of the problems by those who have defined the "solutions". The extent of this incorrect understanding is demonstrated by semiconductor industry patents which, being based on a physical principle that has been experimentally proven to be incorrect, will actually have the opposite effect to the protective one that the designers intended. Being a prominent supplier to the industry and even being awarded a patent for an invention clearly do not guarantee that the design will actually be protective in the way the maker claims.

Reticles are extremely field-sensitive and have served as an excellent test subject with which to study electrostatic effects and field-induced damage phenomena in general. The relative simplicity of the structure of a reticle which can be easily used to perform computer simulations of field distribution and strength, the visibility of the parts that can sustain damage, the ability to perform atomic force microscopy to study the damage mechanisms in detail and then correlate their distribution with the field simulations, all without having to deconstruct the test piece, has led to new awareness about the changing nature of the electrostatic damage problem.

The characteristics of electric field behavior that have been identified through the reticle damage studies have led to the realization, as has been proven with reticles, that some handling methods being used to combat ESD in the semiconductor industry put all New generations of device are typically more susceptible to electrostatic damage effects than previous generations because device features and critical dimensions are becoming smaller over time. This characteristic is further accentuated by the changing nature of field induction with decreasing feature separation, as illustrated by the computer simulation results shown in **??**ig 12, which were produced to help explain the changing characteristics of field-induced damage in reticles over time. Field induction is seen to be highly non-linear and to change radically in nature as the separation of conductive features is reduced, on a dimensional scale relevant to semiconductor devices and the reticles that are used to print them.

ESD prevention methodology involves reducing the potential difference between adjacent conductive objects below the threshold for breakdown, and ESD is dependent on both voltage and separation. As the separation of conductive objects moves into the nanometer regime it becomes impossible to generate conditions that will cause ESD by field induction, because there is insufficient separation to build up a cascade of ionization (the initiation of a spark) and it is also impossible to generate a large enough potential difference. Yet, while field-induced potential differences fall rapidly with decreasing separation, the field strength produced between adjacent conductors by field induction increases exponentially.

lobal Journal of Researches in Engineering ( ) Volume Xx XI Is sue III Version I J Gl 33 Year 2021 real-life device failures from field returns will be unlikely electrostatic-sensitive devices at heightened risk of fieldinduced damage during their manufacture and subsequent handling.

On the dimensional scale of the features found in current production reticles, small fractions of a volt induced between adjacent conductive features can be accompanied by hazardous levels of electric field, easily threshold for EFM [22]. The features within a semiconductor device are typically 4x smaller, owing to the demagnification factor used in lithography, so this dimension-dependent field enhancement effect is even more significant, and adding dielectrics between the conductors amplifies the field strength still further. Shu et al in their report on damage to the dielectrics used in spacecraft systems [33] quantify the harmful effect of electric field thus (their emphasis):

"One major parameter is the critical electric field for dielectric breakdown, E* = 10 6 to 10 8 V/m" Since the physical processes that ultimately lead to dielectric breakdown are cumulative and likely to start under less extreme field conditions and to begin propagating some time before the point of full dielectric breakdown is reached (as is suggested by the TEM image in **??**ig 11) the field strength of concern for device safety would appear to be comparable to that which causes EFM damage in reticles. On the scale of the structures found in modern production reticles such high levels of local electric field can be produced with induced potential differences of only a fraction of a volt. Evidently devices are now being designed to operate under conditions that this analysis would suggest are capable of creating field-induced damage, so TDDB is probably inevitable. Any uncontrolled exposure to electric field would certainly not enhance their durability. Therefore, concern about any exposure of devices and the dielectric interfaces they contain to uncontrolled electric field conditions would seem to be justified.

A focus on electric field management rather than ESD prevention is perhaps more appropriate today than it was when the principles described earlier were first defined for the industry.

The complexity of electrostatics management in semiconductor production has recently risen to new heights with the introduction of EUV lithography, which is conducted in a vacuum. This complexity is admirably illustrated in the paper by van de Kerkhof [35]. Considering the advanced treatment that the subject of electrostatic control has been given in this study of the latest generation of semiconductor production equipment, it seems anomalous that decades-old and somewhat flawed approaches to electrostatic protection are still being taken with the handling of the devices that these highly advanced machines are being used to produce. As the

Attention should be drawn to the fact that the damage described as "ESD damage" to embedded structures within a semiconductor device is not itself ESD, it is a consequence of a discharge having taken place outside the device. The mechanism of the internal damage will be different from the mechanism driving the external discharge, so controlling the conditions that result in an external discharge will not necessarily eliminate all the conditions within the device that could cause internal damage. As has been observed with reticles, the application of electrostatic stress always leads to a natural relaxation that can be achieved in various different ways. If the stress relaxation does not occur via a spark or by electronic conduction, it can happen by some other means that may not be intuitively obvious. The migration of the dielectric barrier and the formation of DBIE in the FET shown in The problem for the semiconductor industry is that it is extremely reluctant to change what is believed to be a working formula, even if problems are known about and potential improvements have been identified. If the present handling methods are deemed to be technically imperfect, but they seem to be good enough to make the devices in production today with satisfactory yield as they leave the factory, nobody seems inclined to change anything. Few managers with responsibility for assuring electrostatic compliance in a semiconductor factory would want to be the first to step out of line and adopt a different approach to that adopted by their peers, especially when so many certification schemes require the use of currentlyadvised practices.

Nevertheless, it cannot be a sound foundation for future device production to be using manufacturing practices that are known to be technically imperfect and to have the capability to damage sensitive devices. This is why the calls for more research to be carried out as cited and repeated here need to be heeded, so that empirical rather than anecdotal evidence as mentioned in SEMI Standard E129 can be collected, decisions about electrostatic control policies can be objectively reviewed, and if necessary they can be changed.

13 VI.

14 Conclusions

The semiconductor industry is generally reactive rather than proactive. An identified problem that isn't causing losses today will often be ignored until it becomes so serious that it cannot be dismissed any longer. Unfortunately, the cost of taking this "wait and see" approach can be orders of magnitude greater than the cost of taking timely preventive action. It has been shown here that concentrating on ESD control, rather than specifically the protection of the electrostaticsensitive devices being used and manufactured, has led to a number of technical errors and design weaknesses that ironically put those devices at elevated risk of fieldinduced damage.

While this situation may be survivable at present, the trend in semiconductor manufacturing as identified by industry roadmaps and Standards is inexorably towards greater susceptibility to electrostatic damage. It has been warned that unknown damage mechanisms may arise as new semiconductor device technologies and architectures are developed, and it has even been noted in SEMI Standards for decades that such damage mechanisms have been observed, but this has not yet been extensively investigated. The simple test recently conducted by Smallwood has shown that the confidence of the ESD community about devices not being susceptible to field-induced damage has been misplaced, and re-assessed evidence from past studies of semiconductor device damage have indicated that devices may not be as immune to fieldinduced damage as ESD experts advising the industry have hitherto believed.

It is therefore unwise for the industry to continue operating in a manner that has been identified as potentially hazardous, with technical errors embedded in operating procedures and being made in the assessment of risk, and using equipment that does not actually provide the protection that is claimed of it. A proactive approach needs to be taken to improve operating procedures, manufacturing equipment and even factory designs, and to improve the understanding of the subject by those assessing electrostatic risks and advising on best practice in semiconductor factories, so that future generations of semiconductor devices will be adequately protected against electrostatic damage. This process has already begun in flat panel display manufacturing.

A new focus on electric field management rather than ESD control is required, and research is urgently needed to quantify the susceptibility of electronic and microelectro mechanical devices to damage by exposure to electric field, both externally and internally. Until such fundamental research is done, the semiconductor industry will be in a state of "radical uncertainty" about the potential risk to devices from this cause. "Radical uncertainty" was explained as follows by Mervyn King, the former Governor of the Bank of England [36], when describing the management of economic risk. The final point he makes is perhaps the most important thing for the semiconductor industry to realize about risk assessment when knowledge is limited.

"The best example, I think is what we're going through now, COVID-19, in which we knew, well before it happened, that there could be things called pandemics. And, indeed? it was likely that we should expect to be hit by an epidemic of an infectious disease resulting from a virus that doesn't yet exist. But, the whole point of that was not to pretend that we, in any sense, could predict when it would happen, but the opposite. To say that: the fact that you knew that pandemics could occur did not mean that you could say there was a probability of 20% or 50% or any other number that there would be a virus coming out of Wuhan in China in December 2019". Year 2021 "Most uncertainty is of that kind. It's where you know something, but not enough, and certainly not

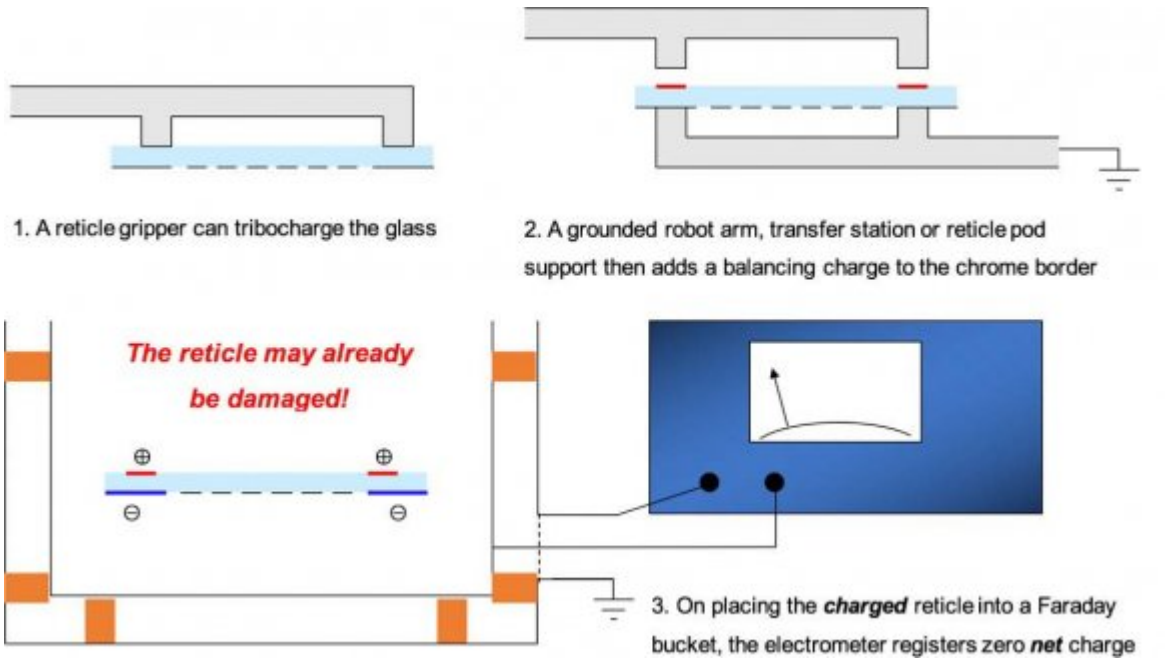


Figure 1: lobal

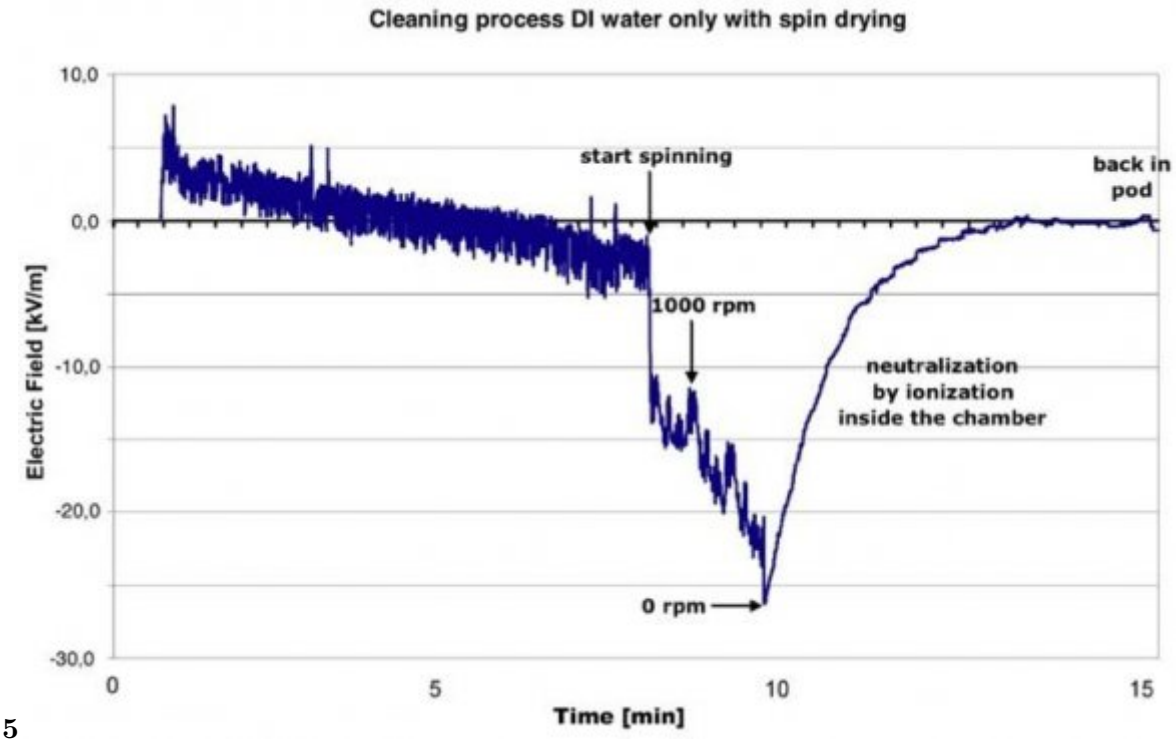


Figure 2: Fig. 5

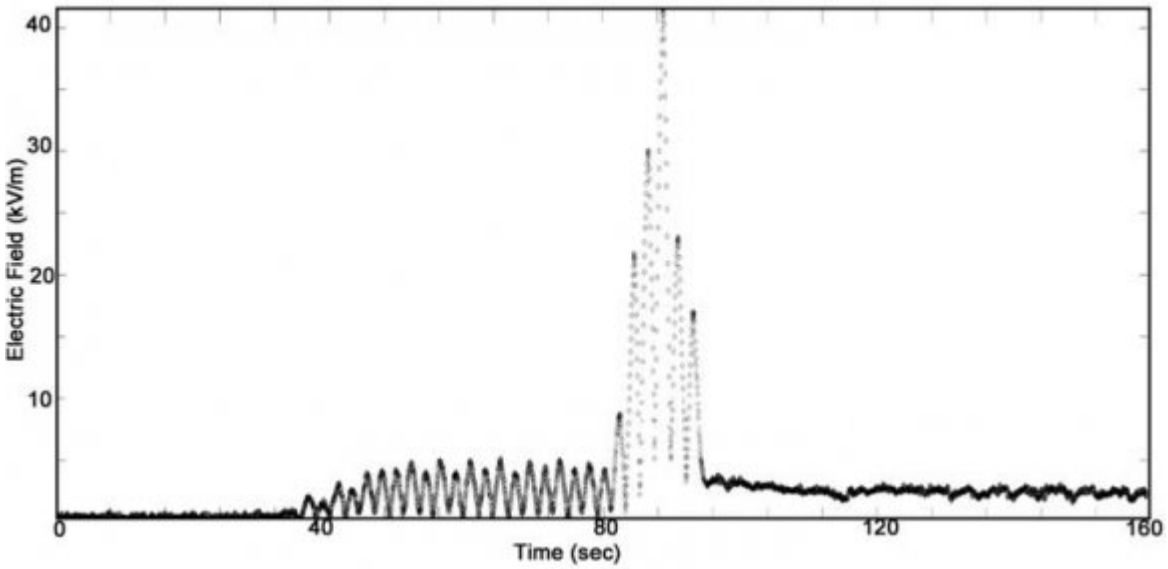
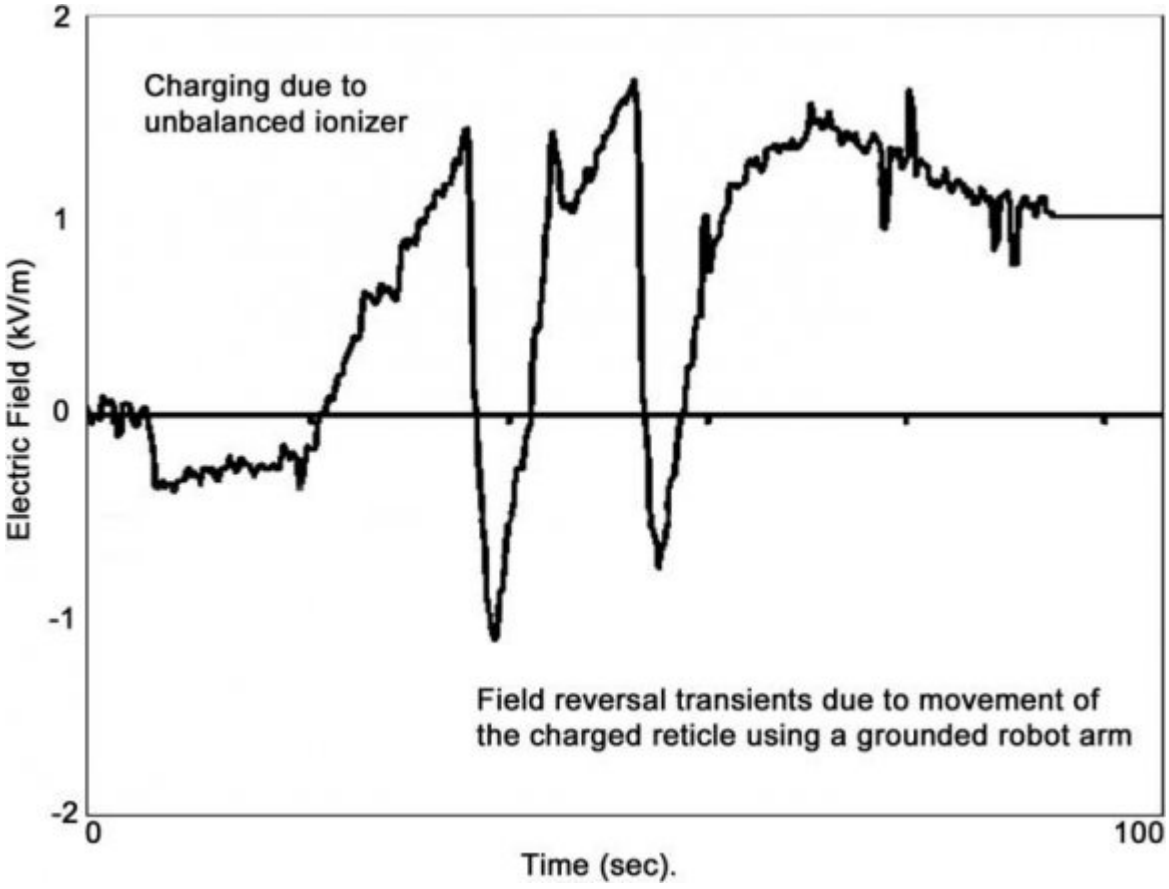
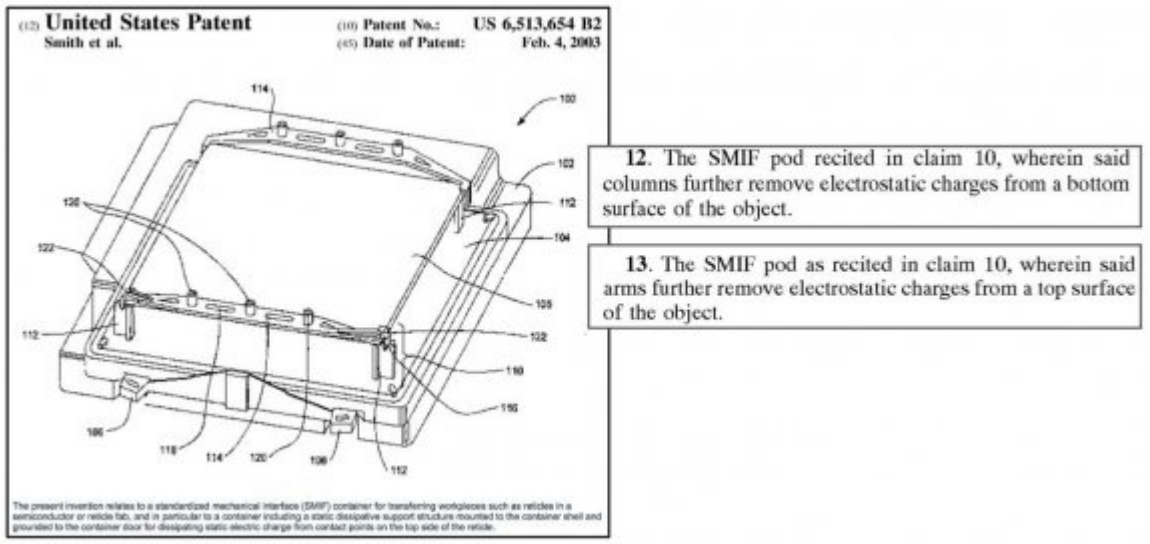

40
30
20
10
Electric Field (kV/m)
0
40
80
120
160
Time (sec)

Figure 3:


2
1
0
-1
-2
Electric Field (kV/m)
Charging due to
unbalanced ionizer
Field reversal transients due to movement of
the charged reticle using a grounded robot arm
0
100
Time (sec).



(12) **United States Patent**
Smith et al.

(10) Patent No.: US 6,513,654 B2
(45) Date of Patent: Feb. 4, 2003

The present invention relates to a standardized mechanical interface (SMIF) container for transferring workpieces such as reticles in a semiconductor or reticle fab, and in particular to a container including a static dissipative support structure mounted to the container shell and grounded to the container door for dissipating static electric charge from contact points on the top side of the reticle.

12. The SMIF pod recited in claim 10, wherein said columns further remove electrostatic charges from a bottom surface of the object.

13. The SMIF pod as recited in claim 10, wherein said arms further remove electrostatic charges from a top surface of the object.

Figure 5: lobal

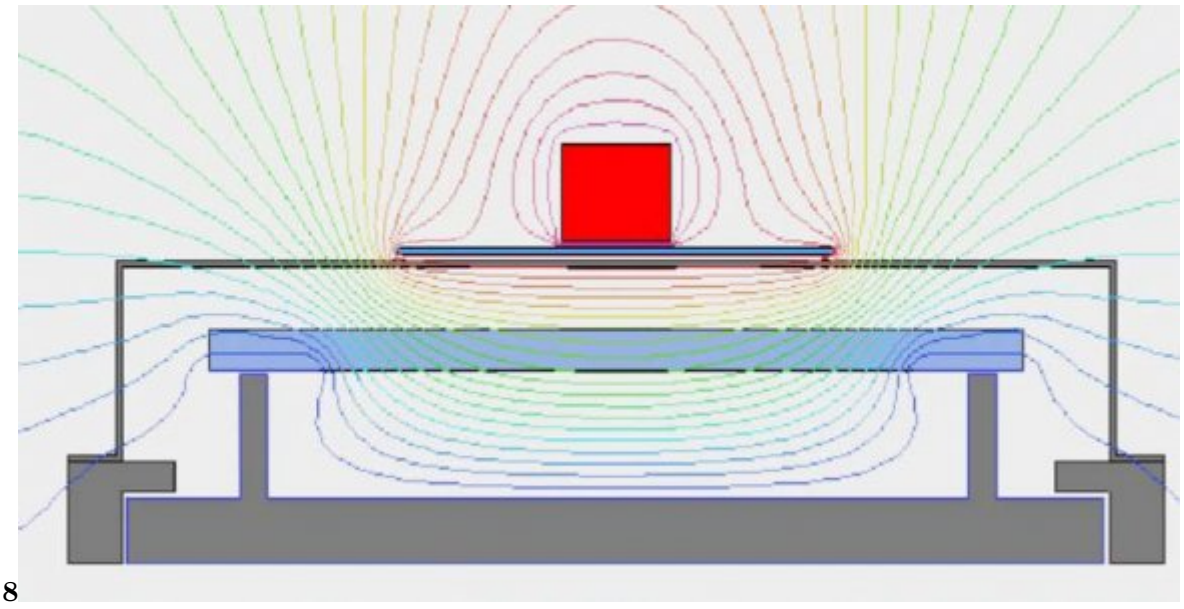


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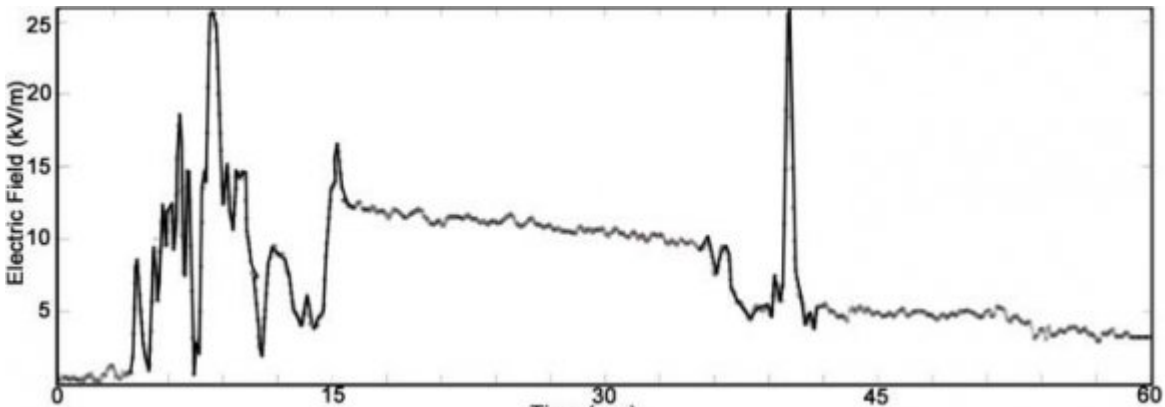
Figure 6: Fig. 8 :



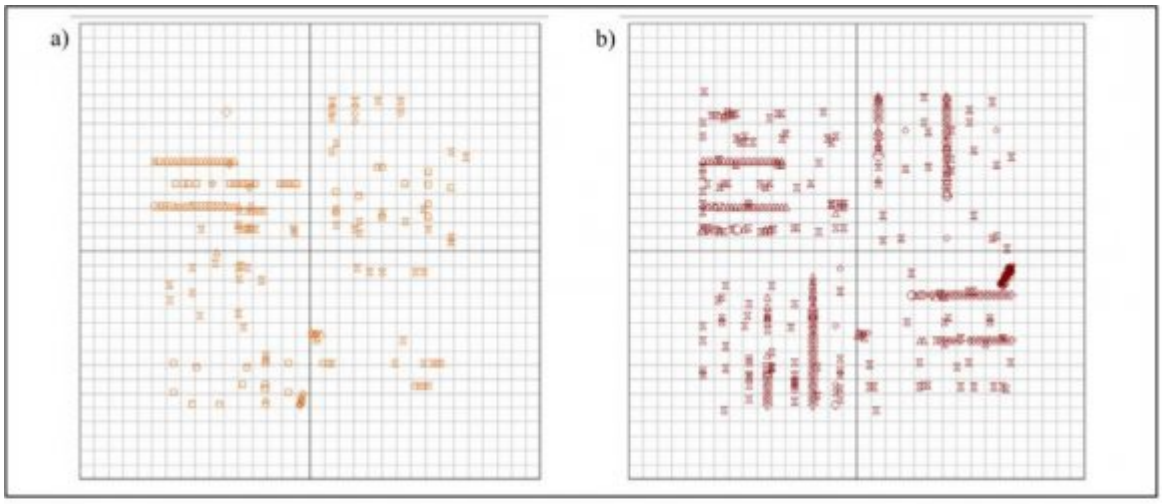


Fig 4 STARlight™ defect maps of ESD damages on a reticle held on a)insulation and b) conductive supports.

Both reticles were inspected on the STARlight™ mode on a KLA-Tencor mask inspection system after the tests, the results a displayed in Fig 4. Even though the reticle used in the experimental setup for isolating reticle contact points has been exposed to a much higher ESD challenge (20,000V highest voltage and 25 cycles of tests) the reticle shows much less ESD damages than the reticle used in the setup for conductive reticle contact points. A quantitative comparison cannot be made since the experimental setups were no the same, but qualitatively there is a clear picture: isolating reticle contact points greatly reduce the risk of ESD damages.

Figure 8: lobal

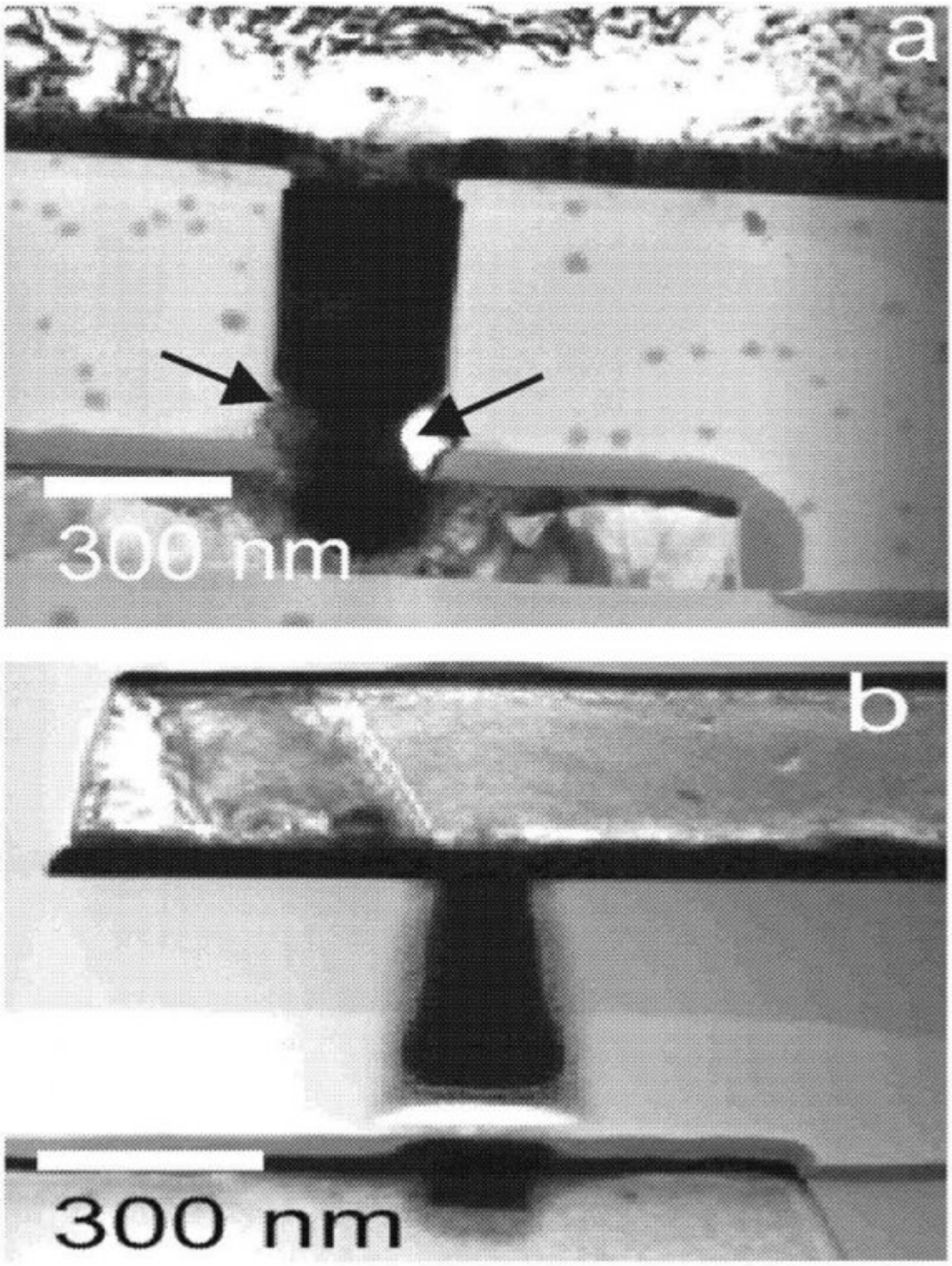


Fig. 4 TEM cross section on burnt out via and contact. (a) the via is still functioning but the necking has started, as indicated, (b) the contact is open.

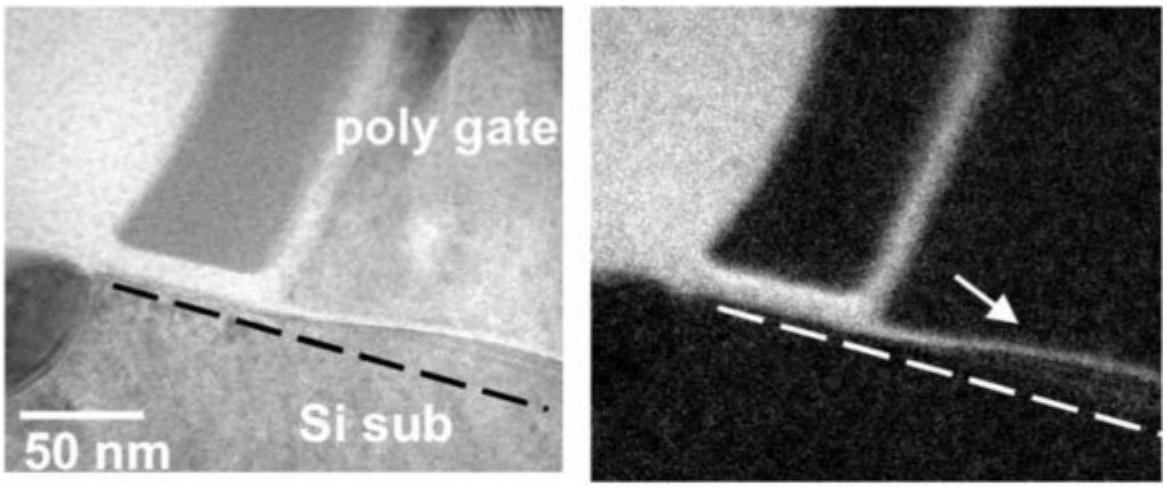
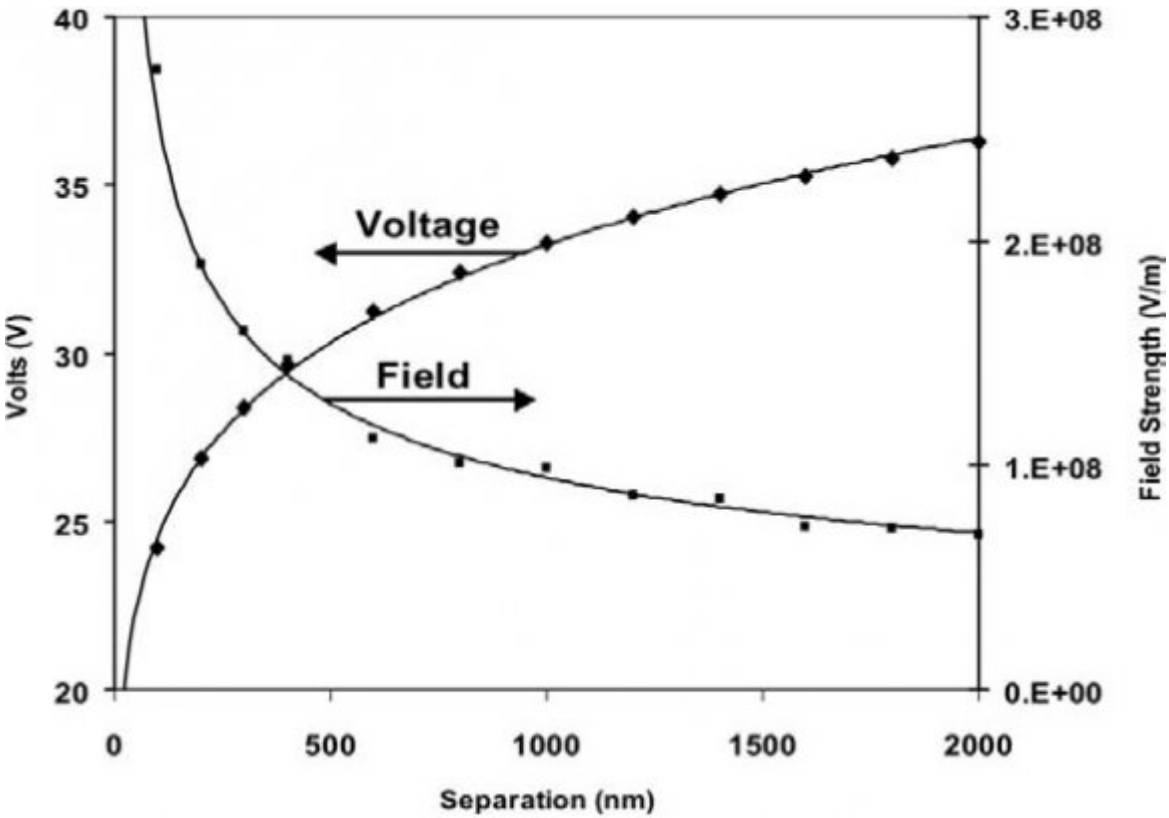


FIG. 4: TEM micrograph of a 0.18 µm nMOSFET with 33 Å Gox after a SBD for a current compliance set at 100 nA. (a) Gox was pushed up by the DBIE above the original Si substrate, as indicated by the dashed line. (b) EELS oxygen mapping showing that the gate oxide, as indicated by the arrow, was pushed-up along with the epitaxy islands.

Figure 10: lobal



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