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A First Principle's Approach to Study of the Silicon Drift Detector with Embedded JFET: Noise Analysis, Simulations & Analytical Modeling

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Abstract

Proto-type commercial grade Silicon Drift Detectors (SDDs) with on-chip low noise JFETs have been realized using silicon bipolar technology at Bharat Electronics Ltd (BEL), Bangalore. Noise analysis articulating the relationships of various noise sources on the electrical parameters of the fabricated SDD and JFET have been discussed. TCAD device simulations have been performed for the SDD and on-chip JFET for static (dc) and dynamic cases. The static case simulations revealed values of critical dc performance parameters like leakage current, anode capacitance etc. Dynamic simulations meant to study the effect of radiation, revealed the relationship between drift time drift distance within the detector. Analytical modeling of the I-V characteristics of the SDD has also been performed to predict the leakage current behavior for various other designs fabricated at BEL.

Index terms— Silicon Drift Detectors, Junction Field Effect Transistors,

1 Introduction

ilicon drift detector (SDD) is a detector based on the principle of lateral charge transport within the bulk of a fully depleted detector, as proposed by Gatti and Rehak (Reference-1). SDDs are fabricated over high resistivity n-type substrate with p-n junctions on both top and bottom sides of the substrate. PN junctions on the top-side are segmented field shaping cathodes whereas the back-cathode is a uniform p-n junction. A reverse bias gradient is applied to the field shaping cathodes, which results in creation of a potential energy distribution in the shape of a "Potential Gutter" with its ultimate electron potential energy minimum at the anode. Electron-hole pairs are created by passage of ionizing radiation and get swept vertically across the parabolic potential along the depth and are focused at the local potential minima. They then get drifted along the lateral drift channel towards the anode. The noteworthy feature of the SDD is that its small output (anode) capacitance is independent of its large detector active area. SDDs are suitable for high Author : Bhabha Atomic Research Centre, Electronics Division, MOD Lab, Trombay, Mumbai 400085, India. resolution (127eV @ 5.9 keV for Mn-K? line; Ketek Vitus SDD) and high count rate (~1x10 6 cps) X-ray spectroscopy applications. These detectors have found wide application in high-energy physics for tracking applications. SDDs have been incorporated in the ALICE detector experiment along the Large Hadron Collider at CERN. SDD's high-resolution capability can be further augmented by integrating the input device of the preamplifier (JFET) within the detector so as to avoid stray capacitance and microphonism. The integration of JFET onto the detector also facilitates better matching II.

2 Detector Design

Fig. 1(b) shows the 2D cross-section of the SDD of circular geometry with a cathode pitch of 120 ?m {p+ cathode width (70?m) + Inter-strip gap (50?m)}. An n-type high resistivity (4 k?.cm) <111> orientation substrate of 300 ?m thickness is employed concentration in p+ cathode region is approximated to be 1x10 18 cm -3 with

a gaussian distribution profile. Similarly, the back junction is also having the same concentration and profile. This version of SDD had an on-chip poly-resistor network for biasing the intermediate p+ strips together with an on-chip JFET for first level amplification [Fig. **??**(a)]. This device had 20 p+ cathodes with two guard rings encircling its outer perimeter. The first, fifth, tenth, fifteenth, twentieth, and last p+ strips were individually biased whereas The anode being an annular ring (radius = 50 ?m) having area of 7.7 x 10 4 ?m 2 which fetched an analytical full depletion anode capacitance of 27 fF for 300 ?m thick fully depleted silicon wafer. The total detector active area of the detector was 2.31 x 10 7 ?m 2 . The embedded lownoise JFET (named as JFET-10) for this SDD design had the smallest channel length (15 ?m) possible with BEL process [Fig. 1(c)]. For a designed channel length of 15 ?m and the channel width of 172 ?m, the analytical Transconductance (g m) worked out to be 0.247 mS. the gate current should be as small as possible to reduce the ENC 1 component of noise.

3 Noise Analysis

detector leakage current should be minimum for reduction of ENC 2 component.

4 c) Equivalent Noise Charge for feedback circuit

The noise due to feedback circuit can be minimized by choosing a very high value of feedback and bias resistors so as to make the effective parallel combination R P large.

The Equivalent Noise Charge (ENC) has a strong dependence on the optimum shaping time (TM) (Equations 1-5) (Refer Spieler notes). It can be inferred from equations 1-5 that TM should be as small as possible to reduce the components of noise playing a critical role in the SDD & JFET system. It was found that for a particular value of Transconductance g m and detector leakage current I D , the optimum shaping time was least for a capacitance mismatch factor (h) of ~1.

This means that the detector capacitance and JFET gate capacitance should not only be small but also nearly equal to each other. To prove this argument, a numerical simulation has been performed using values obtained from simulation of the JFET & SDD together. The plot in figure **??** shows the graphical representation of the relationship between optimum shaping time and mismatch factor. Figure 3 shows the mathematical relationship of the ENC on mismatch factor for the SDD-JFET system.

—Eq. 5 e) Net effective Equivalent Noise Charge ——Eq. 6

5 Device Simulations

Three Dimensional device simulations have been carried out keeping a two fold approach in mind. Firstly, device simulations carried out for the static case (without application of any radiation) on the SDD-JFET composite device system. Secondly, to study the effect of application of incident radiation (X-ray photons; ? = 2 A o) on the performance curves of the SDD. ii. Junction field effect transistor (JFET)

The virtual SDD-JFET detection system was again ported to the device simulator and device characteristics of the JFET alone were studied. The JFET was biased in common source configuration with the source at 0V and drain voltage of 30.5V and gate voltage varied from 0V to -20V (Transfer characteristics illustrated in figure 7). Fig. 6 shows the I D -V DS (Drain) of the JFET having gate width of 172 µm. The gate pinchoff voltage is V GSOFF = -6 V with a saturation drain current of ~6 mA (Fig. 6). The extracted Transconductance at I D = 5 mA and V DS =30 V is g m = 1.7 mS. The slope of the I D -V DS curve in the saturation region corresponds to an output resistance of 18 k?. The extracted gate leakage current was 1 pA at operating conditions, which would be significantly small as compared to leakage current of the detector (4.5nA). This ensures that the shot noise contribution due to gate current is negligibly small as compared to the one associated with the detector leakage current. It was observed that the transistor does not breakdown even at V DS = 42 V. The gate capacitance is in such a range that output capacitance of the SDD can be matched to get optimal results. Fig. 4 shows the leakage current of the detector as a function of reverse bias applied to cathode C-20 whereas figure 5 gives the C-V characteristics of the simulated SDD structure respectively. As the reverse bias is increased, the depletion region extends as function of from both sides of the device. The capacitance decreases to significant low value during initial reverse bias of -5 V when the depletion region from first strip touches the n + anode. Further increase in reverse bias continues to deplete the bulk (and reduce the capacitance) till full depletion is reached at -30 V. Beyond this bias anode capacitance saturates to a low value corresponding to a parallel plate capacitor of area that of anode and spacing between the plates being the detector thickness. 0.4 ns. The beam intensity was fixed at 1 W/cm 2 as the incidence area of 10 x 10 ?m 2 . The resultant anode which gave a Gaussian current pulse (Equation-7) with the rise time depending the distance from the point of incidence on the detector. Simulations were performed for X-ray incidence distances of 500, 1000, 1500, 2000 and 2200 ?m from the anode, and the current pulses at the anode were extracted. It was found that the current at the anode was delayed and rise times increased with increase in the distance of the X-ray incidence point from the anode. Drift times varied proportionately with the drift distance thus maintaining drift time to drift distance linearity. Alternatively, it was Additionally, a simulation was also performed in which both the SDD and JFET were biased in such a way that the anode of the SDD was shorted to the gate of the JFET and the combined node was connected to a resistor of 100 k Ohm and the other end of the resistor was connected to ground potential. This ensured that the anode current would be dropped across the resistor and this voltage drop would be fed to the gate of the JFET,

which in turn would result in a dynamical change in the drain current (ref. Fig. **??**). This ensures that the small change in the anode current be amplified by the transistor to give a large change in the drain also found that the current pulse at the anode experienced significant broadening due to diffusion of the charge cloud. This effect is incremental with increase in drift distance from the anode. The net deposited charge (0.24 femto-Coulomb) always remains conserved in all cases. This dynamic simulation helped in accurate estimation of pulse timing and height characteristics. This helped in designing the latter end of the instrumentation chain like pre-Amplifier, shaper etc. V.

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Analytical Modeling Of SDD I-V Characteristics (Static Case)

I-V characteristics of the SDD have been analytically deduced to predict the leakage current behavior for various other designs fabricated at BEL. The values of the constituent parameters of equations 8 & 9 have been enlisted below in Table-1. The I-V curve resulting from the equations 8 & 9 has been illustrated in figure 11. As seen from the curve, the saturation behavior is similar to the one derived from simulation. The deviation of the saturation anode current derived from simulation from that achieved from I-V model is merely 4.8 %. This small value of deviation in saturation current shows that the model is fairly successful in predicting the behavior of the SDD's I-V characteristics.

—-Eq. 8 ? = Constant = 200 (depends on surface recombination velocity) ——Eq. 9 1 * 1 qV qV KT KT R s I J A e e ? ? ? ? ? ? ? ? ? ? ? = ? ? ? ? ? ? ? ? ? ? ? ? ? ——Amperes 2 2 p n s p D n A D ni D ni J q N N ? ? ? ? = + ? ? ? ? ? ? ; Js = 1.

7 Conclusions

Noise analysis revealed the optimum value of capacitance mismatch factor (h) between SDD and JFET capacitances to be ~1. The relationship of shaping time with mismatch factor was found to be parabolic with minima at the optimum mismatch value. The net ENC too was found to be minimum at the optimum mismatch value. The full depletion anode capacitance derived from simulation was 200 fF for a full depletion voltage of -30V. The saturation value of anode leakage current was 4.5 nA. The transconductance derived from I-V simulation of the embedded JFET was 1.7mS for a gate pinchoff voltage of -6V. Dynamic simulations revealed the near linear dependence of drift time on drift distance within the SDD. Analytical modeling of the SDD's I-V characteristics showed a deviation of 4.8% in saturation anode current values achieved from simulation and analysis. [1] [2] [3]

Figure 1: S

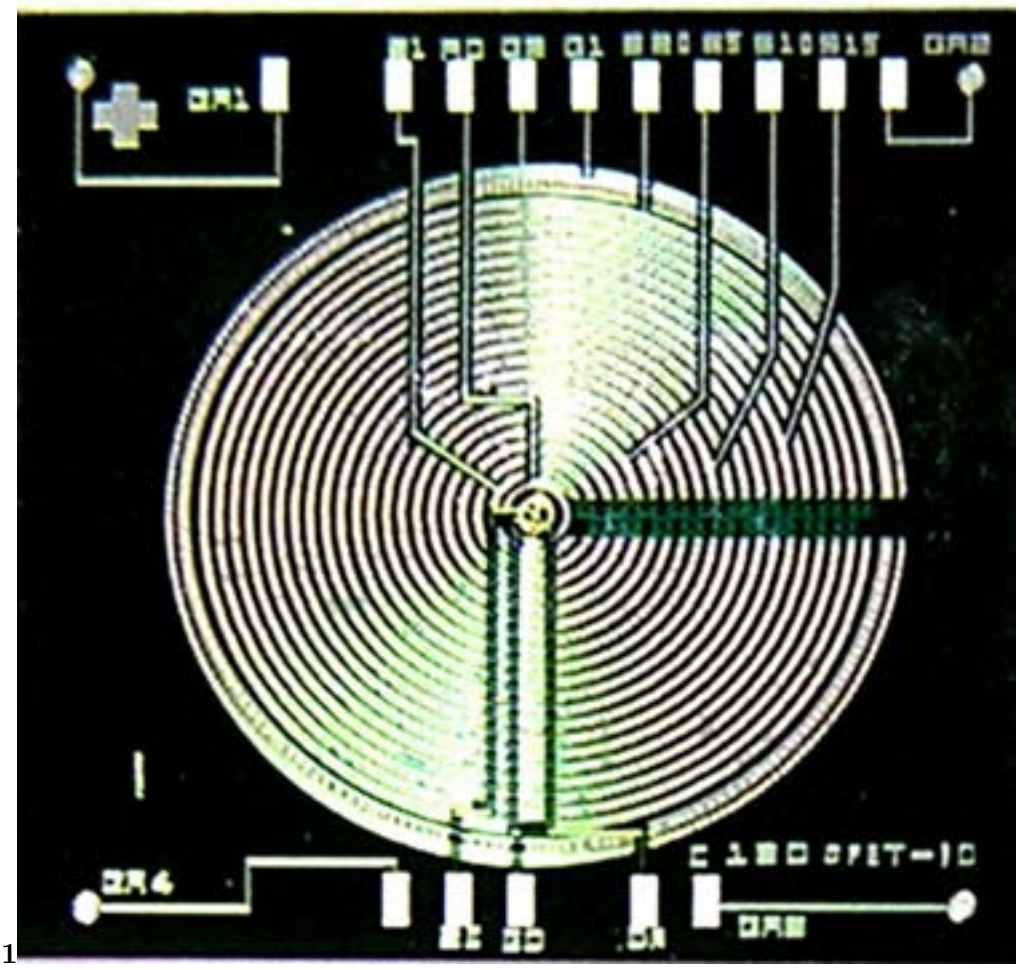

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Figure 2: Fig. 1 (

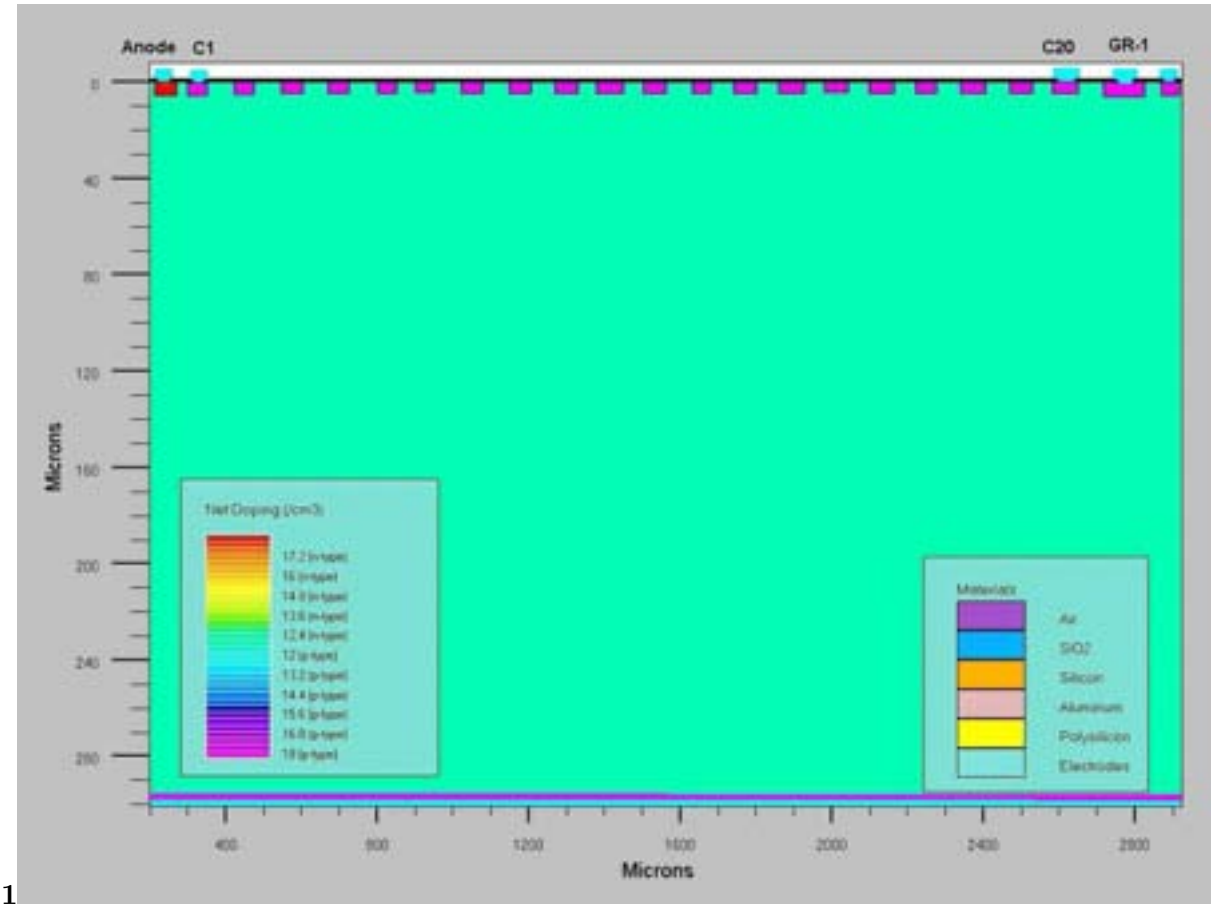

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Figure 3: Fig. 1 (

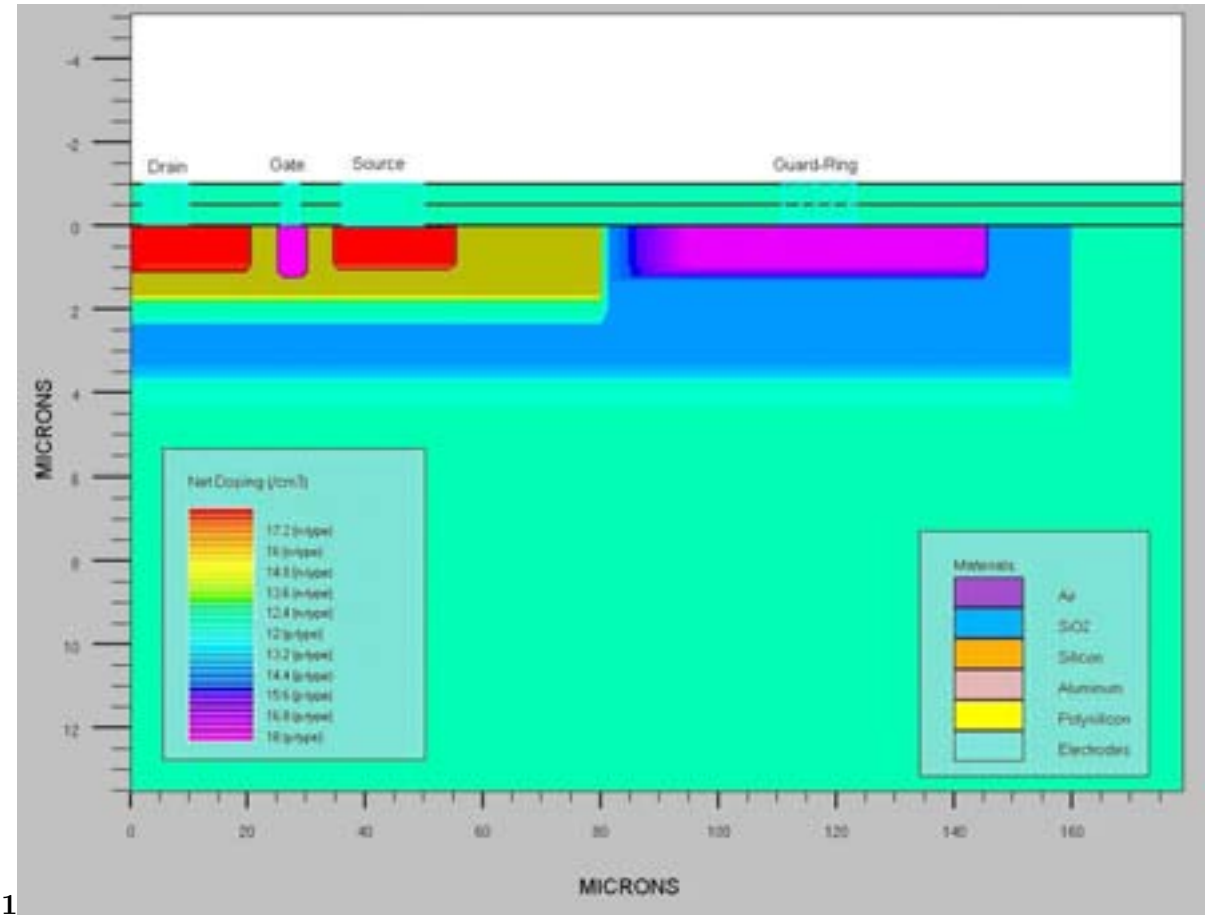

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Figure 4: Fig. 1 (

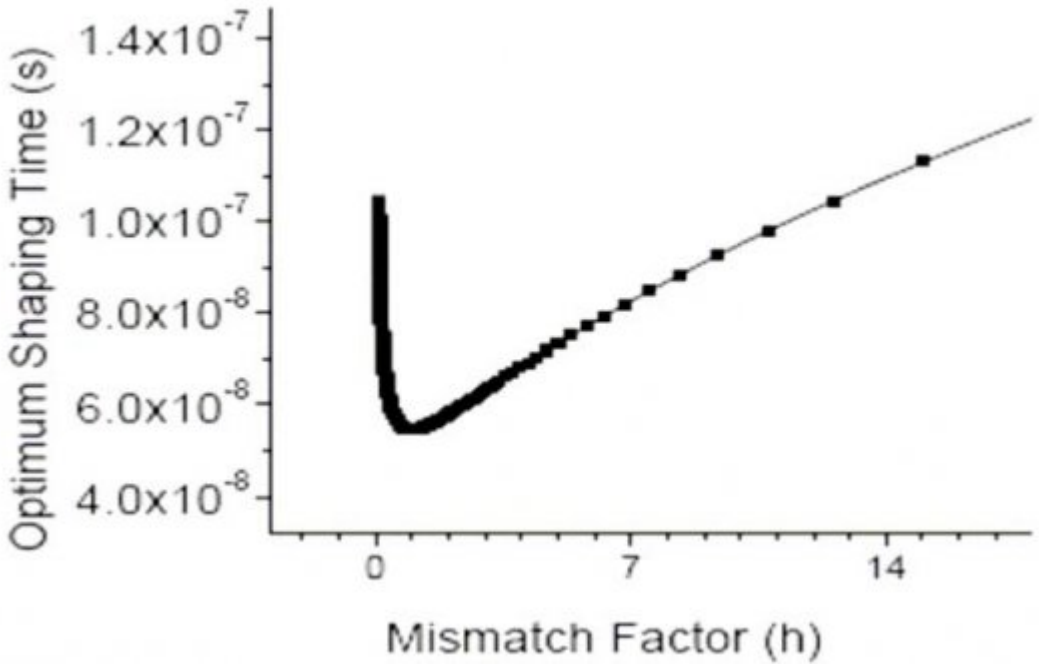

Figure 5:

$$ENC_1 = \frac{e}{2q}\sqrt{q \times T_M \times I_g} \quad \mathbf{e} = 2.718,\ \mathbf{q} = \text{electron charge}$$

21

Figure 6: Fig. 2 :A 1 -

$$T_M = 0.65 \times \frac{1}{2} \times \left(\sqrt{h} + 1/\sqrt{h}\right) \times \sqrt[3]{\frac{C_{FET}}{g_m}} \times \sqrt[3]{\frac{C_D}{I_{leak}}}$$

$$\text{Where } h = \frac{C_D}{C_{FET}} \qquad \text{(Mismatch Factor)}$$

3

Figure 7: Fig. 3 :

$$ENC_2 = \frac{e}{2q}\sqrt{q \times T_M \times I_D}$$

Figure 8:

$$\mathrm{ENC}^2 = \mathrm{ENC}_1{}^2 + \mathrm{ENC}_2{}^2 + \mathrm{ENC}_3{}^2 + \mathrm{ENC}_4{}^2$$

$$ENC = \sqrt{\mathrm{ENC}_1{}^2 + \mathrm{ENC}_2{}^2 + \mathrm{ENC}_3{}^2 + \mathrm{ENC}_4{}^2}$$

4

Figure 9: Fig. 4 :

$$ENC_4 = \frac{e}{2q} \times (C_D + C_F + C_{GS}) \times \sqrt{\frac{4 \times K \times T}{3 \times T_M \times g_m}}$$

Where C_D = Detector Capacitance
C_f = Feedback capacitor
C_{GS} = JFET gate-source capacitance

5

Figure 10: Fig. 5 :

$$ENC_3 = \frac{e}{2q} \sqrt{\frac{2 \times K \times T \times T_M}{R_P}}$$

Where $R_P = \frac{R_B \times R_f}{R_B \oplus R_f}$
$R_P = R_B \parallel R_f$
R_B = Bias resistor
R_f = Feedback resistor

Figure 11: A

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[2] A First Principle's Approach to Study of the Silicon Drift Detector with embedded JFET: Noise Analysis, Simulations & Analytical Modeling
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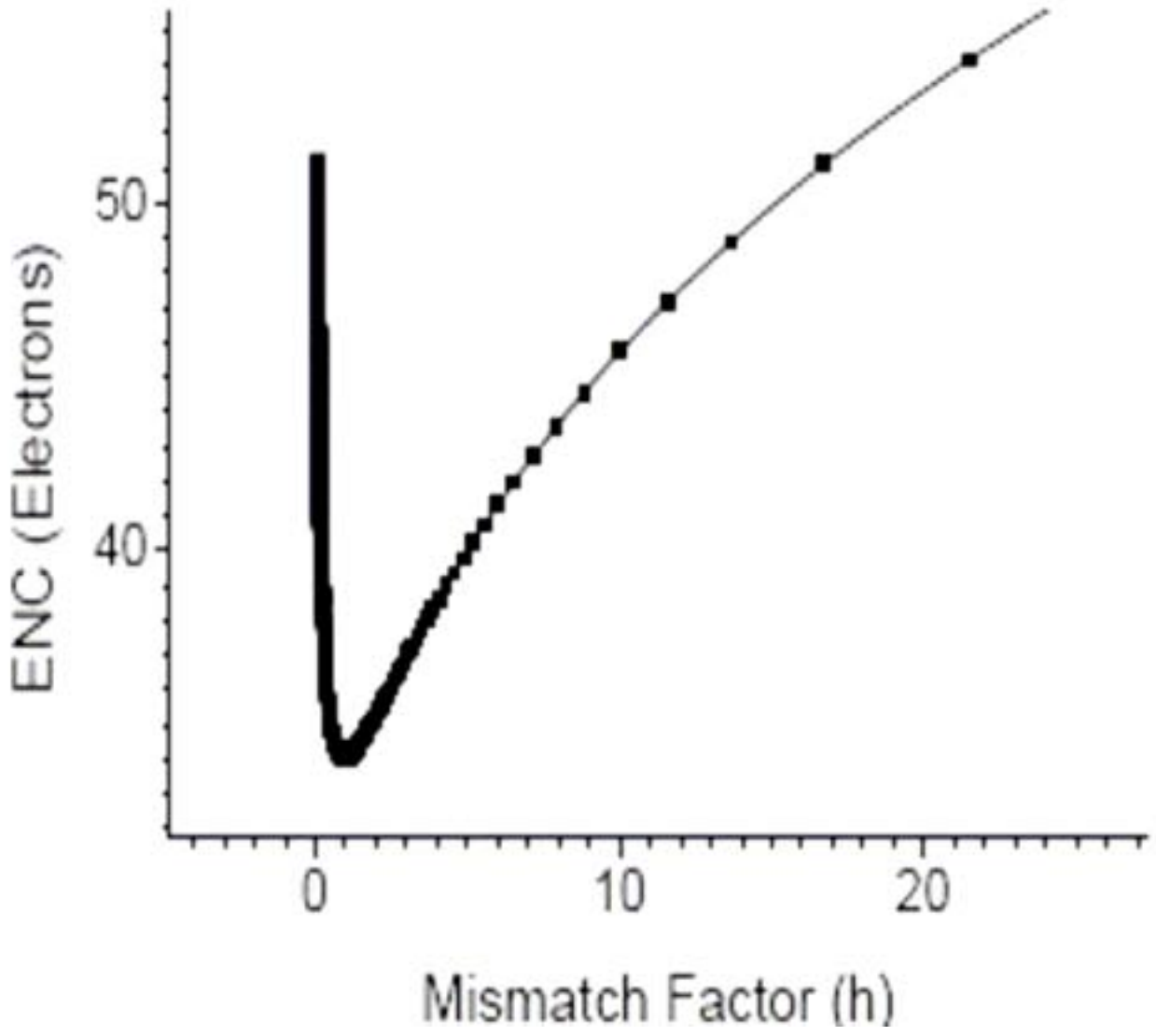

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Figure 12: VFig. 6 :

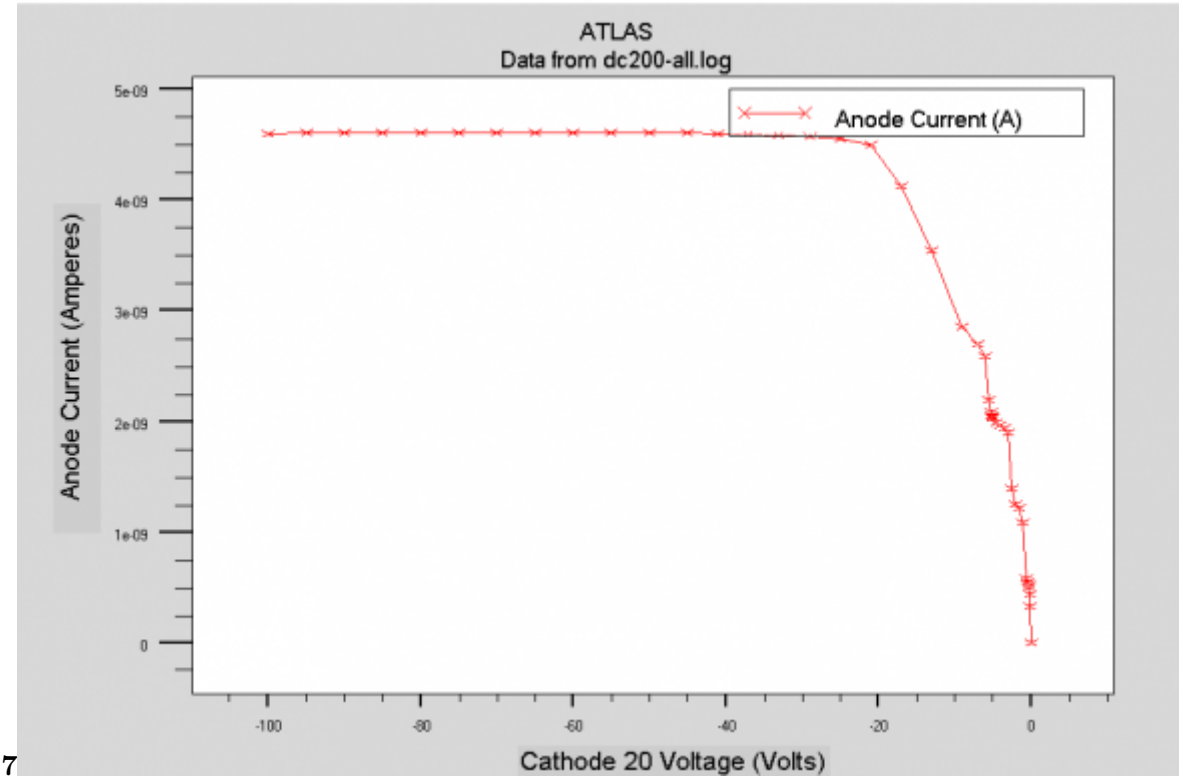

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Figure 13: Fig. 7 :

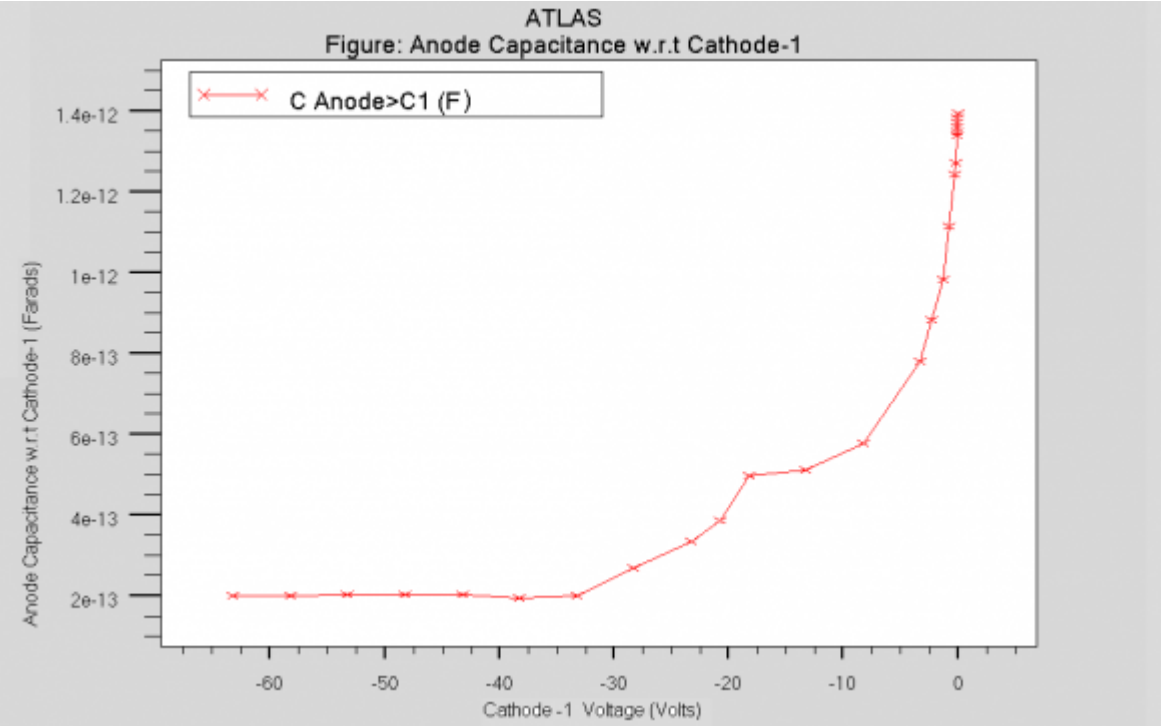

Figure 14:

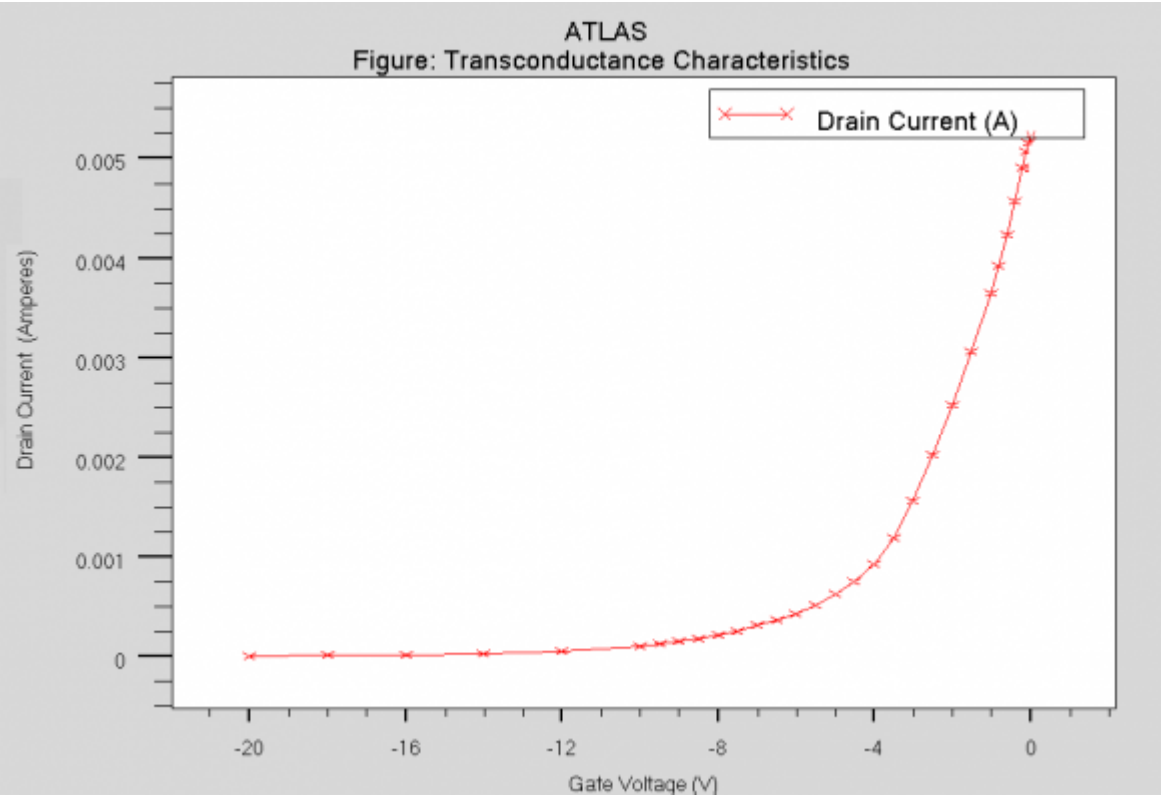

Figure 15:

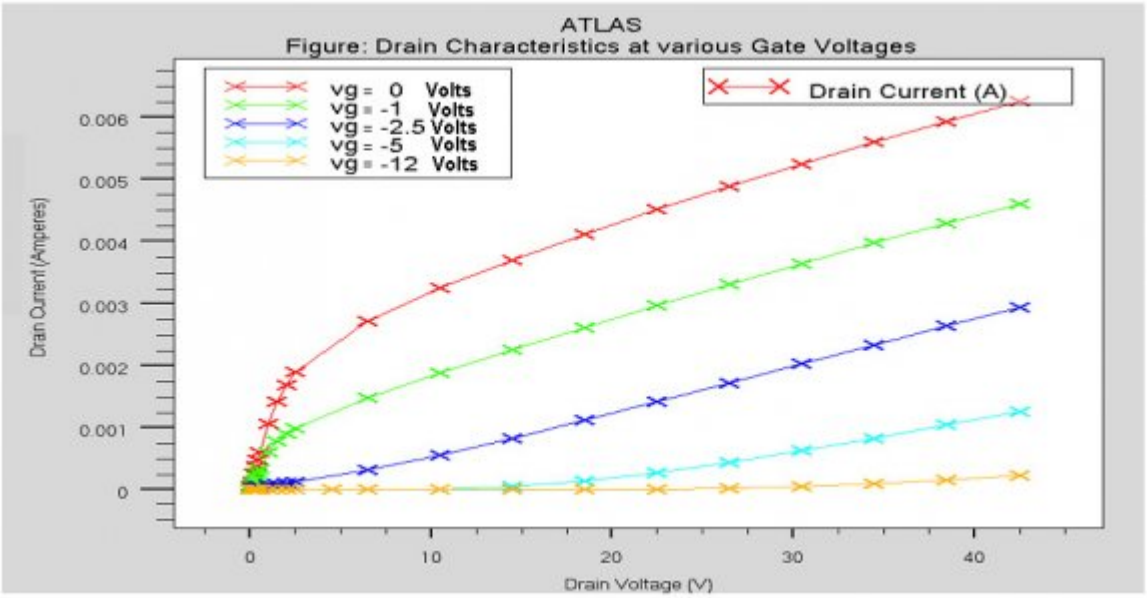

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Figure 16: Fig. 11 :

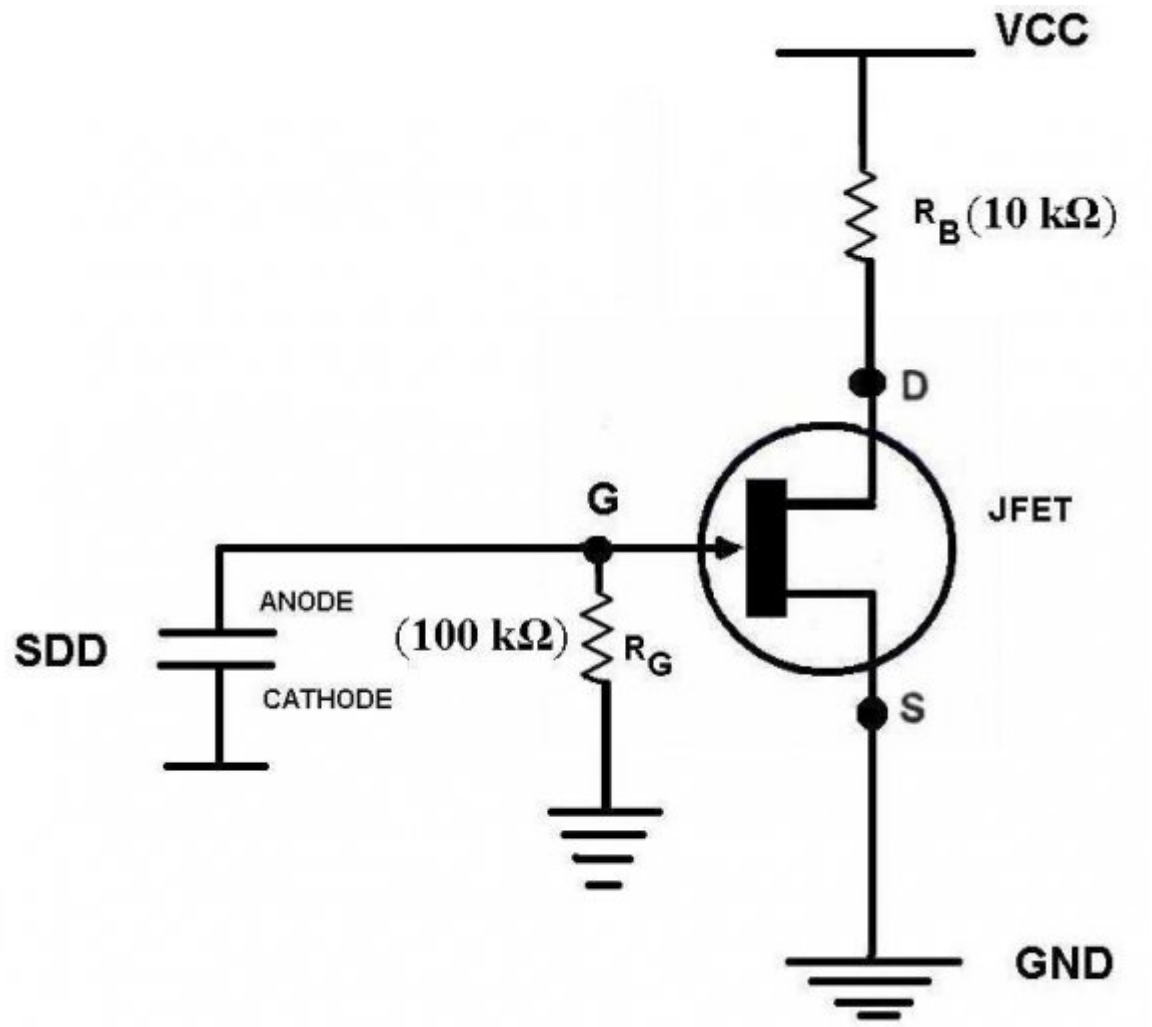

Figure 17: A

1

Figure 18: Table 1 :

.1 Acknowledgements

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