

# A Qualitative Approach to Design Multi Channel UART Using FPGA and FIFO Technologies

ravindraiah<sup>1</sup>, C.K.Hemantha Lakshmi<sup>2</sup> and C.K.Hemantha Lakshmi<sup>3</sup>

<sup>1</sup> Dept., of ECE, MITS, Madanapalle, Andhra Pradesh

*Received: 11 February 2012 Accepted: 29 February 2012 Published: 15 March 2012*

---

## Abstract

To meet modern complex control systems communication demands, my paper presents a multi channel UART controller based on FIFO (first in first out) and FPGA (field programmable gate array). The paper presents design method of asynchronous FIFO and structure of controller. This controller is designed with FIFO circuit block and UART (universal asynchronous receiver transmitter) circuit block with in FPGA to implement communication in modern complex control systems quickly and effectively. This controller can be used to implement communication when master equipment and slaver equipment are set at different baud rate. It can also be used to reduce synchronization error between sub systems in a system with several sub systems. The controller is reconfigurable and scalable. The whole scenario is simulated using VHDL coding.

---

*Index terms*— communication, complex, programmable, synchronization.

## 1 Introduction

oday, owing to availability of state-of-the-art microcontrollers and digital signal processors (DSPs), complex control algorithms can be easily implemented to attain the desired system performance [3]. But in actual control systems it is difficult to attain the expected result for various factors affect the control systems such as control algorithms itself, capability of implement equipment and states of control circumstance. Except those factors, communication parameters of control systems including baud rate, BER (bit error rate) and synchronization between sub systems also engender great effect. In order to improve precision of control system and make good use of modern control algorithms, we should pay much more attention on communication in control systems [1].

In several control systems, UART a kind of serial communication circuit used widely. A universal asynchronous receive transmit is an integrated circuit which plays most important role in serial communication. It handles the conversion between serial and parallel data. Serial communication reduces the distortion of a signal therefore makes data transfer between two systems separated in great distance possible [2].

In some complex systems, communications between the master controller and slaver controllers are implemented by serial or parallel port. Parallel communication needs a lot of multi-bit address bus and data bus and it is only convenient for short distance transmission. Serial communication is another way of communication used extensively because of its simple structure and long transmission distance. But sometimes a common serial port could not meet requirements of complex systems with different baud rates equipments even some special baud rate equipments. It is impossible to implement this multi baud rate communication system without a special baud rate converter [3]. A RAM array with separate read and write ports is used to store data. The writer pointer points to the location that will be written next, and read pointer points to the location that will be read currently. A write operation increments the writer pointer and read operation increments the read pointer. On reset, both pointers are reset to zero, the FIFO is empty. The write pointer happens to be the next FIFO location to be written and read pointer is pointing to invalid data. The responsibility of status block is to generate the EMPTY and FULL signals to the FIFO [4]. If the FULL signal is active then the FIFO cannot accommodate

44 more data and if the EMPTY is active then the FIFO cannot provide more data to read out. When writing data  
45 into the FIFO "wclk" will be used as the clock domain and when reading data out of the FIFO "rclk" will be used  
46 as the clock domain. These both clock domains are asynchronous.

### 47 **2 c) Factors for the design of Asynchronous FIFO**

48 In the designing of asynchronous FIFOs, two important factors are considered. One is how to judge FIFOs status  
49 according to the writer pointer and read pointer. The other is how to design circuit to synchronize asynchronous  
50 clock domains to avoid metastability. We can use software codes in VHDL to design FPGAs hardware structure,  
51 it is easy to create and adjust to satisfy requirements of applications. There are one UART used to communicate  
52 with PC or other main MCU and there are also four other UARTs used to communication with sub MCUs [5].  
53 Each channel has two FIFOs one for receiving data and the other for transmitting data. Each FIFO's depth is  
54 64 bytes. The software flow chart is shown in figure 6. As shown in figure ,when FIFO is full we cannot write  
55 any more byte into the FIFO. At this time, the status detector will set CS high to indicate that the FIFO is full  
56 and when FIFO is full you cannot write any more byte into the FIFO. At this time, the status detector will set  
57 CS high to indicate that the FIFO is full and stop writing to the FIFO. When FIFO is empty we cannot read  
58 from it any more. Then the status detector will set empty high to indicate the status of FIFO and stop reading  
59 from it [6] [7].

60 When FIFO is not full or empty it will be written or read data according to the control order. After finishing  
61 all write or read operation it will stop until next access is coming.

### 62 **3 III.**

### 63 **4 Simulation Results**

### 64 **5 a) Simulation And Verification**

65 To verify design of the controller a test bench is written to make verification in modelsim .Data received from  
66 the PC or other main MCU will be stored in FIFO's within FPGA till the controller will set a kind of baud rate  
67 according to commands desired. The controller is receiving data and store the data received to different FIFO  
68 waiting for read. When sub-controllers are required to receive data at different baud rates, the controller can  
69 set each channel at its required baud rate to transmit data. The controller sends data at the same time but at  
70 different baud rate. IV.

### 71 **6 Conclusion**

72 This paper introduces a method to design a method to design a asynchronous FIFO based on FPGA. And using  
73 asynchronous FIFO technique implements a multi channel UART controller within FPGA based on SRAM with  
74 high speed and reliability .The controller can be used to implement communications in complex system with  
75 different baud rates of sub controllers. And it also can be used to reduce time delays between sub controllers of  
76 a complex control system to improve the synchronization of each sub controller. The controller is reconfigurable,  
77 so the controller's fault is that it would be influenced by the radiation from surroundings and by short time  
78 pulses easily. <sup>1 2 3 4 5</sup>

---

<sup>1</sup>F © 2012 Global Journals Inc. (US)2012JulyAuthor ? : Assistant Professor, Dept., of ECE, MITS, Madanapalle, Andhra Pradesh. E-mail : hemanthaster@gmail.com Author ? : Assistant Professor, Dept., of CSE, KEC, Kuppam, Andhra Pradesh. Email : ckhemantha@gmail.com Author ? : M.Tech, Dept of EEE., NIT Nagpur, Email : ckmahesh111@gmail.com

<sup>2</sup>© 2012 Global Journals Inc. (US)2012July different, it means that the write pointer has wrapped one more time that the read pointer. If the MSBs of the two pointers are the same, it means that both pointers have wrapped the same number of times.

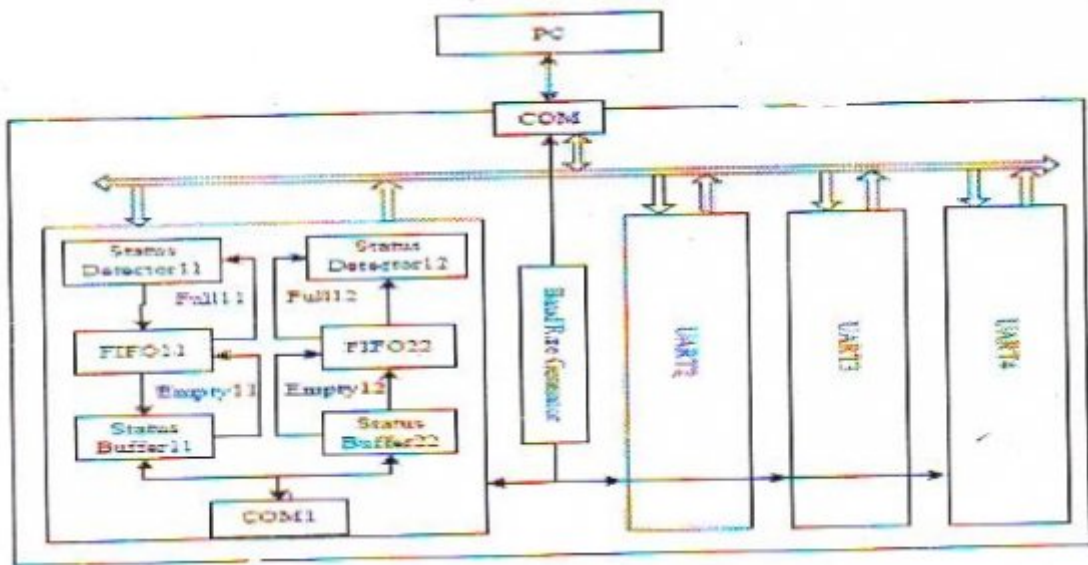
<sup>3</sup>F © 2012 Global Journals Inc. (US) 2012 July

<sup>4</sup>© 2012 Global Journals Inc. (US)

<sup>5</sup>© 2012 Global Journals Inc. (US) 2012 July



Figure 1:



1

Figure 2: Figure 1 :

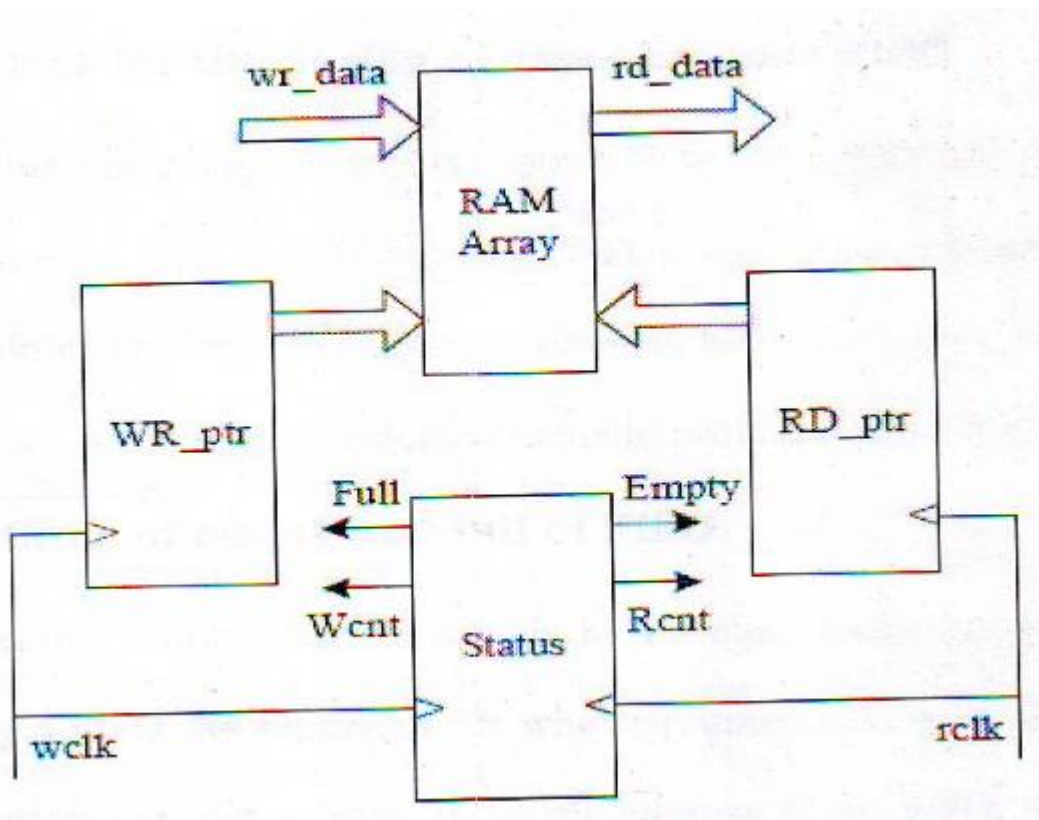
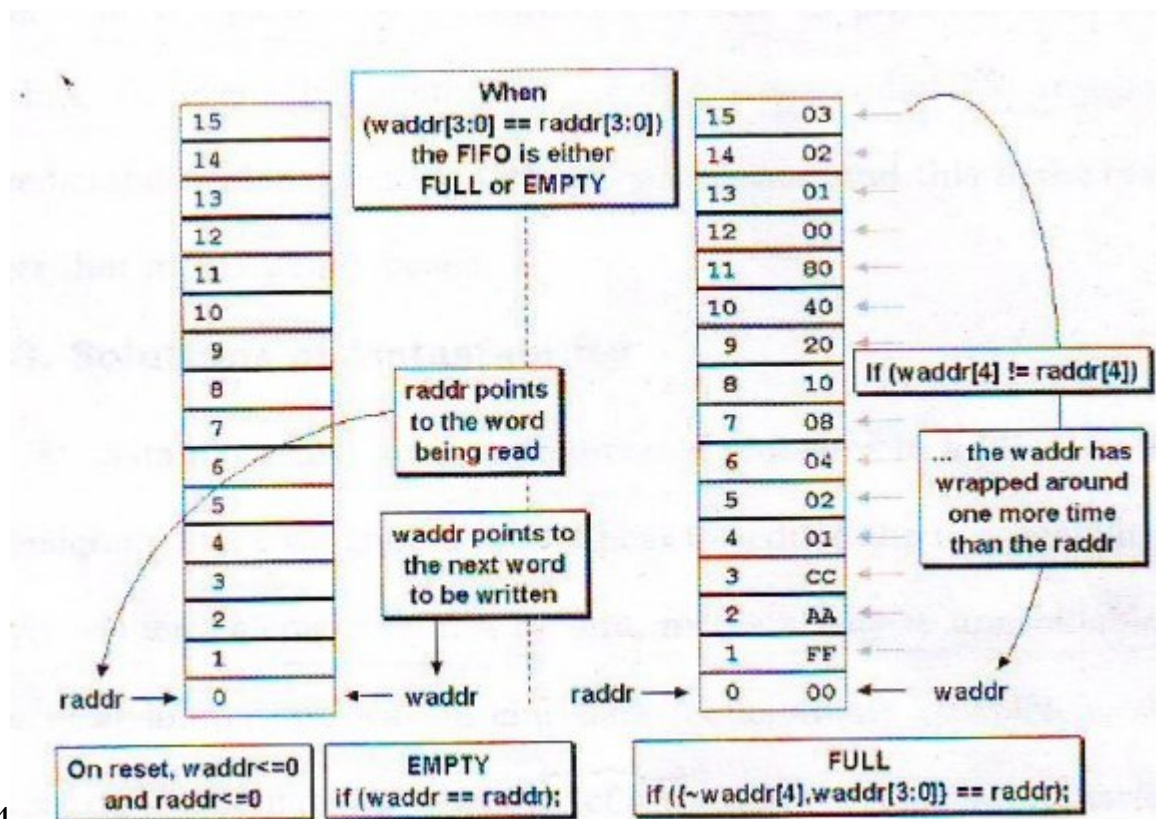
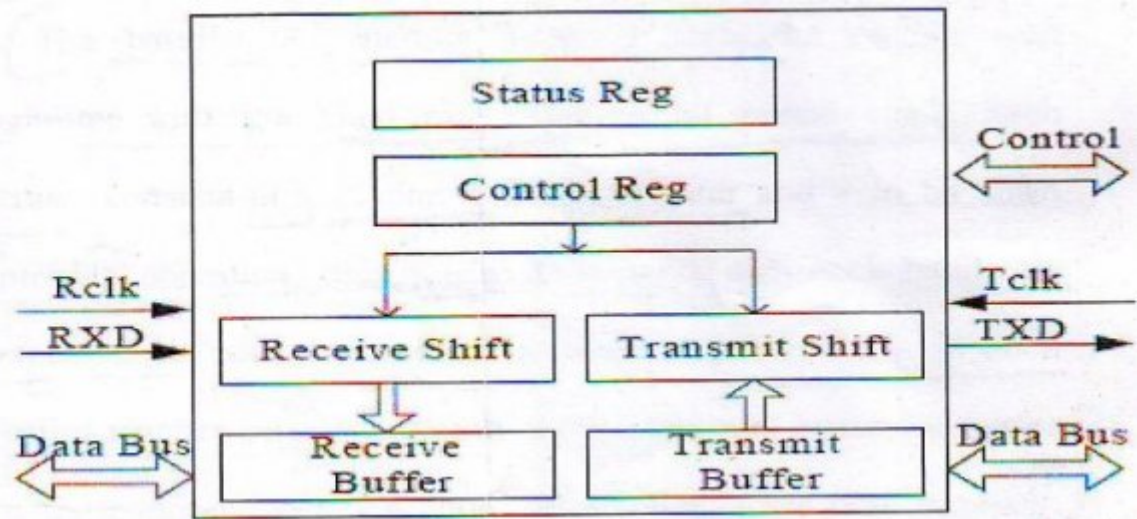


Figure 3:



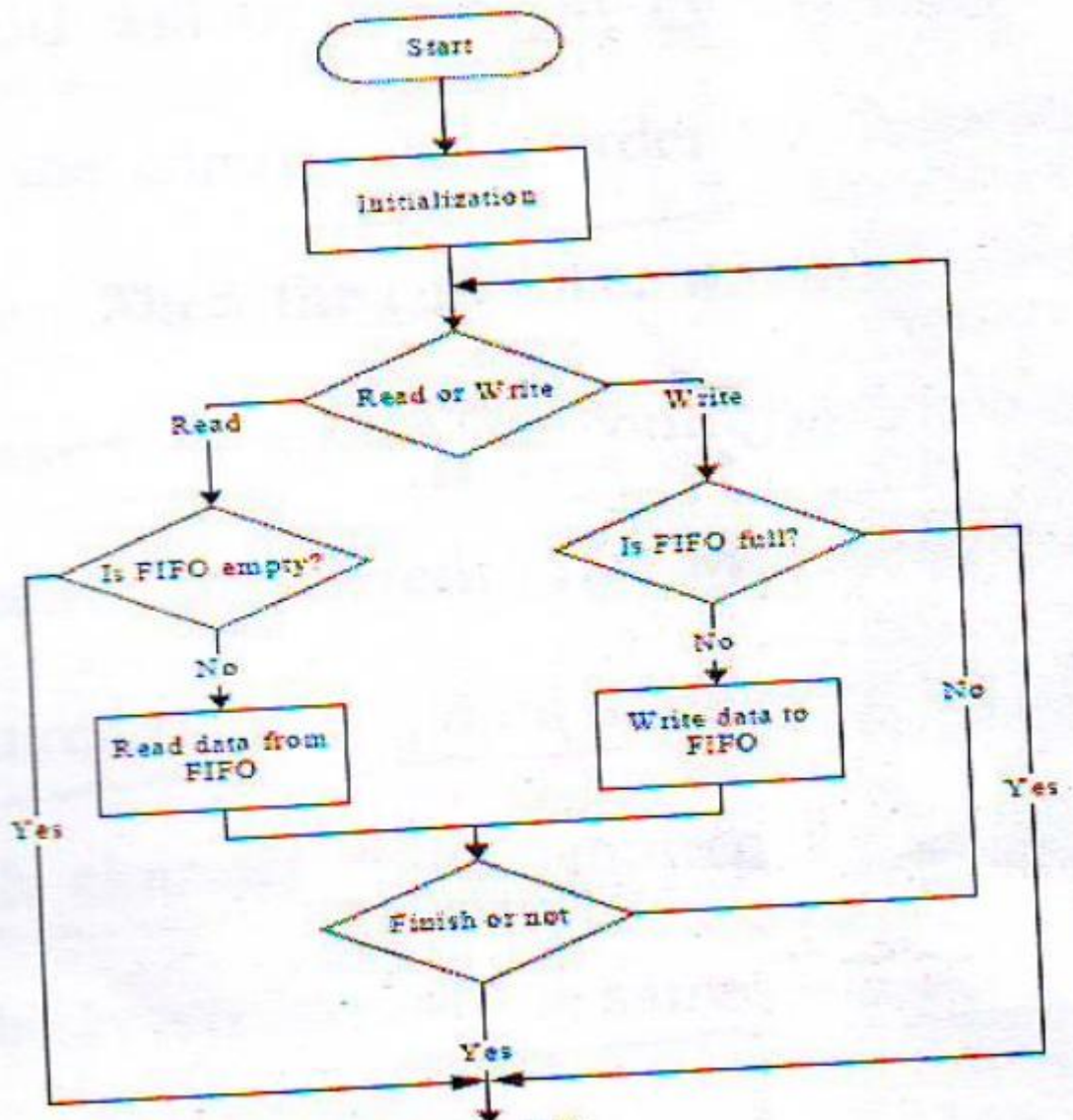
34

Figure 4: Figure 3 :Figure 4 :



5

Figure 5: Figure 5 :



6

Figure 6: Figure 6 :

## 6 CONCLUSION

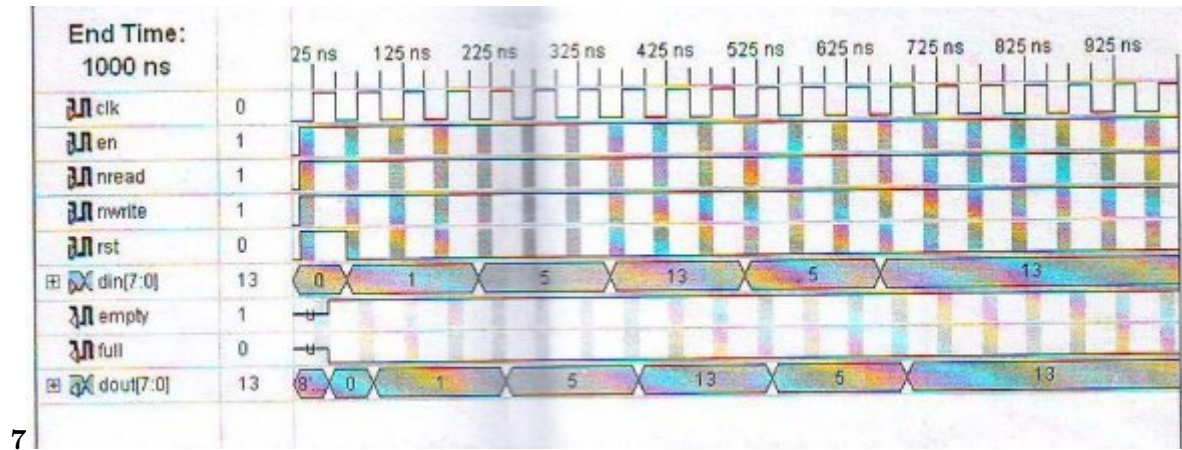


Figure 7: Figure 7 :

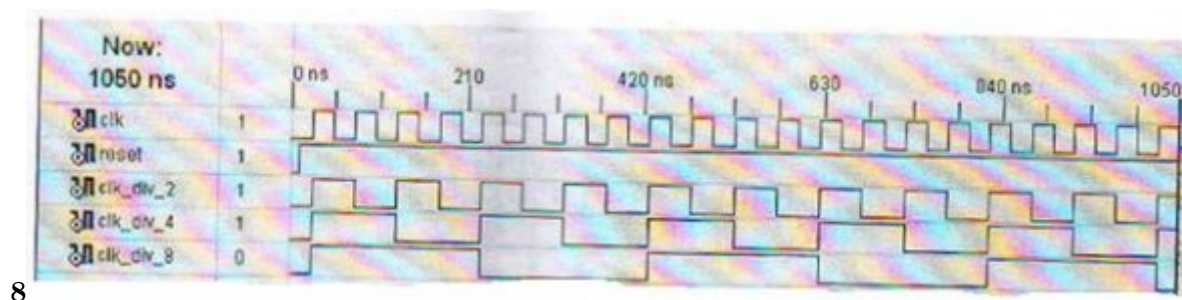


Figure 8: Figure 8 :

- 
- 79 [Jayram Bhaskar and Primer] , ”a Vhdl Jayram Bhaskar , Primer . Prentice Hall Publications. (2nd edition)
- 80 [Stallings] *Data and Computer communications*, William Stallings . McGraw-Hill publications.
- 81 [Wu and Dai (2006)] ‘Design of interface Between High speed A/D and DSP based on FIFO’. X D Wu , B Dai .
- 82 *Journal of Beijing Institute of petrochemical Technology* June 2006. 14 (12) p. .
- 83 [Brown and Vranesic (2004)] *Fundamentals of Digital Logic with VHDL Design*, Stephen Brown , Zvonko
- 84 Vranesic . July 2004. McGraw-Hill, Hardcover, Published. (2nd edition)
- 85 [Pan et al. (2006)] ‘Implementation of Parallel Signal processing system based on FPGA and multi-DSP’. F S
- 86 Pan , F Zhao , J Xi , Y Luo . *Computer Engineering* Dec 2006. 32 (23) p. .
- 87 [Roth] Charles H Roth . *Digital system design using VHDL*, (2nd edition, Thomson publication)
- 88 [Hu and Wang (2006)] ‘UART -Based reliable Communication and performance analysis’. L K Hu , Q Wang .
- 89 *Computer Engineering* May 2006. 32 (10) p. .
- 90 [Nawabi (1998)] *VHDL Analysis and Modeling of Digital systems*, Zainalabedin Nawabi . January 1998.
- 91 Hardcover. (2nd edition. Published)